Suggested Retail Price: $19.95

TEXAS INSTRUMENTS

Programmable Logic

Data Book

1993

The Programmable Logic
Data Book

Texas
Instruments

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to current specifications in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Please be aware that TI products are not intended for use in life-support appliances, devices, or systems. Use of TI product in such applications requires the written approval of the appropriate TI officer. Certain applications using semiconductor devices may involve potential risks of personal injury, property damage, or loss of life. In order to minimize these risks, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards. Inclusion of TI products in such applications is understood to be fully at the risk of the customer using TI devices or systems.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Copyright © 1993, Texas Instruments Incorporated

INTRODUCTION

In this data book, Texas Instruments (TI) provides comprehensive information about TI's programmable logic devices (PLDs). These products have been developed to meet your performance and time to market requirements with efficient and effective products. TI offers over 40 PLD products in the standard architecture with speeds ranging from the low-power 25-ns to the high-speed 5-ns devices. TI also offers the flexible '22V10-architecture in the same speed range as the standard architecture product, including 5-ns tpd.

The 25-ns and 15-ns programmable bipolar devices utilize TI's IMPACT™ process while the high-speed bipolar devices utilize TI's IMPACT-X™ technologies. The IMPACT-X™ uses trench isolation and polysilicon emitters to increase performance. The IMPACT-XL™ process uses arsenic doped emitters and is optimized for low capacitance to achieve further improvements in performance.

Besides the design and specifications data we have also included characterization data, packaging data, as well as process and die data to further assist you in designing with and qualifying TI's PLDs. All TI PLDs use a titanium-tungsten (TiW) fuse technology developed at TI to improve programming reliability.

Thank you for selecting Texas Instruments as your PLD supplier. If we can be of further assistance or if you require more information please contact your local TI field sales office, authorized distributor, or TI's PLD/FPGA Help Line at 214- 997-5666.

IMPACT, IMPACT-X, and IMPACT-XL are trademarks of Texas Instruments Incorporated.

ALPHANUMERIC INDEX

INTRODUCTION

These symbols, terms, and definitions are in accordance with those currently agreed upon by the JEDEC Council of the Electronic Industries Association (EIA) for use in the USA and by the International Electrotechnical commission (IEC) for international use.

PART 1 — GENERAL CONCEPTS AND CLASSIFICATIONS OF CIRCUIT COMPLEXITY

Chip-Enable Input

A control input that when active permits operation of the integrated circuit for input, internal transfer, manipulation, refreshing, and/or output of data and when inactive causes the integrated circuit to be in reduced-power standby mode.
NOTE: See chip-select input.

Chip-Select Input

A gating input that when inactive prevents input or output of data to or from the integrated circuit.
NOTE: See chip-enable input.

Field-Programmable Logic Array (FPLA)

A user-programmable integrated circuit whose basic structure consists of a programmable AND array and whose outputs feed a programmable OR array.

Gate Equivalent Circuit

A basic unit-of-measure of relative digital-circuit complexity. The number of gate-equivalent circuits is that number of individual logic gates that would have to be interconnected to perform the same function.

Large-Scale Integration (LSI)

A concept whereby a complete major subsystem or system function is fabricated as a single microcircuit. In this context, a major subsystem or system, whether digital or linear, is considered to be one that contains 100 or more equivalent gates or circuitry of similar complexity.

Medium-Scale Integration (MSI)

A concept whereby a complete subsystem or system function is fabricated as a single microcircuit. The subsystem or system is smaller than for LSI, but whether digital or linear, is considered to be one that contains 12 or more equivalent gates or circuitry of similar complexity.

Output-Enable Input

A gating input that when active permits the integrated circuit to output data and when inactive causes the integrated circuit output(s) to be at a high impedance (off).

Programmable Array Logic (PAL®)

A user-programmable integrated circuit which utilizes proven fuse link technology to implement logic functions. Implements sum of products logic by using a programmable AND array whose outputs feed a fixed OR array.

PAL is a registered trademark of Advanced Micro Devices Inc.

Small-Scale Integration (SSI)

Integrated circuits of less complexity than medium-scale integration (MSI).

Typical (TYP)

A calculated value representative of the specified parameter at nominal operating conditions (V_{CC} = 5 V, T_A = 25°C), based on the measured value of devices processed, to emulate the process distribution.

Very-Large-Scale Integration (VLSI)

A concept whereby a complete system function is fabricated as a single microcircuit. In this context, a system, whether digital or linear, is considered to be one that contains 3000 or more gates or circuity of similar complexity.

PART 2 — OPERATING CONDITIONS AND CHARACTERISTICS (IN SEQUENCE BY LETTER SYMBOLS)

C_i	**Input capacitance** The internal capacitance at an input of the device.
C_o	**Output capacitance** The internal capacitance at an output of the device.
f_{max}	**Maximum clock frequency** The highest rate at which the clock input of a bistable circuit can be driven through its required sequence while maintaining stable transitions of logic level at the output with input conditions established that should cause changes of output logic level in accordance with the specification.
I_{CC}	**Supply current** The current into* the VCC supply terminal of an integrated circuit.
I_{IH}	**High-level input current** The current into* an input when a high-level voltage is applied to that input.
I_{IL}	**Low-level input current** The current into* an input when a low-level voltage is applied to that input.
I_{OH}	**High-level output current** The current into* an output with input conditions applied that, according to the product specification, will establish a high level at the output.
I_{OL}	**Low-level output current** The current into* an output with input conditions applied that, according to the product specification, will establish a low level at the output.
I_{OS} (I_O)	**Short-circuit output current** The current into* an output when that output is short-circuited to ground (or other specified potential) with input conditions applied to establish the output logic level farthest from ground potential (or other specified potential).
I_{OZH}	**Off-state (high-impedance-state) output current (of a three-state output) with high-level voltage applied** The current flowing into* an output having three-state capability with input conditions established that, according to the product specification, will establish the high-impedance state at the output and with a high-level voltage applied to the output. NOTE: This parameter is measured with other input conditions established that would cause the output to be at a low level if it were enabled.
I_{OZL}	**Off-state (high-impedance-state) output current (of a three-state output) with low-level voltage applied** The current flowing into* an output having three-state capability with input conditions established that, according to the product specification, will establish the high-impedance state at the output and with a low-level voltage applied to the output. NOTE: This parameter is measured with other input conditions established that would cause the output to be at a high level if it were enabled.

* Current out of a terminal is given as a negative value.

V_{IH}	**High-level input voltage** An input voltage within the more positive (less negative) of the two ranges of values used to represent the binary variables. NOTE: A minimum is specified that is the least-positive value of high-level input voltage for which operation of the logic element within specification limits is guaranteed.
V_{IK}	**Input clamp voltage** An input voltage in a region of relatively low differential resistance that serves to limit the input voltage swing.
V_{IL}	**Low-level input voltage** An input voltage within the less positive (more negative) of the two ranges of values used to represent the binary variables. NOTE: A minimum is specified that is the most-positive value of low-level input voltage for which operation of the logic element within specification limits is guaranteed.
V_{OH}	**High-level output voltage** The voltage at an output terminal with input conditions applied that, according to product specification, will establish a high level at the output.
V_{OL}	**Low-level output voltage** The voltage at an output terminal with input conditions applied that, according to product specification, will establish a low level at the output.
t_{dis}	**Disable time (of a three-state output)** The time interval between the specified reference points on the input and output voltage waveforms, with the three-state output changing from either of the defined active levels (high or low) to a high-impedance (off) state. ($t_{dis} = t_{PHZ}$ or t_{PLZ}).
t_{en}	**Enable time (of a three-state output)** The time interval between the specified reference points on the input and output voltage waveforms, with the three-state output changing from a high-impedance (off) state to either of the defined active levels (high or low). ($t_{en} = t_{PZH}$ or t_{PZL}).
t_h	**Hold time** The time interval during which a signal is retained at a specified input terminal after an active transition occurs at another specified input terminal. NOTES 1: The hold time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed. 2. The hold time may have a negative value in which case the minimum limit defines the longest interval (between the release of the signal and the active transition) for which correct operation of the digital circuit is guaranteed.
t_{pd}	**Propagation delay time** The time between the specified reference points on the input and output voltage waveforms with the output changing from one defined level (high or low) to the other defined level. ($t_{pd} = t_{PHL}$ or t_{PLH}).

t_{PHL}	**Propagation delay time, high-to-low level output** The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined high level to the defined low level.
t_{PHZ}	**Disable time (of a three-state output) from high level** The time interval between the specified reference points on the input and the output voltage waveforms with the three-state output changing from the defined high level to a high-impedance (off) state.
t_{PLH}	**Propagation delay time, low-to-high level output** The time between the specified reference points on the input and output voltage waveforms with the output changing from the defined low level to the defined high level.
t_{PLZ}	**Disable time (of a three-state output) from low level** The time interval between the specified reference points on the input and the output voltage waveforms with the three-state output changing from the defined low level to a high-impedance (off) state.
t_{PZH}	**Enable time (of a three-state output) to high level** The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined high level.
t_{PZL}	**Enable time (of a three-state output) to low level** The time interval between the specified reference points on the input and output voltage waveforms with the three-state output changing from a high-impedance (off) state to the defined low level.
$t_{sk(o)}$	**Output Skew** The time interval between any two propagation delay times when a single switching input or multiple inputs switching simultaneously causes multiple outputs to switch, as observed across all switching outputs.
t_{su}	**Setup time** The time interval between the application of a signal at a specified input terminal and a subsequent active transition at another specified input terminal. NOTES 1: The setup time is the actual time interval between two signal events and is determined by the system in which the digital circuit operates. A minimum value is specified that is the shortest interval for which correct operation of the digital circuit is guaranteed. 2. The setup time may have a negative value in which case the minimum limit defines the longest interval (between the active transition and the application of the other signal) for which correct operation of the digital circuit is guaranteed.
t_w	**Pulse duration (width)** The time interval between specified reference points on the leading and trailing edges of the pulse waveform.

EXPLANATION OF FUNCTION TABLES

The following symbols are used in function tables on TI data sheets.

H = high level (steady state)

L = low level (steady state)

↑ = transition from low to high level

↓ = transition from high to low level

→ = value/level or resulting value/level is routed to indicated destination

↶ = value/level is reentered

X = irrelevant (any input, including transitions)

Z = off (high impedance) state of a 3-state output

a ... h = the level of steady-state inputs A through H respectively

Q_0 = the level of Q before the indicated steady-state input conditions were established

$\overline{Q}_0$ = complement of Q_0 or level $\overline{Q}$ before the indicated steady-state input conditions were established

Q_n = level of Q before the most recent active transition indicated by ↓ or ↑

_|‾|_ = one high-level pulse

‾|_|‾ = one low-level pulse

TOGGLE = each output changes to the complement of its previous level on each transition indicated by ↓ or ↑

If, in the input columns, a row contains only the symbols H, L, and/or X, this means the indicated output is valid whenever the input configuration is achieved and regardless of the sequence in which it is achieved. The output persists so long as the input configuration is maintained.

If, in the input columns, a row contains H, L, and/or X together with ↑ or ↓, this means the output is valid whenever the input configuration is achieved but the transition(s) must occur following the achievement of the steady-state levels. If the output is shown as a level (H, L, Q_0, or $\overline{Q}_0$), it persists so long as the steady-state input levels and the levels that terminate indicated transitions are maintained. Unless otherwise indicated, input transitions in the opposite direction to those shown have no effect at the output. (If the output is shown as a pulse, _|‾|_ or ‾|_|‾, the pulse follows the indicated input transition and persists for an interval dependent on the circuit.

PLD NUMBERING SYSTEM AND ORDERING INSTRUCTIONS

Factory orders for leadership PLD circuits described in this catalog should include a nine-part type number as explained in the example below. Exclude the prefix when ordering standard PLDs or One-Time Programmable Logic Devices.

EXAMPLE: **TIB PAL 16 R 8 -5 C N**

Prefix
TIB = Bipolar PLD
TIC = CMOS PLD

Product Family Designator

Number of Array Inputs

Output Configuration Designator
R = Registered
L = Active Low

Number of Outputs in the Designated Configuration

Performance Designator

HIGH-SPEED	LOW-POWER
A	A-2
-5	-25

Temperature Range
C = Commerical (0°C to 75°C)
I = Indrustal (−40°C to 85°C)
M = Military (−55°C to 125°C)

Package Type
N = 20-pin Plastic DIP
N = 28-pin, 600-mil Plastic DIP
J = 20-pin Ceramic DIP
NT = 20-pin, 300-mil Plastic DIP
JT = 20-pin, 300-mil Ceramic DIP
FN = Plastic Chip Carrier
FK = Ceramic Chip Carrier
W = Ceramic Flat Pak

ADDRESSES FOR PLD AND FPLA PROGRAMMING AND SOFTWARE MANUFACTURERS

ACUGEN Software Inc.
427-3 Amherst St.
Suite 391
Nashua, NH 03063
(603) 891-1995

Advin Systems
1050-L East Duane Ave.
Sunnyvale, CA 94086
(408) 984-8600

BP Microsystems
10681 Haddington
Suite 190
Houston, TX 77043
(713) 461-9430

Bytek Corporation
508 Northwest 77th St.
Boca Raton, FL 33487
(407) 994-3520

Data I/O Corporation
10525 Willows Road N.E.
Redmond, WA 98073
(800) 247-5700

ISDATA GmbH
Daimlerstr. 51
W-5700 Karlsruhe 21
Federal Republic of Germany
0721/75 10 87

Logic Devices Inc.
1201 N.W. 65th Place
Ft. Lauderdale, FL 33309
(800) 331-7766

MINC Incorporated
6755 Earl Drive
Colorado Springs, CO 80918
(719) 590-1155

ProLogic Systems Inc.*
2100-C West 6th Ave.
Broomfield, CO 80020
(303) 460-0103
* Formerly Inlab Inc.

SMS
Im Morgental 13
8994 Hergatz
Federal Republic of Germany
(49) 755-5018

Stag Microsystems
1600 Wyatt Drive
Santa Clara, CA 95054
(800) 227-8836

System General Corporation
510 South Park Victoria Drive
Malpitas, CA 95035
(408) 263-6667

Texas Instruments Incorporated
P.O. Box 655303, MS 3686
Dallas, TX 75265
(214) 997-5666

IMPACT™ DESIGN AND SERVICE CENTERS

Design and programming assistance is offered by Texas Instruments IMPACT™ Design and service Centers. The centers are equipped with the latest in software and hardware tools for design, debugging, creating prototypes, and production on a local basis. Supported by a professional engineering staff, the centers provide complete code development, device programming, symbolization, functional and static (dc) parametric testing.

Anthem Electronics, Inc.
1160 Ridder Park Drive
San Jose, CA 95131
(408) 453-2200

Anthem Electronics, Inc.
373 Inverness Drive South
Englewood, CO 80112
(303) 790-4500

Arrow/Schweber Electronics, Inc.
17822 Gillett Avenue
Irvine, CA 92714
(714) 587-0404

Arrow/Schweber Electronics, Inc.
1180 Murphy Avenue
San Jose, CA 95131
(408) 441-9700

Arrow/Schweber Electronics, Inc.
4250 River Green Parkway
Suite E
Duluth, GA 30131
(404) 497-1300

Arrow/Schweber Electronics, Inc.
665 Spice Island Drive
Sparks, NV 89431
(800) 777-Arrow

Hall-Mark Electronics Corp.
1 Mauchly
Irvine, CA 92715
(714) 727-6000

Hall-Mark Electronics Corp.
2105 Lundy Avenue
San Jose, CA 95131
(408) 432-4000

Hall-Mark Electronics Corp.
6 Cook Street
Pinehurst Park
Billerica, MA 01821
(508) 667-0902

Hall-Mark Electronics Corp.
11420 Pagemill Road
Dallas, TX 75243
(214) 553-4300

Marshall Industries
9320 Telestar
El Monte, CA 91731
(818) 307-6208

Marshall Industries
336 Los Coches Street
Milpitas, CA 95035
(408) 942-4600

Marshall Industries
33 Upton Drive
Wilmington, MA 01887
(508) 658-0810

Marshall Industries
2045 Chenault Street
Carrollton, TX 75008
(214) 233-5200

Wyle Electronics Marketing Group
5191 Oceanus
Huntington Beach, CA 92649
(714) 863-9953

Wyle Electronics Marketing Group
3000 Bowers Avenue
Santa Clara, CA 95051
(408) 727-2500

Wyle Electronics Marketing Group
452 East 124th Avenue
Thornton, CO 80241
(303) 457-9953

Wyle Electronics Marketing Group
1810 Greenville Avenue
Dallas, TX 75081
(214) 235-9953

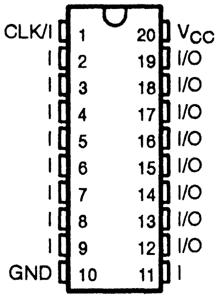
IMPACT is a trademark of Texas Instruments Incorporated.

EP330 SERIES
HIGH-PERFORMANCE 8-MACROCELL ONE-TIME PROGRAMMABLE LOGIC DEVICES

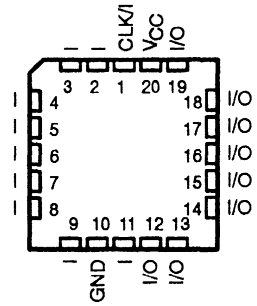
SRES002A – D3374, OCTOBER 1989 – REVISED SEPTEMBER 1992

- **Programmable Replacement for Conventional TTL, 74HC, and 20-Pin PLD Family**
- **High-Voltage EPIC™ Process Allows for Higher Performance as Follows:**
  Maximum t_{pd}: -12C . . . 12 ns
  -15C . . . 15 ns
  -25I . . . 25 ns
- **User-Programmable Output Logic Macrocells Provide Flexibility in Output Types With:**
  - **Selectable for Registered or Combinational Operation**
  - **Output Polarity Control**
  - **Independently User Programmable Feedback Path**
- **Programmable Design-Security Bit Prevents Copying of Logic Stored in Device**
- **Third-Party Advanced Software Support Featuring Schematic Capture, Interactive Netlist, Boolean Equations, and State-Machine Design Entry**
- **Package Options Include:**
  - **20-pin Plastic Dual-In-Line (N)**
  - **20-pin Plastic Chip Carrier (FN)**

N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



Pin assignments in operating mode

description

general

The EP330 features advanced-CMOS speed and very low power utilizing Texas Instruments High-Voltage Enhanced-Processed Implanted CMOS (HVEPIC) process. Each output has an Output-Logic-Macrocell (OLM) configuration that allows user definition of the output type. The EP330 provides a reliable low-power substitute for numerous high-performance TTL PLDs.

The EP330 can accommodate up to 18 inputs and up to eight outputs. The 20-pin 300-mil package contains eight macrocells each using a programmable AND/fixed-OR structure. This AND-OR structure yields eight product terms for the logic function as well as an individual term for Output Enable.

AVAILABLE OPTIONS

T_A RANGE	SPEED CLASS	PACKAGE TYPE	
		PLASTIC DUAL-IN-LINE (N)	PLASTIC CHIP CARRIER (FN)
0°C to 70°C	12 ns	EP330-12CN	EP330-12CFN
	15 ns	EP330-15CN	EP330-15CFN
–40°C to 85°C	25 ns	EP330-25IN	EP330-25IFN

EPIC is a trademark of Texas Instruments Incorporated.

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 1992, Texas Instruments Incorporated

description (continued)

The EP330 output-logic macrocell allows the user to configure output and feedback paths for combinational or registered operation either active high or active low. With propagation delays of 12 and15 ns, the EP330 may be configured as a low-power substitute for popular fast PLD devices such as the PAL16XXB series or the 'PAL16XX-12 and 'PAL16XX-15 series.

The CMOS EPROM technology makes it possible for the EP330 to operate at an active power-consumption level that is less than 75% of equivalent bipolar devices without sacrificing speed performance. This technology also facilitates 100% generic wafer testability using the UV-light erasable capability. As a result, designs and design modification can be quickly effected with a given EP330 without the need for post-programming testing.

Programming the EP330 is made easy by the availability of extensive third-party support for design entry, design processing, and device programming.

The EP330C is characterized for operation from 0°C to 70°C. The EP330I is characterized for operation from −40°C to 85°C.

functional description

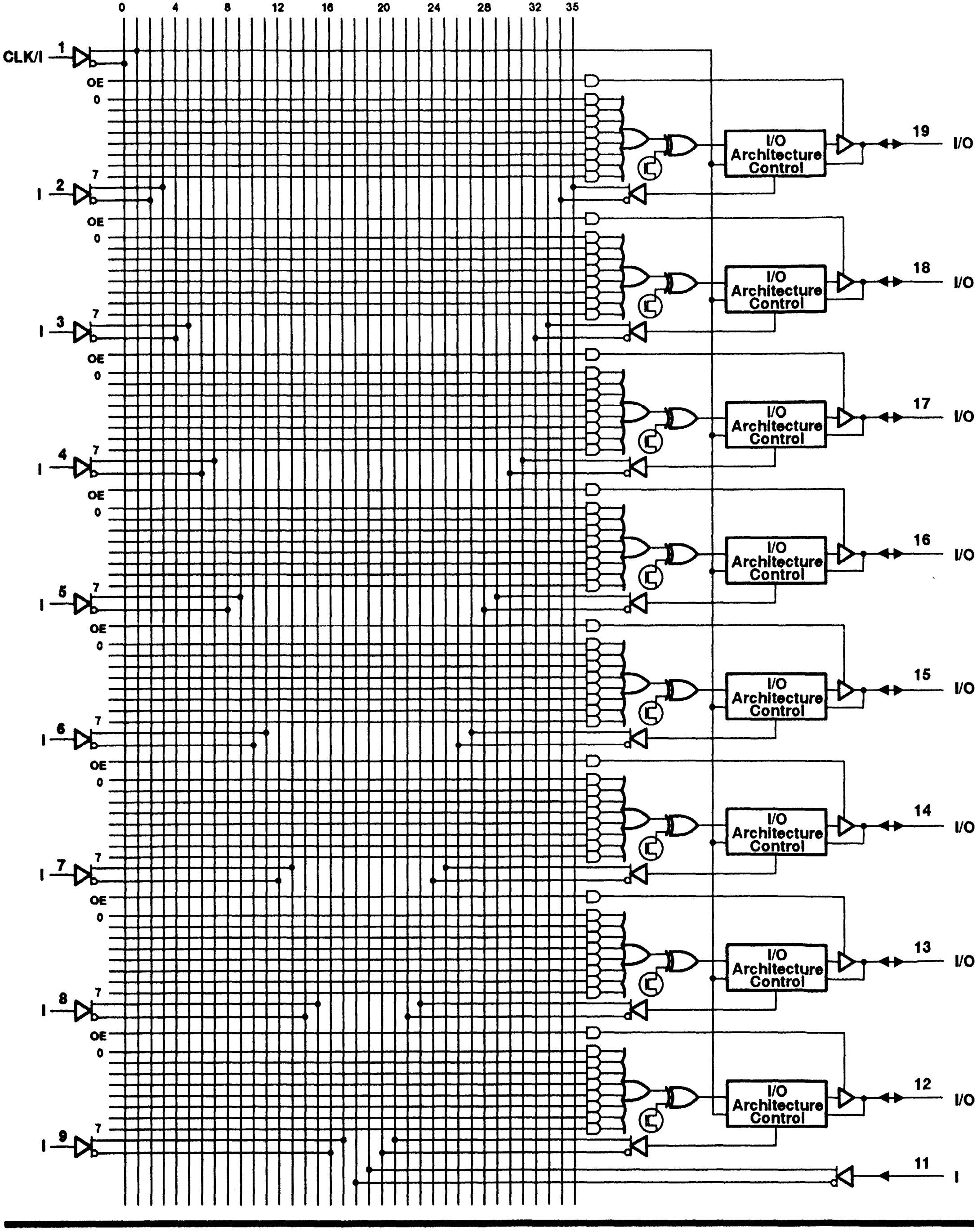
Externally, the EP330 provides ten dedicated inputs (one of which may be used as a synchronous clock input) and eight I/O pins that may be configured for input, output, or bidirectional operation.

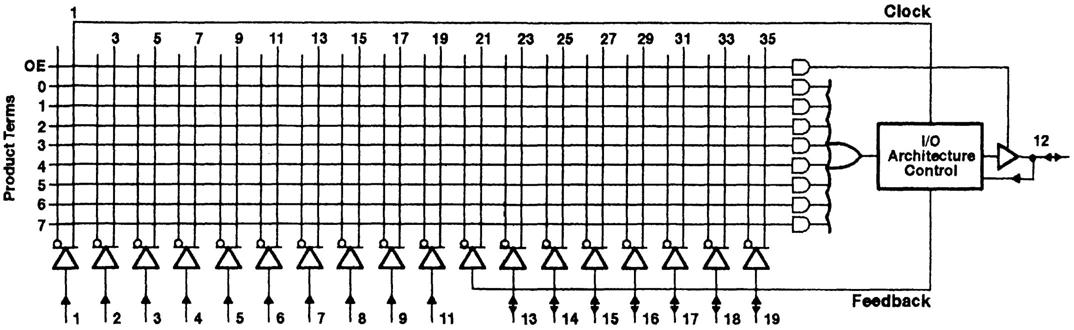
The logic diagram shows the complete EP330, while Figure 1 shows the basic EP330 macrocell. The internal architecture is organized with the familiar sum of products (AND-OR) structure. Inputs to the programmable AND array (shown running vertically in Figure 1) come from two sources: first, the true and complement of the ten dedicated input pins and second, the true and complement of the eight feedback signals, each one originating from an I/O architecture-control block. The 36-input AND array encompasses a total of 72 product terms distributed equally among the eight macrocells. Each product term (shown running horizontally in the logic diagram) represents a 36-input AND gate.

As shown in the logic diagram, the outputs of eight product terms are ORed together, then the output of the OR gate is sent as an input to an exclusive-OR gate. The purpose of this exclusive-OR gate is to allow the user to specify the polarity of the output signal by using the invert-select EPROM cell (active high if the EPROM cell is programmed and active low if it is not programmed).

The exclusive-OR output then feeds the I/O architecture control block. The control block configures the output for registered or combinational operation. In the registered configuration, the output is registered via a positive edge-triggered D-type flip-flop. In this condition, the feedback signal going to the array is also registered and comes directly from the output of the D-type flip-flop. In the combinational configuration, the output is nonregistered and the feedback signal comes directly from the I/O pin. In the erased state, the EP330 contains the same architectural characteristics as the 'PAL16L8.

logic diagram (positive logic)





NOTES: A. This diagram shows one of the eight macrocells within the EP330.
B. The double-arrow lines (↕) show I/O feedback from a macrocell.

Figure 1. Logic Array Macrocell

output-enable product term

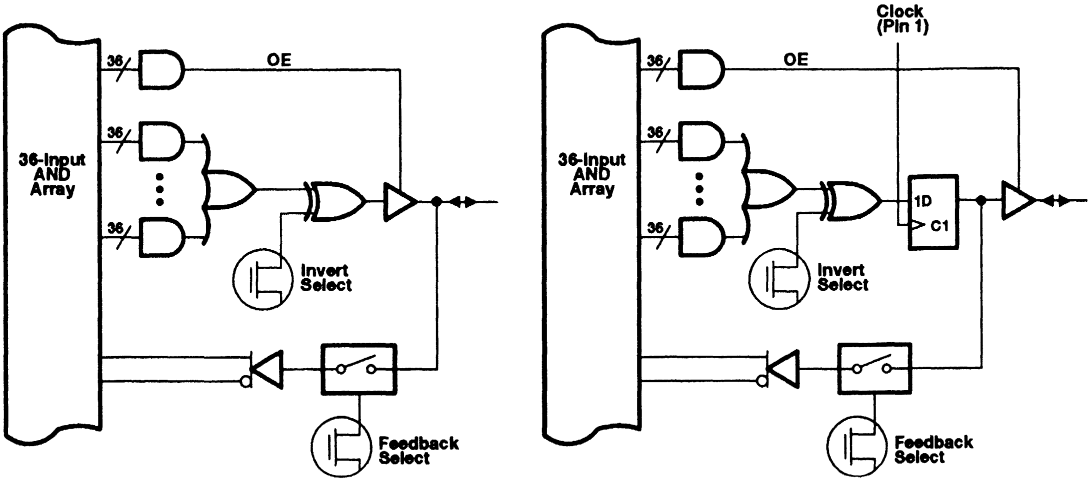
The output enable (OE) product term determines whether an output signal is allowed to propagate to the output pin. If the output of the OE product term is low, then the output buffer becomes a high-impedance node, thus inhibiting the output signal from reaching the output pin. For combinational configurations, this OE product term can be used to allow for true bidirectional operation.

The EP330 contains eight separate OE product terms, one per I/O pin. If it is desired that all outputs be enabled or disabled simultaneously, use an identically programmed product term at each of the outputs. If different outputs are to be enabled under different conditions, different OE product terms for each specific output may be defined.

I/O architecture

Figure 2 shows the different output configurations that can be chosen for any of the eight I/O pins on the EP330. Because of the individuality of each I/O architecture control block, both registered and combinational output can be chosen on a given EP330 device.

In the combinational configuration, either active-high or active-low output polarity can be chosen. Pin feedback or no feedback is also optional. In the registered configuration, the user has control over output polarity and may choose to use the internal feedback path or no feedback. Any I/O pin can be configured as a dedicated input by choosing no output and no feedback from the array. In the erased state, the I/O architecture is configured for a combinational active-low output with pin feedback.



OUTPUT/POLARITY	FEEDBACK
Combinational/High	Pin, None
Combinational/Low	Pin, None
None	Pin

OUTPUT/POLARITY	FEEDBACK
D Register/High	D Register, None
D Register/Low	D Register, None
None	D Register

(a) COMBINATIONAL CONFIGURATION

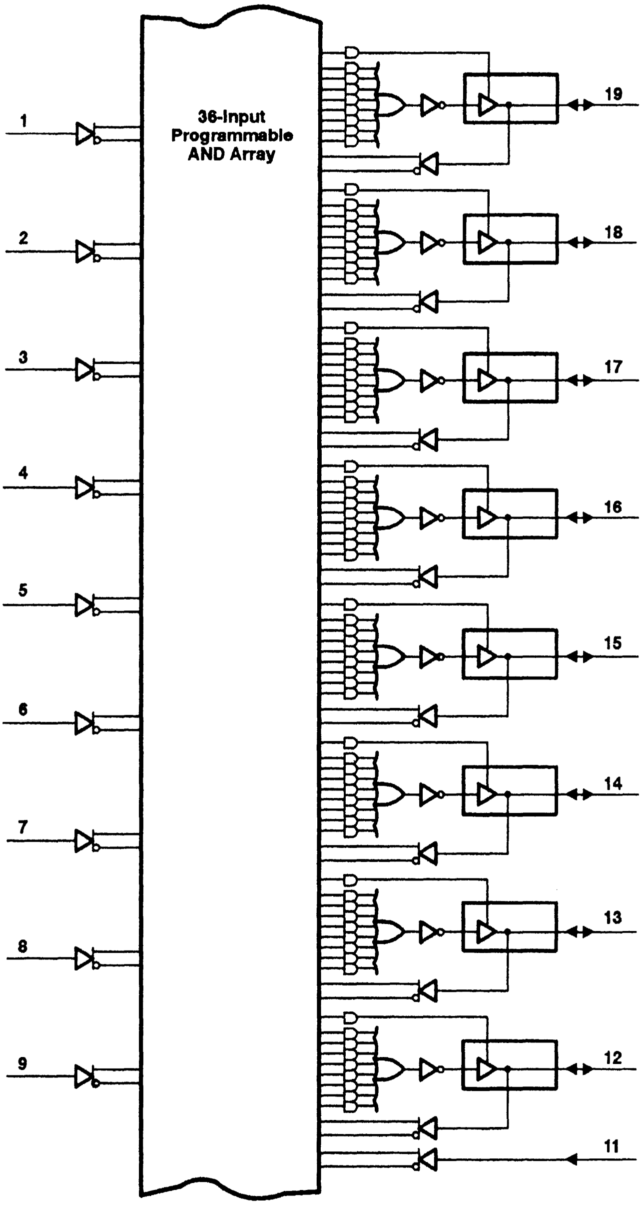
(b) REGISTERED CONFIGURATION

Figure 2. I/O Configurations

PLD compatibility

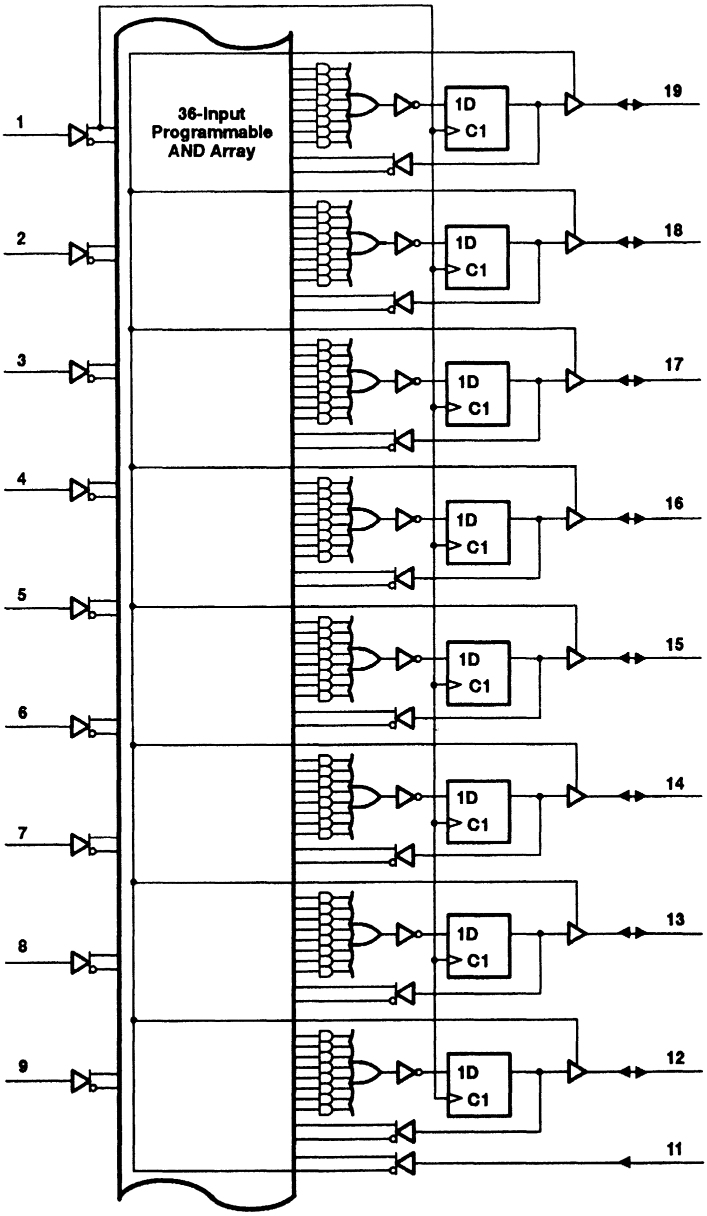
Figures 2(a) and 2(b) show how an EP330 can be configured as a drop-in replacement for two commonly used members of the 20-pin PLD family: the 'PAL16L8 and the 'PAL16R8. When configured in these manners, the EP330 is both a functional replacement, as well as a pin-to-pin replacement, for the 'PAL16L8 and 'PAL16R8.

Tables 1 and 2 provide additional information concerning the EP330 as a replacement for the 20-pin PLD family of devices.



- Invert Select EPROM cell is in the erased state providing active-low outputs.
- Combinational Mode is chosen providing Combinational Output with Input (Pin) Feedback.
- 8-product-term OR gate compared to 7-product-term OR gate on ’PAL16L8.
- Pin feedback to the array at 12 through 19 is not available in ’PAL16L8.

Figure 3. EP330 Configuration for Replacing a ’PAL16L8



- Invert Select EPROM cell is in the erased state providing active-low outputs.
- Registered Mode is chosen providing Registered Output with Registered Feedback.
- Complement of pin 11 is used as common OE term for all eight output pins.

Figure 4. EP330 Configuration for Replacing a ’PAL16R8

Table 1. Configurations for 20-Pin PLD Replacement

PLD PART NUMBER	EP330 PIN NUMBER	EP330 MACROCELL NUMBER	I/O CONFIGURATION MODE	OUTPUT/ POLARITY	FEEDBACK
10H8	12-19	1-8	Combinational	Comb/High	None
10L8	12-19	1-8	Combinational	Comb/Low	None
12H6	12	8	Combinational	None	Pin
	13-18	2-7	Combinational	Comb/High	None
	19	1	Combinational	None	Pin
12L6	12	8	Combinational	None	Pin
	13-18	2-7	Combinational	Comb/Low	None
	19	1	Combinational	None	Pin
14H4	12-13	7-8	Combinational	None	Pin
	14-17	3-6	Combinational	Comb/High	None
	18-19	1-2	Combinational	None	Pin
14L4	12-13	7-8	Combinational	None	Pin
	14-17	3-6	Combinational	Comb/Low	None
	18-19	1-2	Combinational	None	Pin
16C1	12-14	6-8	Combinational	None	Pin
	15	5	Combinational	Comb/Low	None
	16	4	Combinational	Comb/High	None
	17-19	1-3	Combinational	None	Pin
16H2	12-14	6-8	Combinational	None	Pin
	15-16	4-5	Combinational	Comb/High	None
	17-19	1-3	Combinational	None	Pin
16L2	12-14	6-8	Combinational	None	Pin
	15-16	4-5	Combinational	Comb/Low	None
	17-19	1-3	Combinational	None	Pin
16H8 & 16HD8	12	8	Combinational	Comb/High/Z	None
	13-18	2-7	Combinational	Comb/High/Z	Comb
	19	1	Combinational	Comb/High/Z	None
16L8 & 16LD8	12	8	Combinational	Comb/Low/Z	None
	13-18	2-7	Combinational	Comb/Low/Z	Comb
	19	1	Combinational	Comb/Low/Z	None
16R4	12-13	7-8	Combinational	Comb/Low/Z	Comb
	14-17	3-6	Registered	Reg/Low/Z	Reg
	18-19	1-2	Combinational	Comb/Low/Z	Comb
16R6	12	8	Combinational	Comb/Low/Z	Comb
	13-18	2-7	Registered	Reg/Low/Z	Reg
	19	1	Combinational	Comb/Low/Z	Comb
16R8	12-19	1-8	Registered	Reg/Low/Z	Reg
16P8	12	8	Combinational	Comb/Option/Z	None
	13-18	2-7	Combinational	Comb/Option/Z	Comb
	19	1	Combinational	Comb/Option/Z	None
16RP4	12-13	7-8	Combinational	Comb/Option/Z	Comb
	14-17	3-6	Registered	Reg/Option/Z	Reg
	18-19	1-2	Combinational	Comb/Option/Z	Comb
16RP6	12	8	Combinational	Comb/Option/Z	Comb
	13-18	2-7	Registered	Re/Option/Z	Reg
	19	1	Combinational	Comb/Option/Z	Comb
16RP8	12-19	1-8	Registered	Reg/Option/Z	Reg

Table 2. Device Specifications[†]

SYMBOL	PARAMETER	HIGH-SPEED EPLD		HIGH-SPEED PLD SERIES '16XXB/-15	
		EP330-12C	EP330-15C	'PAL16L8B/-15	'PAL16R8B/-15
I_{CC}	Supply current active	75 mA	75 mA	180 mA	180 mA
t_{pd}	Input to nonregistered output	12 ns	15 ns	15 ns	N/A
t_{CO1}	Clock to output delay	8 ns	10 ns	N/A	12 ns
t_{su}	Input setup time	6 ns	8 ns	N/A	15 ns
f_{max}	Max frequency	125 MHz	100 MHz	N/A	37 MHz

[†] Over commercial temperature range

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1)	−0.3 V to 7 V
Instantaneous supply voltage range, V_{CC} ($t \leq 20$ ns)	−2 V to 7 V
Programming supply voltage range, V_{PP}	−0.3 V to 14 V
Instantaneous programming supply voltage range, V_{PP} ($t \leq 20$ ns)	−2 V to 14 V
Input voltage range, V_I	−0.3 V to 7 V
Instantaneous input voltage range, V_I ($t \leq 20$ ns)	−2 V to 7 V
V_{CC} or GND current range	−160 mA to 160 mA
Operating free-air temperature range, T_A	−65°C to 135°C
Storage temperature range	−65°C to 150°C

NOTE 1: All voltage values are with respect to GND terminal.

recommended operating conditions

		EP330-12C		EP330-15C		UNIT
		MIN	**MAX**	**MIN**	**MAX**	
V_{CC}	Supply voltage	4.75	5.25	4.75	5.25	V
V_I	Input voltage	0	V_{CC}	0	V_{CC}	V
V_{IH}	High-level input voltage	2	V_{CC}+0.3	2	V_{CC}+0.3	V
V_{IL}	Low-level input voltage (see Note 2)	−0.3	0.8	−0.3	0.8	V
V_O	Output voltage	0	V_{CC}	0	V_{CC}	V
t_w	Pulse duration, CLK high or low	4		5		ns
t_{su}	Setup time, input	6		8		ns
t_h	Hold time, input	0		0		ns
t_r	Rise time, input		20		20	ns
t_f	Fall time, input		20		20	ns
T_A	Operating free-air temperature	0	70	0	70	°C

NOTE 2: The algebraic convention, in which the more negative value is designated minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended ranges of supply voltage and free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	EP330-12C EP330-15C			UNIT
			MIN	**TYP**†	**MAX**	
V_{OH}	High-level output voltage	V_{CC} = 4.75 V, I_{OH} = −12 mA	2.4			V
V_{OL}	Low-level output voltage	V_{CC} = 4.75 V, I_{OL} = 24 mA			0.5	V
I_I	Input current	V_I = 5.25 V or GND			±10	µA
I_{OZ}	Off-state output current	V_{CC} = 5.25 V, V_O = V_{CC} or GND			±10	µA
I_{CC}	Supply current	f = 1 MHz, No load, Programmed as an 8-bit counter		45	75	mA
C_i‡	Input capacitance	V_{CC} = 5 V, V_I = 0, f = 1 MHz			10	pF
C_o	Output capacitance	V_{CC} = 5 V, V_O = 0, f = 1 MHz			15	pF
C_{clk}	Clock capacitance	V_{CC} = 5 V, V_{CLK} = 0, f = 1 MHz			10	pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The input capacitance at pin 11 is 20 pF maximum when used as a programming pin and with V_{PP} = 14 V.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figure 5)

PARAMETER[†]			EP330-12C		EP330-15C		UNIT
			MIN	MAX	MIN	MAX	
f_{max}[‡]	Maximum frequency	With no feedback	125		100		MHz
		With internal feedback	100		100		
		With external feedback	71.4		55.6		
t_{pd1}	Input to nonregistered output delay (see Note 3)			12		15	ns
t_{pd2}	I/O to nonregistered output delay (see Note 3)			13		16	ns
t_{io}	I/O input and buffer delay (see Note 3)			1		1	ns
t_{co}	Clock input to registered output delay (see Note 3)			8		10	ns
t_{PZX}	Output enable time (see Note 4)			12		15	ns
t_{PXZ}	Output disable time (see Note 4)			12		15	ns
t_{cnt}	Minimum clock period (internal)			10		12	ns

[†] Letter symbols for switching characteristics and timing requirements in this data sheet have been chosen for compatibility with those used in other documentation previously prepared by another supplier for similar products. Any similarity to symbols used on other TI data sheets or to those shown in glossaries in TI data books is coincidental. The meanings may not be the same.

[‡] f_{max} with no feedback $= \frac{1}{t_w \text{ high} + t_w \text{ low}}$, f_{max} with internal feedback $= \frac{1}{t_{cnt}}$,

f_{max} with external feedback $= \frac{1}{t_{su} + t_{co}}$.

f_{max} with internal feedback is programmed as an 8-bit counter.

NOTES: 3. This parameter is measured with only one output switching.
4. This is for an output voltage change of 500 mV.

PRODUCT PREVIEW

recommended operating conditions

		MIN	MAX	UNIT
V_{CC}	Supply voltage	4.5	5.5	V
V_I	Input voltage	0	V_{CC}	V
V_{IH}	High-level input voltage	2	V_{CC}+0.3	V
V_{IL}	Low-level input voltage (see Note 2)	−0.3	0.8	V
V_O	Output voltage	0	V_{CC}	V
t_w	Pulse duration, CLK high or low	12		ns
t_{su}	Setup time, input	15		ns
t_h	Hold time, input	0		ns
t_r	Rise time, input		20	ns
t_f	Fall time, input		20	ns
T_A	Operating free-air temperature	−40	85	°C

NOTE 2: The algebraic convention, in which the more negative value is designated minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended ranges of supply voltage and free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	V_{CC} = 4.5 V, I_{OH} = −12 mA	2.4			V
V_{OL}	Low-level output voltage	V_{CC} = 4.5 V, I_{OL} = 24 mA			0.5	V
I_I	Input current	V_I = 5.5 V or GND			±10	µA
I_{OZ}	Off-state output current	V_{CC} = 5.5 V, V_O = V_{CC} or GND			±10	µA
I_{CC}	Supply current	f = 1 MHz, No load, Programmed as an 8-bit counter		45	75	mA
C_i	Input capacitance	V_{CC} = 5 V, V_I = 2 V, f = 1 MHz			10	pF
C_o	Output capacitance	V_{CC} = 5 V, V_O = 2 V, f = 1 MHz			15	pF
C_{clk}	Clock capacitance	V_{CC} = 5 V, V_{CLK} = 2 V, f = 1 MHz			10	pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (see Figure 5)

PARAMETER‡			MIN	MAX	UNIT
f_{max}§	Maximum frequency	With no feedback	41.6		MHz
		With internal feedback	41.6		
		With external feedback	28.5		
t_{pd1}	Input to nonregistered output delay (see Note 3)			25	ns
t_{pd2}	I/O to nonregistered output delay (see Note 3)			26	ns
t_{io}	I/O input and buffer delay (see Note 3)			1	ns
t_{co}	Clock input to registered output delay (see Note 3)			15	ns
t_{PZX}	Output enable time (see Note 4)			25	ns
t_{PXZ}	Output disable time (see Note 4)			25	ns
t_{cnt}	Minimum clock period (internal)			24	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ Letter symbols for switching characteristics and timing requirements in this data sheet have been chosen for compatibility with those used in other documentation previously prepared by another supplier for similar products. Any similarity to symbols used on other TI data sheets or to those shown in glossaries in TI data books is coincidental. The meanings may not be the same.

§ f_{max} with no feedback $= \dfrac{1}{t_w \text{ high} + t_w \text{ low}}$, f_{max} with internal feedback $= \dfrac{1}{t_{cnt}}$,

f_{max} with external feedback $= \dfrac{1}{t_{su} + t_{co}}$.

f_{max} with internal feedback is programmed as an 8-bit counter.

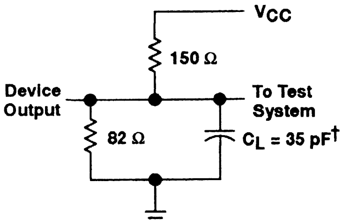
NOTES: 3. This parameter is measured with only one output switching.
4. This is for an output voltage change of 500 mV.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

PARAMETER MEASUREMENT INFORMATION

functional testing

The EP330 is functionally tested through complete testing of each programmable EPROM bit and all internal logic elements, thus ensuring 100% programming yield.



† Includes probe and circuit capacitance. Equivalent loads may be used for testing.

Figure 5. Dynamic Test Circuit

design security

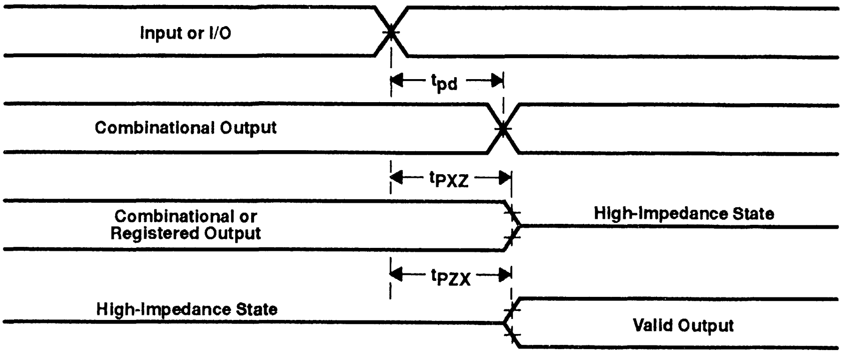
The EP330 contains a programmable design-security feature that controls the access to the data programmed into the device. If this programmable feature is used, a proprietary design implemented in the device cannot be copied or retrieved. Therefore, a very high level of design control is achieved since programmed data within EPROM cells is invisible. The bit that controls this function, along with all other program data, may be reset by erasing the cells in the device.

latch-up

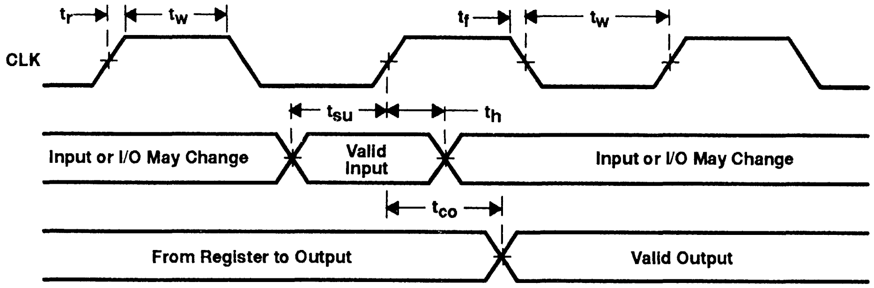
The EP330 input, I/O, and clock pins have been carefully designed to resist the latch-up that is inherent in CMOS structures. The EP330 pins will not latch up for input voltages between −1 V and V_{CC} + 1 V with currents up to 250 mA. During transitions, the inputs may undershoot to −2 V for periods of less than 20 ns.

Although the programming pin (pin 11) is designed to resist latch-up to the 13.5-V limit, during positive-current latch-up testing, the verify mode (pin 1) and program mode (pin 11) can be inadvertently entered into, causing current flow in the pins. This should not be construed as latch-up.

PARAMETER MEASUREMENT INFORMATION



(a) COMBINATIONAL MODE



(b) SYNCHRONOUS CLOCK MODE

NOTES: A. Rise time (t_r) and fall time (t_f) < 3 ns

B. t_w is measured at 0.3 V and 2.7 V. All other timing is measured at 1.5 V, except t_{PZX} and t_{PXZ} which are measured for an output voltage change of 500 mV.

C. Input voltage levels at 0 V and 3 V

Figure 6. Voltage Waveforms

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
FREQUENCY

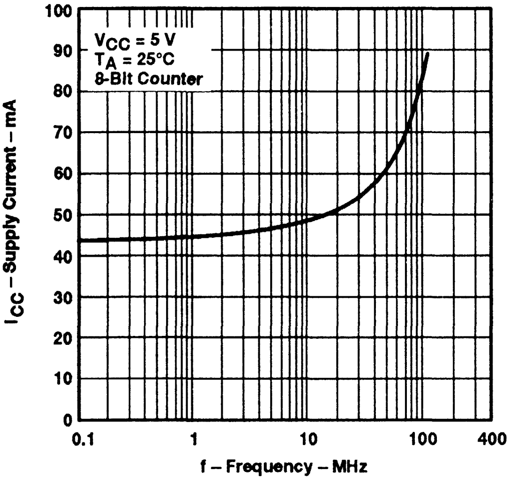


Figure 7

CHANGE IN PROPAGATION DELAY TIME
vs
LOAD CAPACITANCE

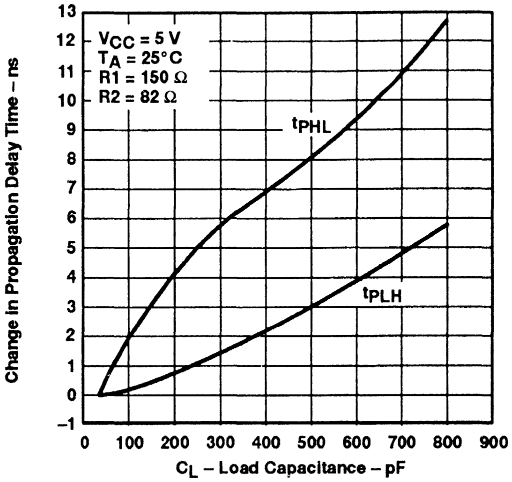


Figure 8

CHANGE IN PROPAGATION DELAY TIME
vs
NUMBER OF OUTPUTS SWITCHING

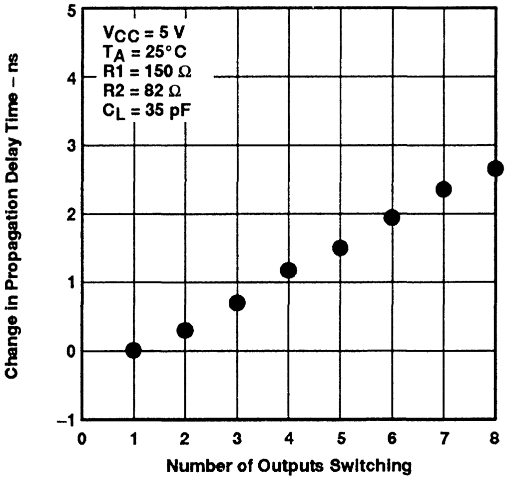


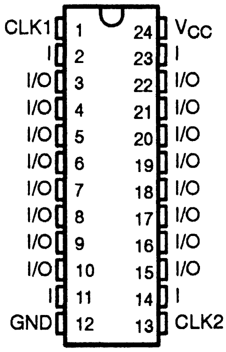
Figure 9

EP630 SERIES
HIGH-PERFORMANCE 16-MACROCELL ONE-TIME PROGRAMMABLE LOGIC DEVICES

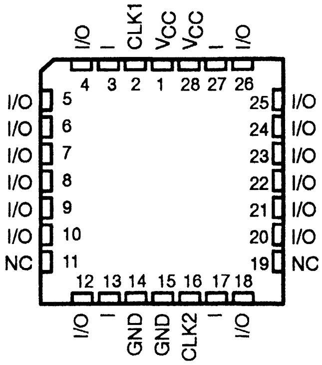
SRES001B – D3357, OCTOBER 1989 – REVISED MARCH 1992

- **Programmable Replacement for Conventional TTL and 74HC Devices**
- **Virtually Zero Standby Current**
  Typ 20 μA
- **Low Operating Current:**
  I_{CC} max (turbo bit on) . . . 90 mA
  I_{CC} max (turbo bit off) . . . 10 mA
- **High Performance CMOS Process Allows:**
  Maximum t_{pd}: - 15C . . . 15 ns
  - 20C . . . 20ns
  - 25I . . . 25 ns
- **Asynchronous Clocking of All Registers or Banked Register Operation From 2 Synchronous Clocks**
- **Sixteen Macrocells With Configurable I/O Architecture Allowing for up to 20 Inputs and 16 Outputs**
- **User-Programmable Output Logic Macrocells Provide Flexibility in Output Types with:**
  - **Selectable for Registered or Combinational Operation**
  - **Output Polarity Control**
  - **Independently User Programmable Feedback Path**
- **Programmable Design Security Bit Prevents Copying of Logic Stored in Device**
- **Third-Party Advanced Software Support Featuring Schematic Capture, Interactive Netlist, Boolean Equations, and State Machine Design Entry**

NT PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



NC – No internal connection

AVAILABLE OPTIONS

T_A RANGE	PACKAGE TYPE	
	PLASTIC DUAL-IN-LINE PACKAGE (PDIP)	PLASTIC CHIP CARRIER PACKAGE (PLCC)
0°C to 70°C	EP630-15CNT	EP630-15CFN
	EP630-20CNT	EP630-20CFN
−40°C to 85°C	EP630-25INT	EP630-25IFN

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 1992, Texas Instruments Incorporated

TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

description

general

The Texas Instruments EP630 is capable of implementing over 600 equivalent gates of SSI and MSI logic functions all in plastic and ceramic space-saving 24-pin, 300-mil dual-in-line (DIP) packages and 28-pin chip-carrier packages. It uses the familiar sum-of-products logic, providing a programmable AND with a fixed OR structure. The device accommodates both combinational and sequential (registered) logic functions with up to 20 inputs and 16 outputs. The EP630 has a user programmable output logic macrocell that allows each output to be configured as a combinational or registered output and feedback signals active high or active low.

A unique feature of the EP630 is the ability to program D, T, SR, or JK flip-flop operation individually for each output without sacrificing product terms. In addition, each register can be individually clocked from any of the input or feedback paths available in the AND array. These features allow a variety of logic functions to be simultaneously implemented.

The CMOS EPROM technology reduces the power consumption to less than 55% of equivalent bipolar devices without sacrificing speed performance. Erasable EPROM bits allow for enhanced factory testing.

Programming the EP630 is made easy by the availability of extensive third-party support for design entry, design processing and device programming.

The EP630-15C and EP630-20C devices are characterized for operation from 0°C to 70°C. The EP630-25I is characterized for operation from −40°C to 85°C.

functional

The EP630 uses a CMOS EPROM technology to implement logic designs in a programmable AND logic array. The device contains a revolutionary programmable I/O architecture that provides advanced functional capability for user programmable logic.

Externally, the EP630 provides 4 dedicated data inputs and 16 I/O pins, which may be configured for input, output, or bidirectional operation. Figure 1 shows the EP630 basic logic array macrocell. The internal architecture is organized with familiar sum-of-products (AND-OR) structure. Inputs to the programmable AND array come from true and complement signals from the 4 dedicated data inputs and the 16 I/O architecture-control blocks. The 40-input AND array encompasses 160 product terms, which are distributed among 16 available macrocells. Each EP630 product term represents a 40-input AND gate.

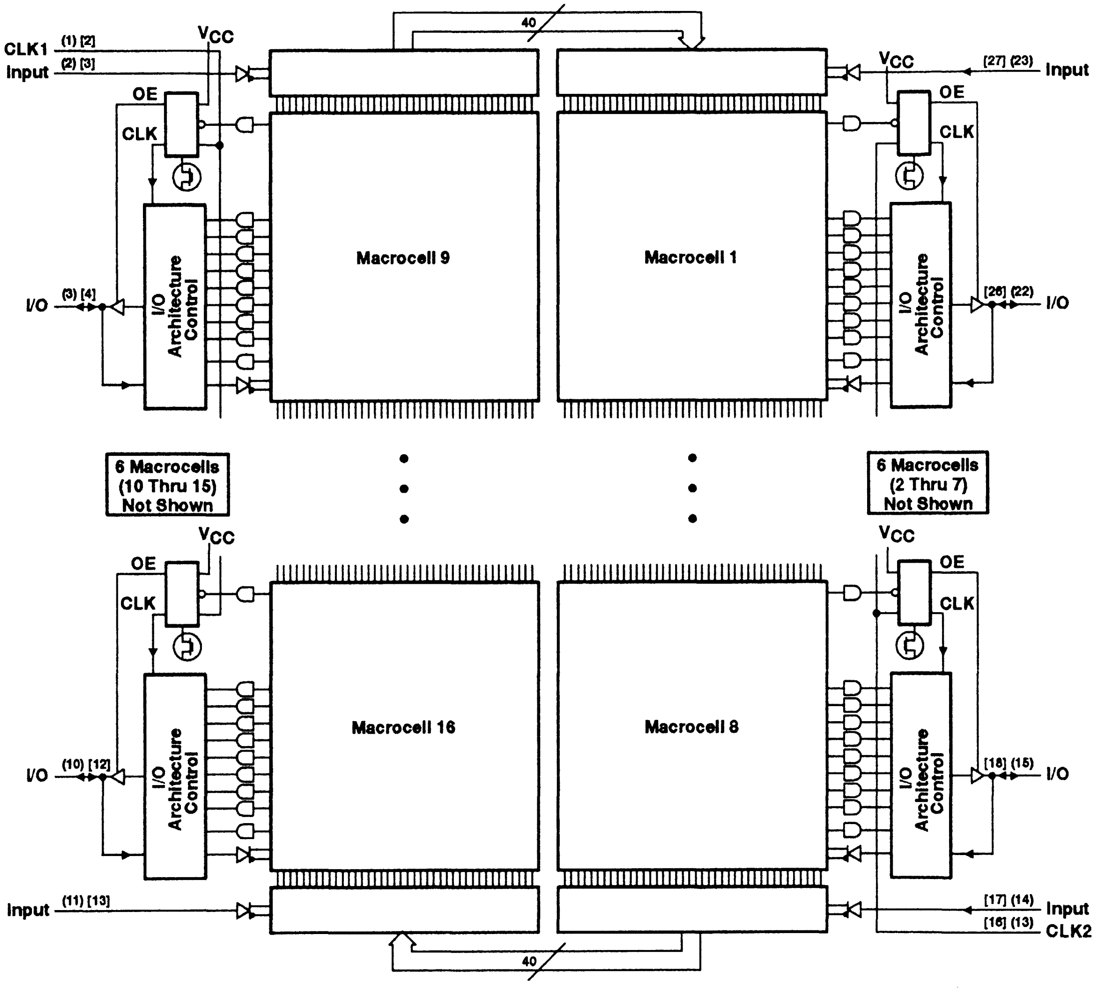
Each macrocell contains 10 product terms, 8 of which are dedicated for logic implementation. One product term is used for clear control of the macrocell internal register. The remaining product term is used for output enable/asynchronous clock implementation.

There is an EPROM connection at the intersection point of each input signal and each product term. In the erased state, all connections are made. This means both the true and complement forms of all inputs are connected to each product term. Connections are opened during the programming process. Therefore, any product term may be connected to the true or complement form of any array input signal.

When both the true and complement forms of any signal are left intact, a logical false state results on the output of the AND gate. If both the true and complement connections are open, then a logical "don't care" applies for that input. If all inputs for the product term are programmed open, then a logical true state results on the output of the AND gate.

Two dedicated clock inputs provide synchronous clock signals to the EP630 internal registers. Each of the clock signals controls a bank of 8 registers. CLK1 controls registers associated with macrocells 9-16, and CLK2 controls registers associated with macrocells 1-8. The EP630 advanced I/O architecture allows the number of synchronous registers to be user defined, from one to sixteen. Both dedicated clock inputs are positive-edge-triggered.

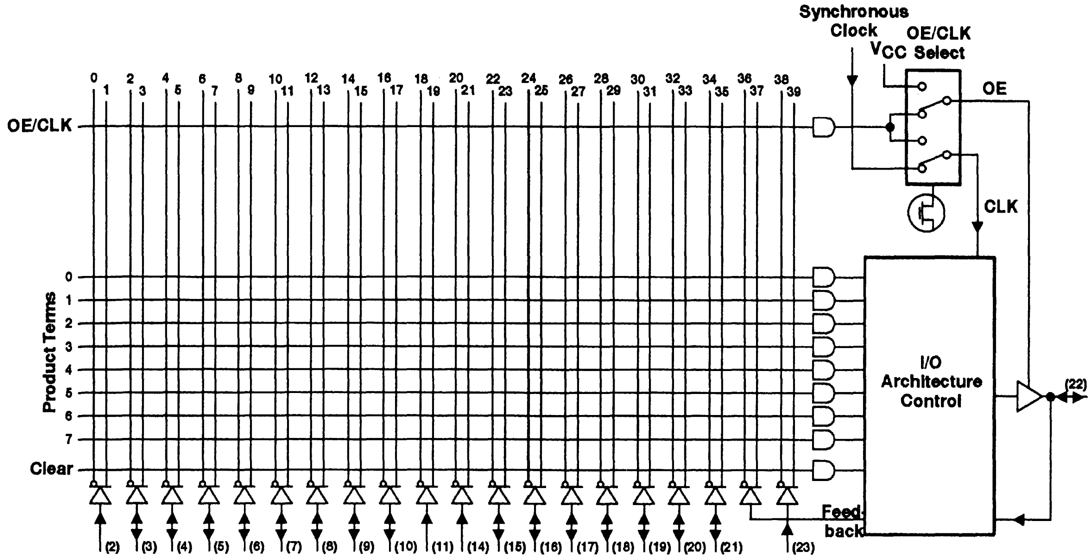
functional block diagram



Pin numbers in ( ) are for DIP packages; pin numbers in [ ] are for the chip-carrier package.

I/O architecture

The EP630 input/output architecture provides each macrocell with over 50 possible I/O configurations. Each I/O can be configured for combinational or registered output, with programmable output polarity. Four different types of registers (D, T, JK, and SR) can be implemented into every I/O without any additional logic requirements. I/O feedback selection can also be programmed for registered or input (pin) feedback. Another benefit of the EP630 I/O architecture is its ability to individually clock each internal register from asynchronous clock signals.



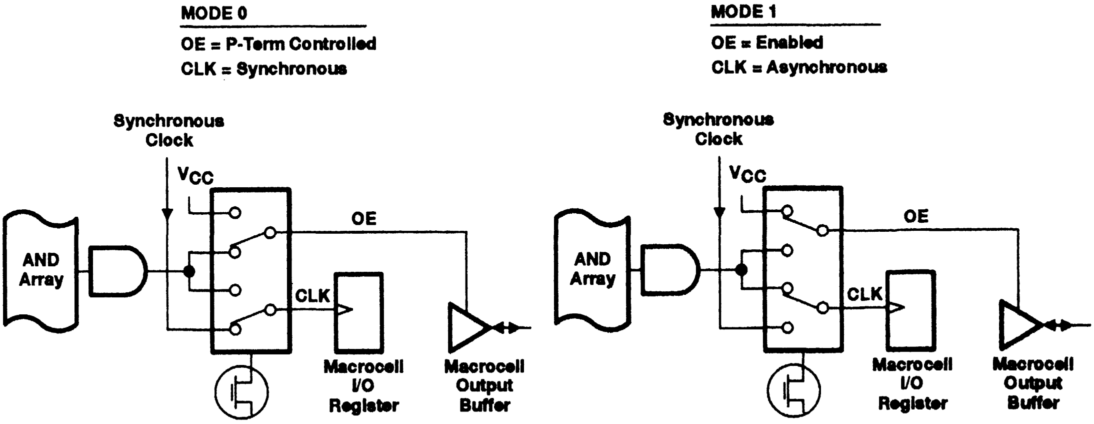
Pin numbers are for the NT package.

Figure 1. Logic Array Macrocell (Macrocell 1 Illustrated)

OE/CLK selection

Figure 2 shows the two modes of operation that are provided by the OE/CLK select multiplexer. The operation of this multiplexer is controlled by a single EPROM bit and may be individually configured for each EP630 I/O pin. In Mode 0, the 3-state output buffer is controlled by a single product term. If the output of the AND gate is true, the output buffer is enabled. If the output of the AND gate is false, the output buffer is in the high-impedance state. In this mode, the macrocell flip-flop may be clocked by its respective synchronous clock input. After erasure, the OE/CLK select multiplexer is configured in Mode 0.

In Mode 1, the output-enable buffer is always enabled. The macrocell flip-flop may now be triggered from an asynchronous clock signal generated by the OE/CLK multiplexable product term. This mode allows individual clocking of flip-flops from any available signal in the AND array. Because both true and complement signals reside in the AND array, the flip-flop may be configured for positive- or negative-edge-triggered operation. With the clock now controlled by a product term, gated clock structures are also possible.



MODE 0

OE = P-Term Controlled
CLK = Synchronous

MODE 1

OE = Enabled
CLK = Asynchronous

The register is clocked by the synchronous clock signal, which is common to seven other Macrocells. The output is enabled by the logic from the product term.

The output is permanently enabled and the register is clocked via the product term. This allows for gated clocks that may be generated from elsewhere in the EP630.

Figure 2. OE/CLK Select Multiplexer

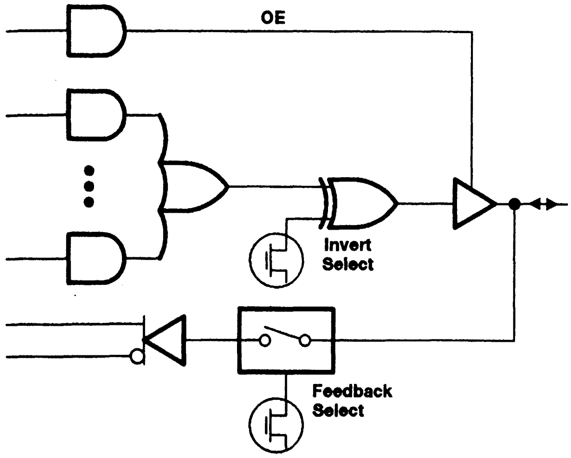
output/feedback selection

Figure 3 shows the EP630 basic output configurations. Along with combinational output, four register types are available. Each macrocell I/O may be independently configured. All registers have individual asynchronous clear control from a dedicated product term. When the product term is asserted, the macrocell register will immediately be loaded with a zero independent of the clock. On power-up, The EP630 performs the clear function automatically.

When the D or T register is selected, eight product terms are ORed together and made available to the register input. The invert select EPROM bit determines output polarity. The feedback-select multiplexer enables register, I/O (pin), or no feedback to the AND array.

If the JK or SR registers are selected, the eight product terms are shared between two OR gates. The invert select EPROM bit configures output polarity. The feedback-select multiplexer enables registered or no feedback to the AND array.

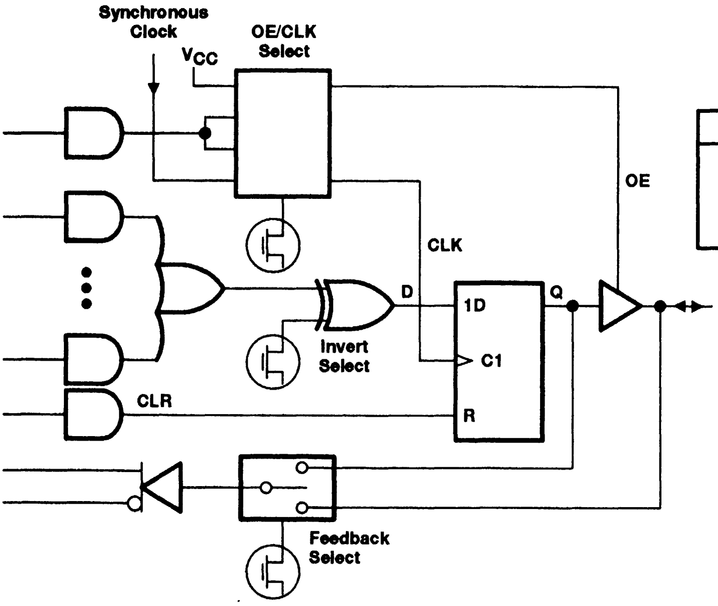
Any I/O pin may be configured as a dedicated input by selecting no output and pin feedback. No output is obtained by disabling the macrocell output buffer. In the erased state, each I/O is configured for combinational active-low output with input (pin) feedback.



I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
Combinational/high	Pin, None
Combinational/low	Pin, None
None	Pin

(a) COMBINATIONAL



I/O SELECTION

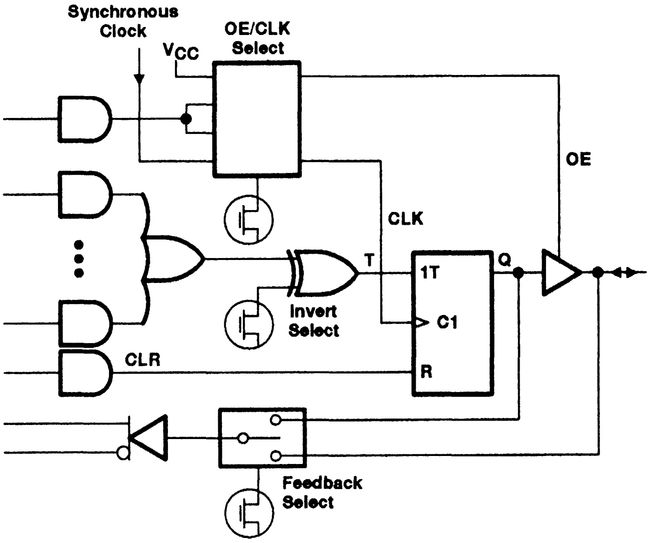
OUTPUT/POLARITY	FEEDBACK
D Register/high	D Register, Pin, None
D Register/low	D Register, Pin, None
None	D Register
None	Pin

FUNCTION TABLE

INPUTS			OUTPUT
CLR	CLK	D	Q
L	↑	L	L
L	↑	H	H
L	L	X	Q_0
H	X	X	L

(b) D-TYPE FLIP-FLOP

Figure 3. I/O Configurations



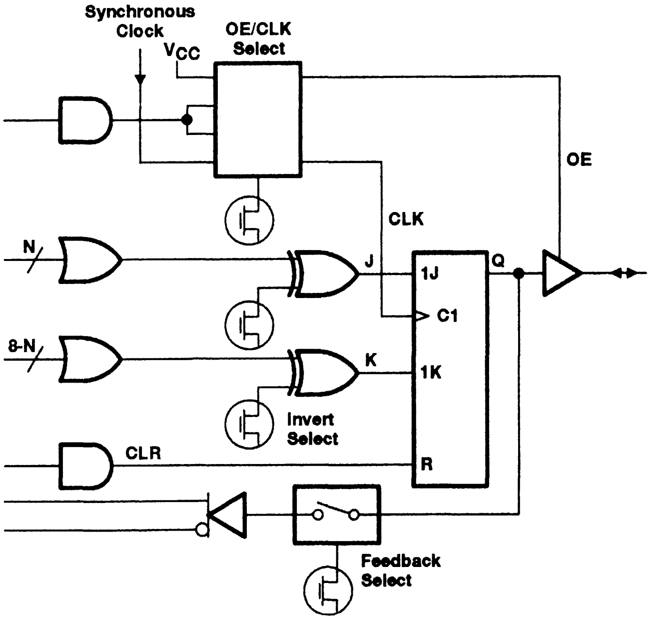
I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
T Register/high	T Register, Pin, None
T Register/low	T Register, Pin, None
None	T Register
None	Pin

FUNCTION TABLE

INPUTS			OUTPUT
CLR	CLK	T	Q
L	↑	L	Q_0
L	↑	H	$\overline{Q}_0$
L	L	X	Q_0
H	X	X	L

(c) TOGGLE FLIP-FLOP



I/O SELECTION

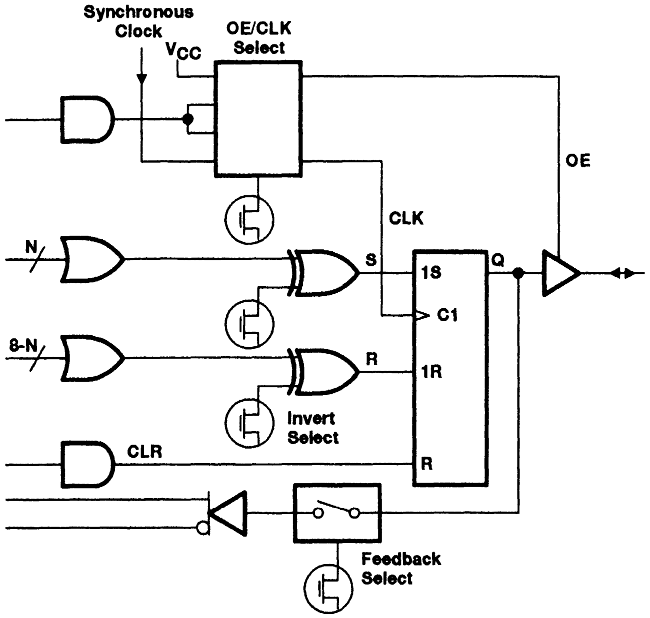
OUTPUT/POLARITY	FEEDBACK
JK Register/high	JK Register, None
JK Register/low	JK Register, None
None	JK Register

FUNCTION TABLE

INPUTS				OUTPUT
CLR	CLK	J	K	Q
L	↑	L	L	Q_0
L	↑	L	H	L
L	↑	H	L	H
L	↑	H	H	$\overline{Q}_0$
L	L	X	X	Q_0
H	X	X	X	L

(d) J-K FLIP-FLOP

Figure 3. I/O Configurations (Continued)



I/O SELECTION

OUTPUT/POLARITY	FEEDBACK
SR Register/high	SR Register, None
SR Register/low	SR Register, None
None	SR Register

FUNCTION TABLE

INPUTS				OUTPUT
CLR	CLK	S	R	Q
L	↑	L	L	Q_0
L	↑	L	H	L
L	↑	H	L	H
L	↑	H	H	Undefined
L	L	X	X	Q_0
H	X	X	X	L

(e) S-R FLIP-FLOP

Figure 3. I/O Configurations (Continued)

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1)	−0.3 V to 7 V
Instantaneous supply voltage range, V_{CC} ($t \leq 20$ ns)	−2 V to 7 V
Programming supply voltage range, V_{pp}	−0.3 V to 14 V
Instantaneous programming supply voltage range, V_{pp} ($t \leq 20$ ns)	−2 V to 14 V
Input voltage range, V_I	−0.3 V to 7 V
Instantaneous input voltage range, V_I ($t \leq 20$ ns)	−2 V to 7 V
V_{CC} or GND current range	−175 mA to 175 mA
Operating free-air temperature range, T_A	−65°C to 135°C
Storage temperature range	−65°C to 150°C

NOTE 1: All voltage values are with respect to GND terminal.

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		4.75	5.25	V
V_I	Input voltage		0	V_{CC}	V
V_{IH}	High-level input voltage		2	V_{CC}+0.3	V
V_{IL}	Low-level input voltage (see Note 2)		−0.3	0.8	V
V_O	Output voltage		0	V_{CC}	V
t_r	Rise time	CLK input		20	ns
		Other inputs		40	
t_f	Fall time	CLK input		20	ns
		Other inputs		40	
T_A	Operating free-air temperature		0	70	°C

NOTE 2: The algebraic convention, in which the more negative value is designated minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIIONS		MIN	MAX	UNIT
V_{OH}	High-level output voltage	TTL	V_{CC} = 4.75 V,	I_{OH} = −4 mA	2.4		V
		CMOS	V_{CC} = 4.75 V,	I_{OH} = −2 mA	3.84		
V_{OL}	Low-level output voltage		V_{CC} = 4.75 V,	I_{OL} = 4 mA		0.45	V
I_I	Input current		V_{CC} = 5.25 V,	V_I = V_{CC} or GND		±10	µA
I_{OZ}	Off-state output current		V_{CC} = 5.25 V,	V_O = V_{CC} or GND		±10	µA
I_{CC}	Supply current	Standby	V_{CC} = 5.25 V, V_I = V_{CC} or GND, No load	See Note 3		150	µA
		Nonturbo		See Note 4		10	mA
		Turbo		See Note 4		90	
C_i	Input capacitance		V_I = 0, f = 1 MHz,	T_A = 25°C		10	pF
C_o	Output capacitance		V_O = 0, f = 1 MHz,	T_A = 25°C		12	pF
C_{clk}	Clock capacitance		V_I = 0, f = 1 MHz,	T_A = 25°C		20	pF

NOTES: 3. When in nonturbo, the device automatically goes into the standby mode approximately 100 ns after the last transition.

4. These parameters are measured with the device programmed as a 16-bit counter and f = 1 MHz.

switching characteristics over recommended ranges of supply voltage and operating free air temperature (unless otherwise noted)

combinational mode, turbo bit on

PARAMETER[†]		TEST CONDITIONS		EP630-15C		EP630-20C		UNIT
				MIN	MAX	MIN	MAX	
t_{pd1}	Input to nonregistered output delay	C_L = 35 pF			15		20	ns
t_{pd2}	I/O input to nonregistered output delay				17		22	ns
t_{PZX}	Output enable time	C_L = 35 pF	See Note 5		15		20	ns
t_{PXZ}	Output disable time	C_L = 5 pF			15		20	ns
t_{io}	I/O input buffer delay				2		2	ns

combinational mode, turbo bit off

PARAMETER[†]		TEST CONDITIONS		EP630-15C		EP630-20C		UNIT
				MIN	MAX	MIN	MAX	
t_{pd1}	Input to nonregistered output delay	C_L = 35 pF			35		40	ns
t_{pd2}	I/O input to nonregistered output delay				37		42	ns
t_{PZX}	Output enable time	C_L = 35 pF	See Note 5		35		40	ns
t_{PXZ}	Output disable time	C_L = 5 pF			35		40	ns
t_{io}	I/O input buffer delay				2		2	ns

synchronous clock mode, mode 0

PARAMETER[†]			TEST CONDITIONS	EP630-15C		EP630-20C		UNIT
				MIN	MAX	MIN	MAX	
f_{max}	Maximum frequency[‡]	No feedback		83.3		62.5		MHz
		Internal feedback		83.3		62.5		
		External feedback[§]		50		41.6		
t_{co1}	Clock to output delay time				11		13	ns
t_{cnt}	Minimum clock period (register feedback to register output)		See Note 6		12		16	ns
t_{clr}	Asynchronous output clear time	Turbo bit on	C_L = 35 pF		15		20	ns
		Turbo bit off			35		40	

[†] Letter symbols for switching characteristics and timing requirements in this data sheet have been chosen for compatibility with those used in other documentation previously prepared by another supplier for similar products. Any similarity to symbols used on other TI data sheets or to those shown in glossaries in TI data books is coincidental. The meanings may not be the same.

[‡] f_{max} with no feedback = $\dfrac{1}{t_{ch} + t_{cl}}$

f_{max} with internal feedback = $\dfrac{1}{t_{cnt}}$

f_{max} with external feedback = $\dfrac{1}{t_{su} + t_{co1}}$

f_{max} with internal feedback is programmed as a 16-bit counter.

[§] Use t_{su} and t_{co1} for a device programmed with the turbo bit on.

NOTES: 5. This is for an output voltage change of 500 mV.

6. These parameters are measured with device programmed as a 16-bit counter.

switching characteristics over recommended ranges of supply voltage and operating free air temperature (unless otherwise noted)

asynchronous clock mode, mode 1

PARAMETER[†]			TEST CONDITIONS	EP630-15C		EP630-20C		UNIT
				MIN	MAX	MIN	MAX	
f_{max}	Maximum frequency[‡]	No feedback		71.4		55.5		MHz
		Internal feedback		71.4		55.5		
		External feedback[§]		47.6		35.7		
t_{aco1}	Clock to output delay time	Turbo bit on			15		20	ns
		Turbo bit off			35		40	
t_{acnt}	Minimum clock period (register feedback to register output)				14		18	ns
t_{clr}	Asynchronous output clear time	Turbo bit on	$C_L = 35$ pF		15		20	ns
		Turbo bit off			35		40	

timing requirements over recommended ranges of supply voltage and free-air temperature

synchronous clock mode, mode 0

PARAMETER[†]			EP630-15C		EP630-20C		UNIT
			MIN	MAX	MIN	MAX	
t_{su}	Input setup time	Turbo bit on	9		11		ns
		Turbo bit off	29		31		
t_h	Input hold time		0		0		ns
t_{ch}	Clock high pulse duration		6		8		ns
t_{cl}	Clock low pulse duration		6		8		ns

asynchronous clock mode, mode 1

PARAMETER[†]			EP630-15C		EP630-20C		UNIT
			MIN	MAX	MIN	MAX	
t_{asu}	Input setup time	Turbo bit on	6		8		ns
		Turbo bit off	26		28		
t_{ah}	Input hold time		6		8		ns
t_{ach}	Clock high pulse duration		7		9		ns
t_{acl}	Clock low pulse duration		7		9		ns

[†] Letter symbols for switching characteristics and timing requirements in this data sheet have been chosen for compatibility with those used in other documentation previously prepared by another supplier for similar products. Any similarity to symbols used on other TI data sheets or to those shown in glossaries in TI data books is coincidental. The meanings may not be the same.

[‡] f_{max} with no feedback $= \dfrac{1}{t_{ach} + t_{acl}}$

f_{max} with internal feedback $= \dfrac{1}{t_{acnt}}$

f_{max} with external feedback $= \dfrac{1}{t_{asu} + t_{aco1}}$

f_{max} with internal feedback is programmed as a 16-bit counter.

[§] Use t_{su} and t_{co1} for a device programmed with the turbo bit on.

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		4.5	5.5	V
V_I	Input voltage		0	V_{CC}	V
V_{IH}	High-level input voltage		2	V_{CC}+0.3	V
V_{IL}	Low-level input voltage (see Note 2)		−0.3	0.8	V
V_O	Output voltage		0	V_{CC}	V
t_r	Rise time	CLK input		20	ns
		Other inputs		40	
t_f	Fall time	CLK input		20	ns
		Other inputs		40	
T_A	Operating free-air temperature		−40	85	°C

NOTE 2: The algebraic convention, in which the more negative value is designated minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		MIN	MAX	UNIT
V_{OH}	High-level output voltage	TTL	V_{CC} = 4.5 V,	I_{OH} = −4 mA	2.4		V
		CMOS	V_{CC} = 4.5 V,	I_{OH} = −2 mA	3.84		
V_{OL}	Low-level output voltage		V_{CC} = 4.5 V,	I_{OL} = 4 mA		0.45	V
I_I	Input current		V_{CC} = 5.5 V,	V_I = V_{CC} or GND		±10	µA
I_{OZ}	Off-state output current		V_{CC} = 5.5 V,	V_O = V_{CC} or GND		±10	µA
I_{CC}	Supply current	Standby	V_{CC} = 5.5 V, V_I = V_{CC} or GND, No load	See Note 3		150	µA
		Nonturbo		See Note 4		15	mA
		Turbo		See Note 4		150	
C_i	Input capacitance		V_I = 0, f = 1 MHz,	T_A = 25°C		10	pF
C_o	Output capacitance		V_O = 0, f = 1 MHz,	T_A = 25°C		12	pF
C_{clk}	Clock capacitance		V_I = 0, f = 1 MHz,	T_A = 25°C		20	pF

NOTES: 3. When in nonturbo, the device automatically goes into the standby mode approximately 100 ns after the last transition.
4. These parameters are measured with the device programmed as a 16-bit counter and f = 1 MHz.

switching characteristics over recommended ranges of supply voltage and operating free air temperature (unless otherwise noted)

combinational mode, turbo bit on

PARAMETER[†]		TEST CONDITIONS		MIN	MAX	UNIT
t_{pd1}	Input to nonregistered output delay	$C_L = 35$ pF			25	ns
t_{pd2}	I/O input to nonregistered output delay				27	ns
t_{PZX}	Output enable time	$C_L = 35$ pF	See Note 5		25	ns
t_{PXZ}	Output disable time	$C_L = 5$ pF			25	ns
t_{io}	I/O input buffer delay				2	ns

combinational mode, turbo bit off

PARAMETER[†]		TEST CONDITIONS		MIN	MAX	UNIT
t_{pd1}	Input to nonregistered output delay	$C_L = 35$ pF			45	ns
t_{pd2}	I/O input to nonregistered output delay				47	ns
t_{PZX}	Output enable time	$C_L = 35$ pF	See Note 5		45	ns
t_{PXZ}	Output disable time	$C_L = 5$ pF			45	ns
t_{io}	I/O input buffer delay				2	ns

synchronous clock mode, mode 0

PARAMETER[†]			TEST CONDITIONS	MIN	MAX	UNIT
f_{max}	Maximum frequency[‡]	No feedback		50		MHz
		Internal feedback		50		
		External feedback[§]		33.3		
t_{co1}	Clock to output delay time				15	ns
t_{cnt}	Minimum clock period (register feedback to register output)		See Note 6		25	ns
t_{clr}	Asynchronous output clear time	Turbo bit on	$C_L = 35$ pF		27	ns
		Turbo bit off			47	

[†] Letter symbols for switching characteristics and timing requirements in this data sheet have been chosen for compatibility with those used in other documentation previously prepared by another supplier for similar products. Any similarity to symbols used on other TI data sheets or to those shown in glossaries in TI data books is coincidental. The meanings may not be the same.

[‡] f_{max} with no feedback $= \dfrac{1}{t_{ch} + t_{cl}}$

f_{max} with internal feedback $= \dfrac{1}{t_{cnt}}$

f_{max} with external feedback $= \dfrac{1}{t_{su} + t_{co1}}$

f_{max} with internal feedback is programmed as a 16-bit counter.

[§] Use t_{su} and t_{co1} for a device programmed with the turbo bit on.

NOTES: 5. This is for an output voltage change of 500 mV.
6. These parameters are measured with device programmed as a 16-bit counter.

switching characteristics over recommended ranges of supply voltage and operating free air temperature (unless otherwise noted)

asynchronous clock mode, mode 1

PARAMETER†			TEST CONDITIONS	MIN	MAX	UNIT
f_{max}	Maximum frequency‡	No feedback		50		MHz
		Internal feedback		50		
		External feedback§		28.6		
t_{aco1}	Clock to output delay time	Turbo bit on			27	ns
		Turbo bit off			47	
t_{acnt}	Minimum clock period (register feedback to register output)				35	ns
t_{clr}	Asynchronous output clear time	Turbo bit on	C_L = 35 pF		27	ns
		Turbo bit off			47	

timing requirements over recommended ranges of supply voltage and free-air temperature

synchronous clock mode, mode 0

PARAMETER†			MIN	MAX	UNIT
t_{su}	Input setup time	Turbo bit on	15		ns
		Turbo bit off	35		
t_h	Input hold time		0		ns
t_{ch}	Clock high pulse duration		10		ns
t_{cl}	Clock low pulse duration		10		ns

asynchronous clock mode, mode 1

PARAMETER†			MIN	MAX	UNIT
t_{asu}	Input setup time	Turbo bit on	8		ns
		Turbo bit off	28		
t_{ah}	Input hold time		12		ns
t_{ach}	Clock high pulse duration		10		ns
t_{acl}	Clock low pulse duration		10		ns

† Letter symbols for switching characteristics and timing requirements in this data sheet have been chosen for compatibility with those used in other documentation previously prepared by another supplier for similar products. Any similarity to symbols used on other TI data sheets or to those shown in glossaries in TI data books is coincidental. The meanings may not be the same.

‡ f_{max} with no feedback = $\frac{1}{t_{ach} + t_{acl}}$

f_{max} with internal feedback = $\frac{1}{t_{acnt}}$

f_{max} with external feedback = $\frac{1}{t_{asu} + t_{aco1}}$

f_{max} with internal feedback is programmed as a 16-bit counter.

§ Use t_{su} and t_{co1} for a device programmed with the turbo bit on.

functional testing

The EP630 is functionally tested through complete testing of each programmable EPROM bit and all internal logic elements, thus ensuring 100% programming yield. As a result, traditional problems associated with fuse programmed circuits are eliminated.

design security

The EP630 contains a programmable design security feature that controls the access to the data programmed into the device. If this programmable feature is used, a proprietary design implemented in the device cannot be copied nor retrieved. A very high level of design control is thus achieved since programmed data within EPROM cells is invisible.

turbo bit

This family of EPLDs contains a programmable option to control the automatic power-down feature that enables the low-standby-power mode of the device. This option is controlled by a turbo bit that can be set by the design software. When the turbo bit is on, the low-standby-power mode is disabled. This renders the circuit less sensitive to V_{CC} noise transients created by the power-up/power-down cycle when operating in the low-power mode. The typical I_{CC} versus frequency data for both the turbo-bit-on mode and the turbo-bit-off (low-power) mode is shown in Figure 5. All dynamic parameters are tested with the turbo bit on.

latch-up

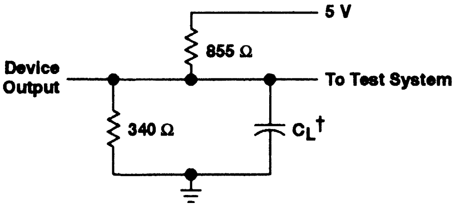
The EP630 input, I/O, and clock pins have been carefully designed to resist latch-up which is inherent in CMOS structures. None of the EP630 pins will latch up for input voltages between –1 V to V_{CC} + 1 V with currents up to 250 mA. During transitions, the inputs may undershoot to –2 V for periods of less than 20 ns.

Although the programming pin (pin 11) is designed to resist latch-up to the 14 V device limit during positive current latch-up testing, the verify mode (pin 1) and program mode (pin 11) can be inadvertently entered into thereby causing current flow in the pins. This should not be construed as latch-up.

device programming

The EP630 can be programmed using certified third-party programming equipment. Please contact Texas Instruments applications department at (214) 997-5666 for current status of third-party programming support.

PARAMETER MEASUREMENT INFORMATION



This figure shows the test circuit and the conditions under which dynamic measurements are made. Because power supply transients can affect dynamic measurements, simultaneous transitions of multiple outputs should be avoided to ensure accurate measurement. The performance of threshold tests under dynamic conditions should not be attempted. Large-amplitude fast ground-current transients normally occur as the device outputs discharge the load capacitances. These transients flowing through the parasitic inductance between the device ground terminal and the test-system ground can create significant reductions in the observable input noise immunity.

† Includes jig capacitance
Equivalent loads may be used for testing

Figure 4. Dynamic Test Circuit

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
MAXIMUM FREQUENCY

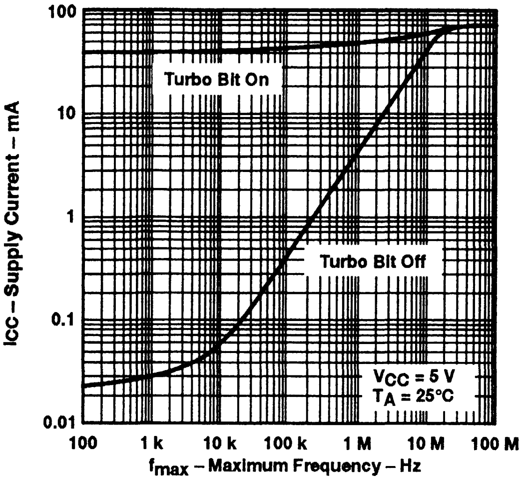


Figure 5

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

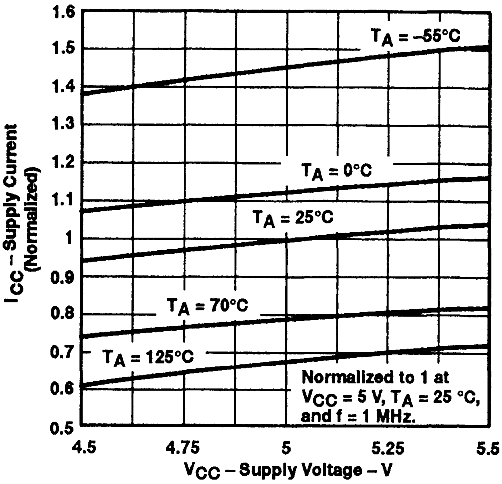


Figure 6

PROPAGATION DELAY TIME
vs
SUPPLY VOLTAGE

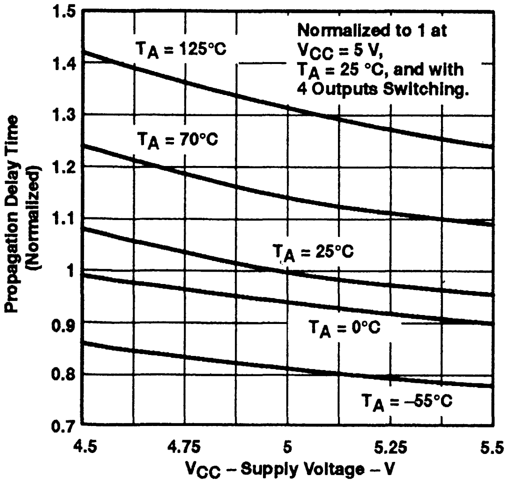


Figure 7

PROPAGATION DELAY TIME
vs
NUMBER OF OUTPUTS SWITCHING

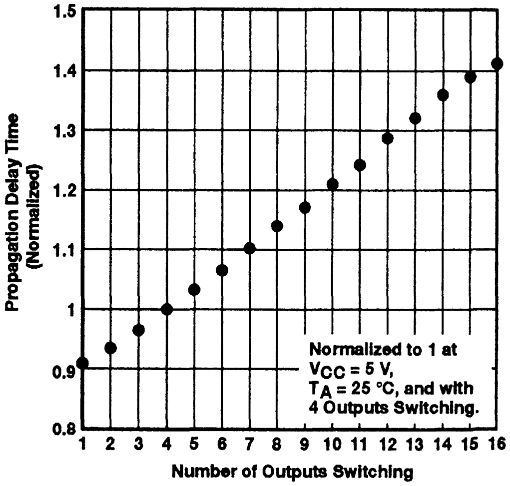
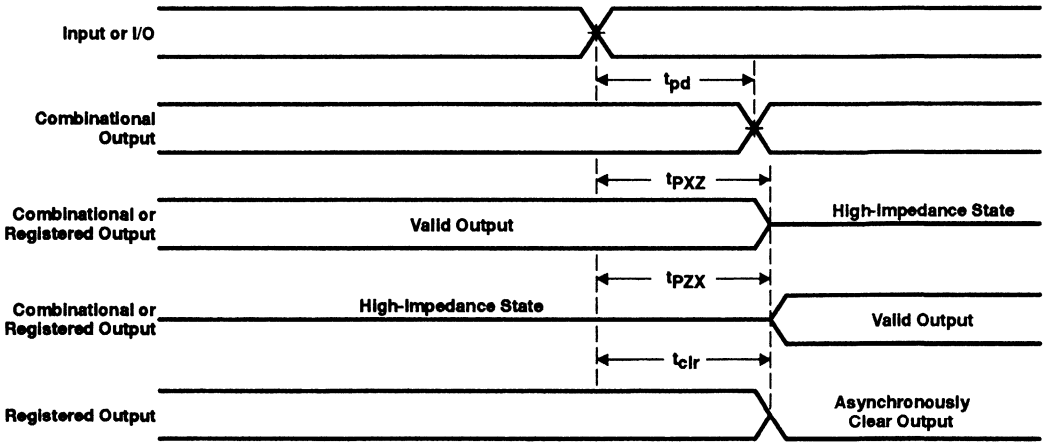
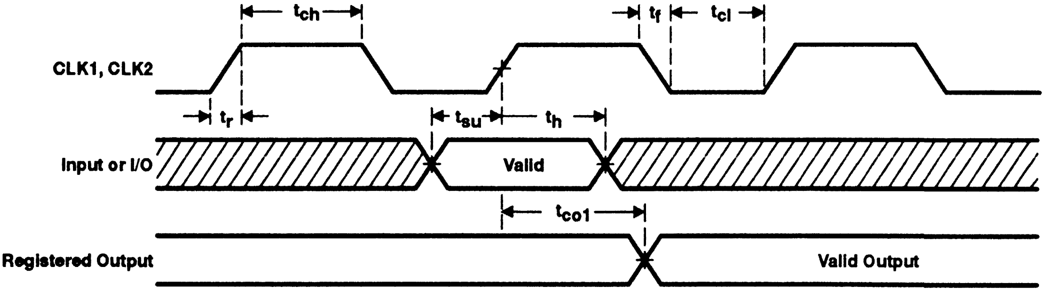


Figure 8

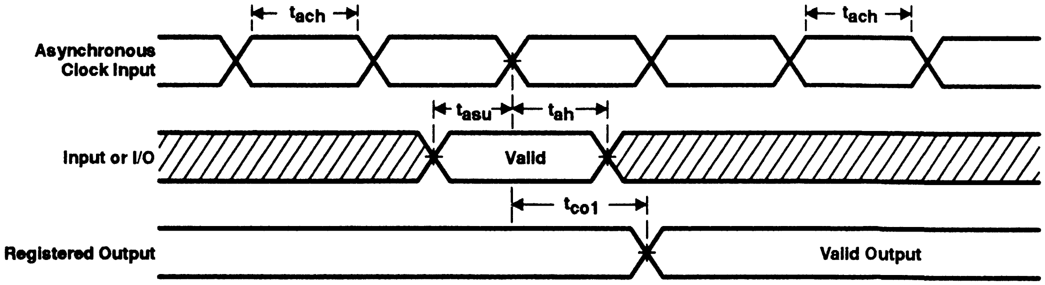
PARAMETER MEASSUREMENT INFORMATION



(a) COMBINATIONAL MODE



(b) SYNCHRONOUS CLOCK MODE



(c) ASYNCHRONOUS CLOCK MODE

NOTES: A. Input and I/O pulse levels are 0 to 3 V and $t_r = t_f \leq 2$ ns.

B. All measurements are made at 1.5 V except t_{cl} and t_{ch} are measured at 0.3 V and 2.7 V respectively and t_{PZX} and t_{PXZ} are measured for an output voltage change of 500 mV.

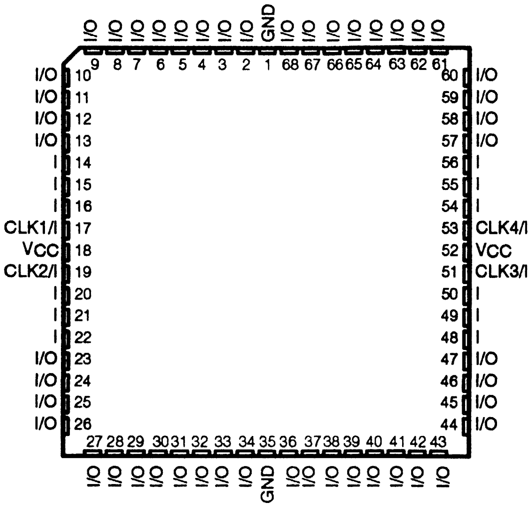
Figure 9. Switching Waveforms

EP1830 SERIES
HIGH-PERFORMANCE 48-MACROCELL ONE-TIME PROGRAMMABLE LOGIC DEVICES

SRES003–D3880, NOVEMBER 1991

- **User-Configurable LSI Circuit Capable of Implementing 2100 Equivalent Gates of Conventional and Custom Logic**
- **High-Performance CMOS Process Allows:**
  Maximum t_{pd}: - 20C . . . 20 ns
  - 25C . . . 25 ns
  - 30C . . . 30 ns
  - 25I . . . 25 ns
  - 30I . . . 30 ns
- **Low Operating Current:**
  I_{CC} max (standby) . . . 150 µA
  I_{CC} max (turbo bit off) . . . 40 mA
  I_{CC} max (turbo bit on) . . . 225 mA
- **Programmable Clock Option Allows Asynchronous Clocking of All Registers or Banked Register Operation From 4 Synchronous Clocks**
- **Programmable Asynchronous Clear of All Registers**
- **Forty-Eight Macrocells With Configurable I/O Architecture Allowing for up to 64 Inputs and 48 Outputs**
- **Macrocell Flip-Flops can be Individually Programmed as D-, T-, JK-, SR-Type Flip-Flops or for Combinational Operation**
- **Programmable Design Security Bit Prevents Copying of Logic Stored in Device**
- **Available Third-Party Design and Programming Support**

FN PACKAGE
(TOP VIEW)



AVAILABLE OPTIONS

T_A RANGE	SPEED CLASS	PLASTIC CHIP CARRIER (PLCC)
0°C to 70°C	20 ns	EP1830-20CFN
	25 ns	EP1830-25CFN
–40°C to 85°C	25 ns	EP1830-25IFN
	30 ns	EP1830-30IFN

description

general

The EP1830 series of CMOS EPLDs from Texas Instruments offer LSI density, TTL equivalent speed performance and low power consumption. Each device is capable of implementing over 2100 equivalent gates of SSI, MSI, and custom logic circuits. The EP1830 series is packaged in a 68-pin J-leaded plastic (one-time programmable) Chip Carrier.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 1991, Texas Instruments Incorporated

TEXAS INSTRUMENTS

The EP1830 series is designed as an LSI replacement for traditional low-power Schottky TTL logic circuits. Its speed and density also make it suitable for high-performance complex functions such as dedicated peripheral controllers and intelligent support chips. Integrated-circuit count and power requirements can be reduced by several orders of magnitude allowing similar reduction in total size and cost of the system, with significantly enhanced reliability.

The EP1830 uses a 1.0 µm CMOS EPROM technology employing EPROM transistors to configure logic connections. The EPROM technology allows 100% generic testing (all devices are 100% tested at the factory).

Programming the EP1830 is made easy by the availability of third-party support for design entry, design processing and device programming.

The EP1830-20C and EP1830-25C devices are characterized for operation from 0°C to 70°C. The EP1830-25I and EP1830-30I are characterized for operation from −40°C to 85°C.

functional

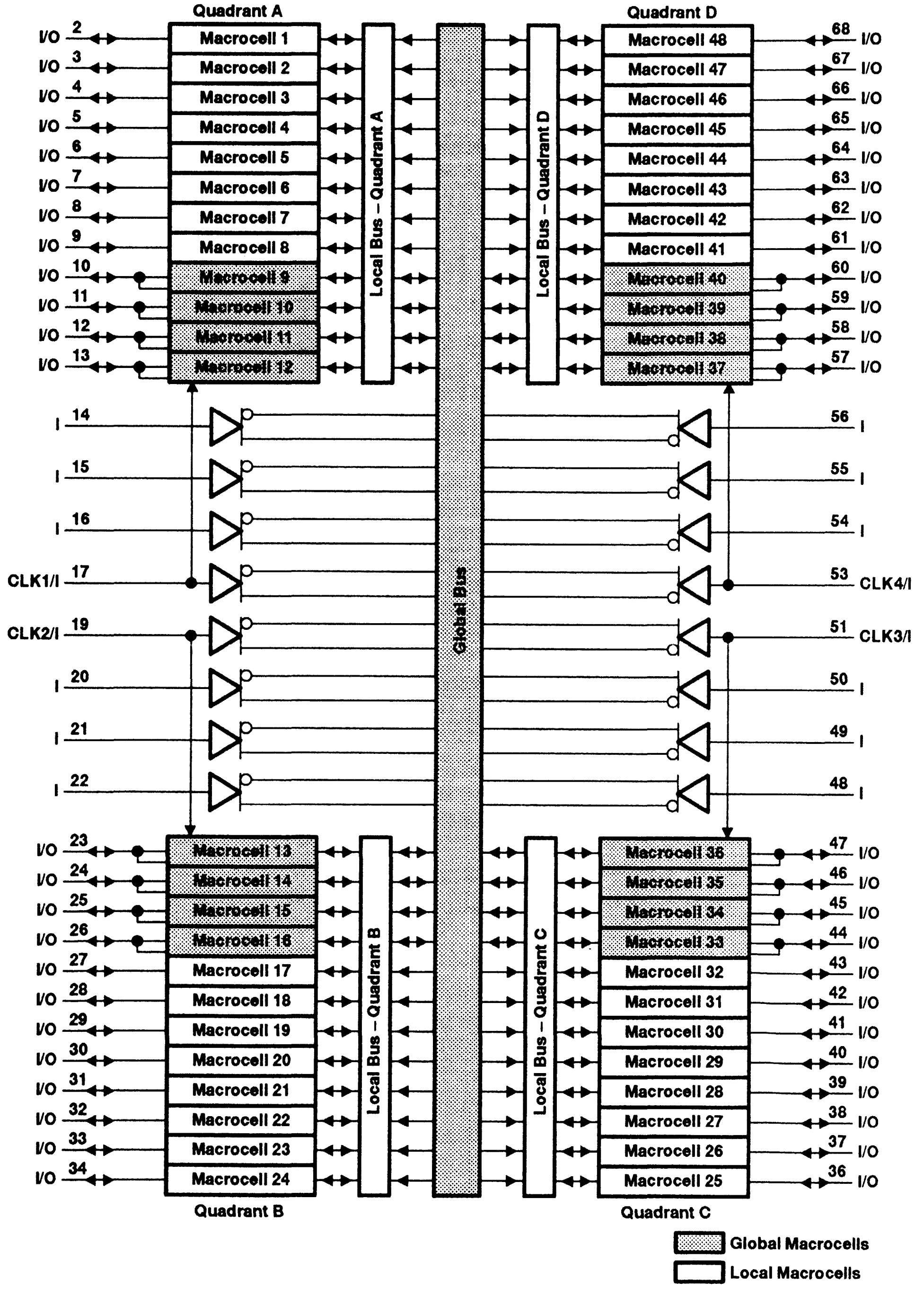
The EP1830 series use CMOS EPROM cells to configure logic functions within the device. The EP1830 architecture is 100% user configurable, allowing the device to accommodate a variety of independent logic functions. Externally, the EP1830 provides 16 dedicated data inputs, four of which may be used as system clock inputs. There are 48 I/O pins, which may be individually configured for input, output, or bidirectional data flow.

macrocells

The EP1830 architecture consists of a series of macrocells. All logic is implemented within these macrocells. Each macrocell, shown in Figure 1, contains three basic elements: a logic array, a selectable register element, and 3-state I/O buffer. All combinational logic such as exclusive-OR, NAND, NOR, AND, OR and inverted gates are implemented within the logic array. For register applications, each macrocell provides one of two possible flip-flop options: D or T. Third party software will allow design with JK or SR flip-flops, implementing these with the T flip-flop option. Each EP1830 macrocell is equivalent to over 40 2-input NAND gates.

The EP1830 is partitioned into four identical quadrants. Each quadrant contains 12 macrocells. Input signals into the macrocells come from the EP1830 internal bus structures. Macrocell outputs may drive the EP1830 external pins as well as the internal buses. Figure 2 illustrates a simple logic function that can be implemented within a single macrocell. Note that all combinational logic is implemented within the logic array, a JK flip-flop is selected, and the 3-state buffer is permanently enabled.

functional block diagram



Each EP1830 macrocell consists of 3 basic components (see Figure 1)

Step 1. A logic array for gated logic
Step 2. A flip-flop for data storage (selectable options include D, T and software emulated JK and SR). The flip-flop may be bypassed for purely combinational functions.
Step 3. A 3-state buffer to define input, output, or bidirectional data flow.

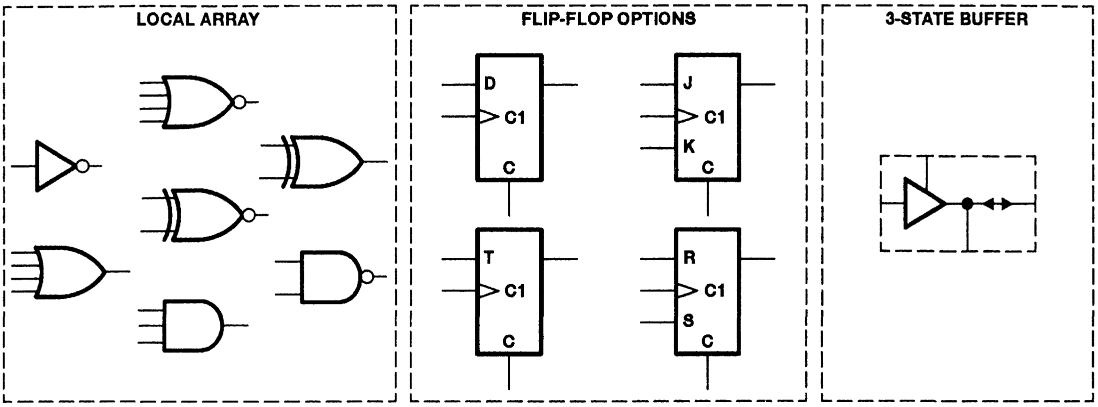


Figure 1. Marcocell Components

Typical logic function implemented into a single macrocell. Each EP1830 macrocell can accommodate the equivalent of 40 gates.

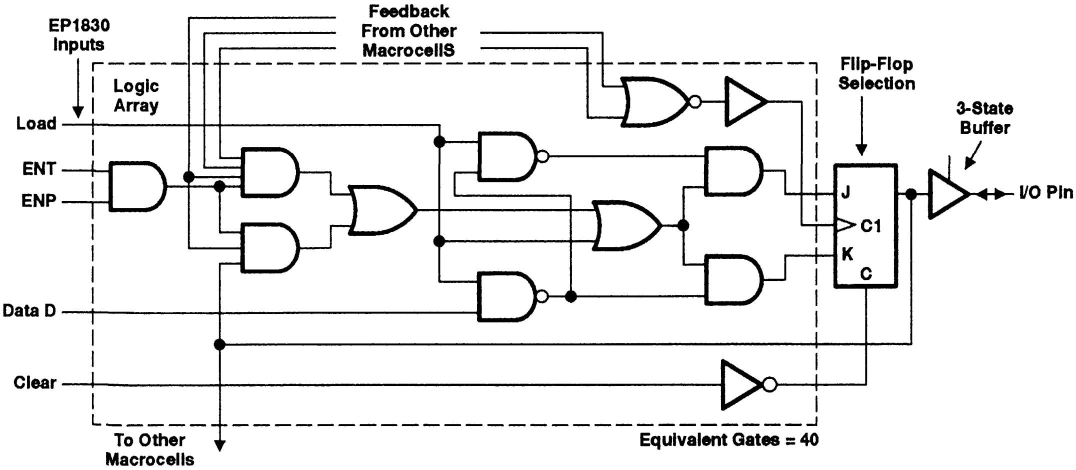


Figure 2. Sample Circuit

The EP1830 macrocell architecture is shown in Figures 3 and 4. There are 32 macrocells called local macrocells. These macrocells offer a multiplexed feedback path (pin or internal) which drives the local bus of the respective quadrant.

There are another 16 macrocells known as the global macrocells (see Figure 4). These global macrocells have features that allow each macrocell to implement buried logic functions and at the same time serve as dedicated input pins. Thus the EP1830 may have an additional 16 input pins giving a total of 32 inputs. The global macrocells have the same timing characteristics as the local macrocells.

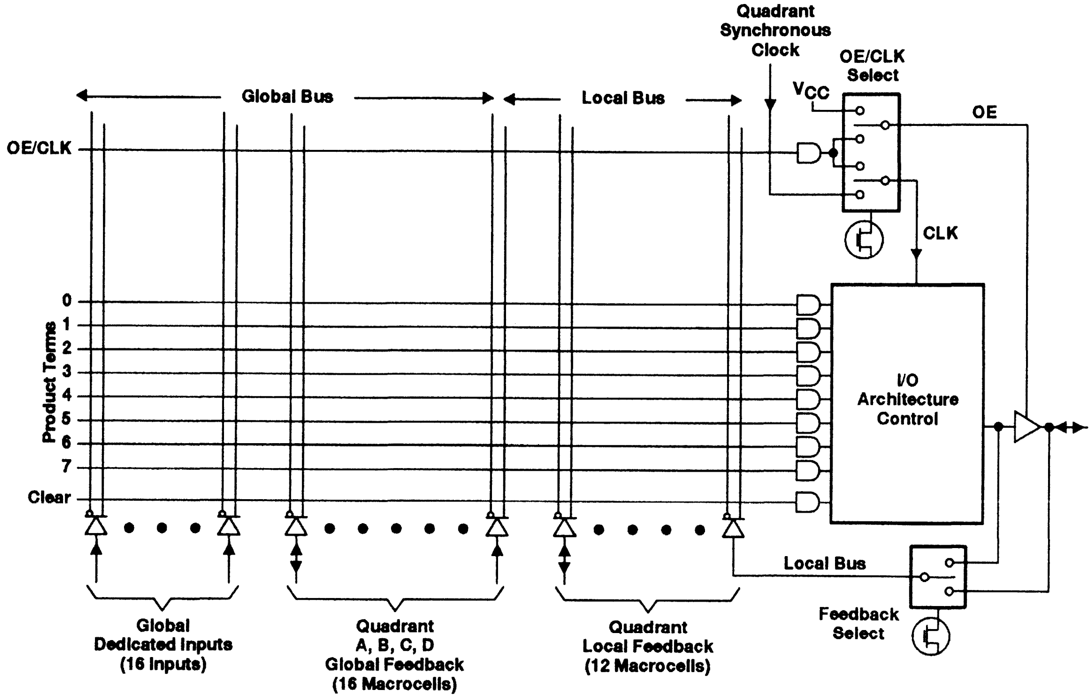


Figure 3. Local Macrocell Logic Array

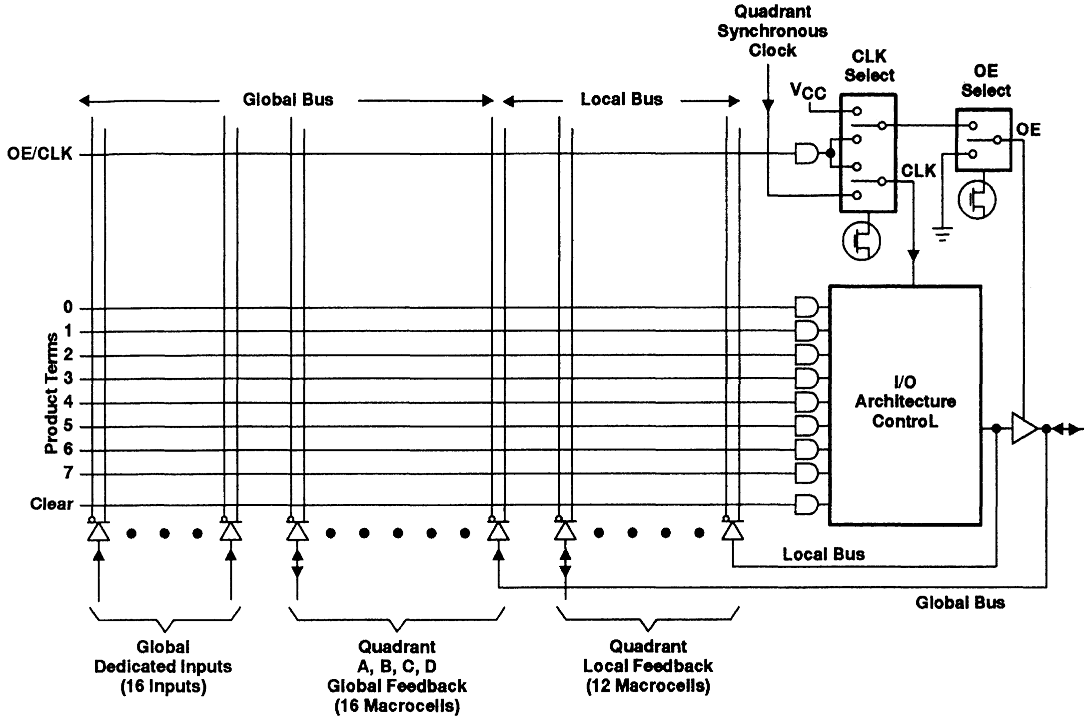


Figure 4. Global Macrocell Logic Array

clock options

Each of the EP1830 internal flip-flops may be clocked independently or in user defined groups. The architecture allows for asynchronous clocking using the OE/CLK product term to provide input or internal logic functions as a clock. If this mode is used the output enable buffer cannot be controled by this product term. The flip-flops can be configured for positive or negative edge triggered operation with asyncronous clock mode.

Four dedicated system clocks (CLK1 thru CLK4) also provide clock signals to the flip-flops. System clocks are connected directly from the EP1830 external pins. With this direct connection, system clocks give enhanced clock to output delay times than internally operated clock signals. There is one system clock per EP1830 quadrant. When using system clocks, the flip-flops are positive edge triggered (data transitions occur on the rising edge of the clock).

third party design support

Texas Instruments is working in conjunction with several software manufacturers to provide excellent design software support for the EP1830. This support ranges from high level design entry compilers to schematic capture programs in which the designer may implement his design with standard TTL SSI and MSI based circuits such as counters, comparators, shift registers, etc. Please contact Texas Instruments applications hotline at (214) 997-5666 for current status of third-party programming support.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1)	−0.3 V to 7 V
Instantaneous supply voltage range, V_{CC} ($t \leq 20$ ns)	−2 V to 7 V
Programming supply voltage range, V_{PP}	−0.3 V to 14 V
Instantaneous programming supply voltage range, V_{PP} ($t \leq 20$ ns)	−2 V to 14 V
Input voltage range, V_I	−0.3 V to 7 V
Instantaneous input voltage range, V_I ($t \leq 20$ ns)	−2 V to 7 V
V_{CC} or GND current range	−300 mA to 300 mA
Continuous total power dissipation at or below 25°C free-air temperature (see Note 2)	1500 mW
Operating free-air temperature, T_A	−65°C to 135°C
Storage temperature range	−65°C to 150°C

NOTES: 1. All voltage values are with respect to GND terminal.
2. For operation above 25°C free-air temperature, derate to 180 mW at 135°C at a rate of 12 mW/°C

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		4.75	5.25	V
V_I	Input voltage		0	V_{CC}	V
V_{IH}	High-level input voltage		2	V_{CC}+0.3	V
V_{IL}	Low-level input voltage (see Note 3)		−0.3	0.8	V
V_O	Output voltage		0	V_{CC}	V
t_r	Rise time	CLK input		20	ns
		Other inputs		50	
t_f	Fall time	CLK input		20	ns
		Other inputs		50	
T_A	Operating free-air temperature		0	70	°C

NOTE 3: The algebraic convention, in which the more negative value is designated minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	TTL	V_{CC} = 4.75 V,	I_{OH} = −4 mA	2.4			V
		CMOS	V_{CC} = 4.75 V,	I_{OH} = −2 mA	3.84			
V_{OL}	Low-level output voltage		V_{CC} = 4.75 V,	I_{OL} = 4 mA			0.45	V
I_I	Input current		V_{CC} = 5.25 V,	V_I = V_{CC} or GND			±10	μA
I_{OZ}	Off-state output current		V_{CC} = 5.25 V,	V_O = V_{CC} or GND			±10	μA
I_{CC}	Supply current	Standby	V_{CC} = 5.25 V, V_I = V_{CC} or GND, No load	See Note 4		50	150	μA
		Nonturbo		See Note 5		20	40	mA
		Turbo		See Note 5		150	225	
C_i	Input capacitance		V_I = 0, f = 1 MHz,	T_A = 25°C		20		pF
C_o	Output capacitance		V_O = 0, f = 1 MHz,	T_A = 25°C		20		pF
C_{clk}	Clock capacitance		V_I = 0, f = 1 MHz,	T_A = 25°C		25		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

NOTES: 4. When in the nonturbo mode, the device automatically goes into the standby mode approximately 100 ns after the last transition.
5. These parameters are measured with the device programmed as four 12-bit counters and f = 1 MHz.

external switching characteristics and timing requirements over recommended ranges of supply voltage and operating free air temperature (unless otherwise noted)

turbo-bit on (turbo mode)

PARAMETER†		TEST CONDITIONS	EP1830-20C		EP1830-25C		EP1830-30C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	See Note 6	62.5		50		41.7		MHz
f_{cnt}	Maximum internal frequency	See Note 7	50		40		33.3		MHz
t_{pd1}	Input to nonregistered output delay	C_L = 35 pF		20		25		30	ns
t_{pd2}	I/O input to nonregistered output delay			22		28		34	ns
t_{su}	System clock setup time		13		17		21		ns
t_{hs}	System clock hold time		0		0		0		ns
t_{ch}	System clock high		8		10		12		ns
t_{cl}	System clock low		8		10		12		ns
t_{co1}	System clock to output delay	C_L = 35 pF		15		18		21	ns
t_{asu}	Array clock setup time		8		10		12		ns
t_{ah}	Array clock hold time		8		10		12		ns
t_{aco1}	Array clock to output delay			20		25		30	ns
t_{cnt}	Minimum system clock period			20		25		30	ns

turbo-bit off (non-turbo mode)

PARAMETER†		TEST CONDITIONS	EP1830-20C		EP1830-25C		EP1830-30C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	See Note 6	62.5		50		41.7		MHz
f_{cnt}	Maximum internal frequency	See Note 7	50		40		33.3		MHz
t_{pd1}	Input to nonregistered output delay	C_L = 35 pF		45		50		55	ns
t_{pd2}	I/O input to nonregistered output delay			47		53		59	ns
t_{su}	System clock setup time		38		42		46		ns
t_{hs}	System clock hold time		0		0		0		ns
t_{ch}	System clock high		8		10		12		ns
t_{cl}	System clock low		8		10		12		ns
t_{co1}	System clock to output delay	C_L = 35 pF		15		18		21	ns
t_{asu}	Array clock setup time		33		35		37		ns
t_{ah}	Array clock hold time		8		10		12		ns
t_{aco1}	Array clock to output delay			45		50		55	ns
t_{cnt}	Minimum system clock period			20		25		30	ns

† Letter symbols for switching characteristics and timing requirements in this data sheet have been chosen for compatibility with those used in other documentation previously prepared by another supplier for similar products. Any similarity to symbols used on other TI data sheets or to those shown in glossaries in TI data books is coincidental. The meanings may not be the same.

NOTES: 6. The f_{max} values shown represent the highest frequency of operation without feedback.
7. This parameter is measured with the device programmed as four 12-bit counters.

internal timing requirements over recommended ranges of supply voltage and operating free air temperature (unless otherwise noted)

turbo-bit on (turbo mode)

PARAMETER†		TEST CONDITIONS	EP1830-20C		EP1830-25C		EP1830-30C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{in}	Input pad and buffer delay			5		7		9	ns
t_{io}	I/O input pad and buffer delay			2		3		4	ns
t_{lad}	Logic array delay			9		12		15	ns
t_{od}	Output pad and buffer delay	C_L = 35 pF		6		6		6	ns
t_{zx}	Output buffer enable time	C_L = 35 pF		6		6		6	ns
t_{xz}	Output buffer disable time	C_L = 5 pF, See Note 8		6		6		6	ns
t_{su}	Register setup time		8		10		12		ns
t_h	Register hold time		8		10		12		ns
t_{ic}	Array clock delay			9		12		15	ns
t_{ics}	System clock delay			4		5		6	ns
t_{fd}	Feedback delay			3		3		3	ns
t_{clr}	Register clear delay			9		12		15	ns

turbo-bit off (non-turbo mode)

PARAMETER†		TEST CONDITIONS	EP1830-20C		EP1830-25C		EP1830-30C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{in}	Input pad and buffer delay			5		7		9	ns
t_{io}	I/O input pad and buffer delay			2		3		4	ns
t_{lad}	Logic array delay			34		35		40	ns
t_{od}	Output pad and buffer delay	C_L = 35 pF		6		6		6	ns
t_{zx}	Output buffer enable time	C_L = 35 pF		6		6		6	ns
t_{xz}	Output buffer disable time	C_L = 5 pF, See Note 8		6		6		6	ns
t_{su}	Register setup time		8		10		12		ns
t_h	Register hold time		8		10		12		ns
t_{ic}	Array clock delay			34		35		40	ns
t_{ics}	System clock delay			4		5		6	ns
t_{fd}	Feedback delay	See Note 9		−22		−22		−22	ns
t_{clr}	Register clear delay			34		35		40	ns

† Letter symbols for switching characteristics and timing requirements in this data sheet have been chosen for compatibility with those used in other documentation previously prepared by another supplier for similar products. Any similarity to symbols used on other TI data sheets or to those shown in glossaries in TI data books is coincidental. The meanings may not be the same.

NOTES: 8. This is for an output voltage change of 500 mV.

9. The negative number shown for this specification is to compensate for the 30 ns that is being added to the t_{lad} parameter in the turbo-bit off mode. In the non-turbo mode, t_{fd} is not affected by the additional propagation delay because the logic array is already taken out of the non-turbo mode by the first transition into the array. See the section on delay elements.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage range, V_{CC} (see Note 1)	−0.3 V to 7 V
Instantaneous supply voltage range, V_{CC} ($t \le 20$ ns)	−2 V to 7 V
Programming supply voltage range, V_{PP}	−0.3 V to 14 V
Instantaneous programming supply voltage range, V_{PP} ($t \le 20$ ns)	−2 V to 14 V
Input voltage range, V_I	−0.3 V to 7 V
Instantaneous input voltage range, V_I ($t \le 20$ ns)	−2 V to 7 V
V_{CC} or GND current range	−300 mA to 300 mA
Continuous total power dissipation at or below 25°C free-air temperature (see Note 2)	1500 mW
Operating free-air temperature, T_A	−65°C to 135°C
Storage temperature range	−65°C to 150°C

NOTES: 1. All voltage values are with respect to GND terminal.
2. For operation above 25°C free-air temperature, derate to 180 mW at 135°C at a rate of 12 mW/°C

recommended operating conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage		4.5	5.5	V
V_I	Input voltage		0	V_{CC}	V
V_{IH}	High-level input voltage		2	$V_{CC}+0.3$	V
V_{IL}	Low-level input voltage (see Note 3)		−0.3	0.8	V
V_O	Output voltage		0	V_{CC}	V
t_r	Rise time	CLK input		20	ns
		Other inputs		50	
t_f	Fall time	CLK input		20	ns
		Other inputs		50	
T_A	Operating free-air temperature		−40	85	°C

NOTE 3: The algebraic convention, in which the more negative value is designated minimum, is used in this data sheet for logic voltage levels only.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIIONS		MIN	TYP†	MAX	UNIT
V_{OH}	High-level output voltage	TTL	$V_{CC} = 4.5$ V,	$I_{OH} = -4$ mA	2.4			V
		CMOS	$V_{CC} = 4.5$ V,	$I_{OH} = -2$ mA	3.84			
V_{OL}	Low-level output voltage		$V_{CC} = 4.5$ V,	$I_{OL} = 4$ mA			0.45	V
I_I	Input current		$V_{CC} = 5.5$ V,	$V_I = V_{CC}$ or GND			±10	µA
I_{OZ}	Off-state output current		$V_{CC} = 5.5$ V,	$V_O = V_{CC}$ or GND			±10	µA
I_{CC}	Supply current	Standby	$V_{CC} = 5.5$ V,	See Note 4		50	150	µA
		Nonturbo	$V_I = V_{CC}$ or GND,	See Note 5		20	40	mA
		Turbo	No load	See Note 5		150	260	
C_i	Input capacitance		$V_I = 0$, f = 1 MHz,	$T_A = 25°C$		20		pF
C_o	Output capacitance		$V_O = 0$, f = 1 MHz,	$T_A = 25°C$		20		pF
C_{clk}	Clock capacitance		$V_I = 0$, f = 1 MHz,	$T_A = 25°C$		25		pF

† All typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

NOTES: 4. When in the nonturbo mode, the device automatically goes into the standby mode approximately 100 ns after the last transition.
5. These parameters are measured with the device programmed as four 12-bit counters and f = 1 MHz.

external switching characteristics and timing requirements over recommended ranges of supply voltage and operating free air temperature (unless otherwise noted)

turbo-bit on (turbo mode)

PARAMETER†		TEST CONDITIONS	EP1830-25I		EP1830-30I		UNIT
			MIN	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	See Note 6	50		41.7		MHz
f_{cnt}	Maximum internal frequency	See Note 7	40		33.3		MHz
t_{pd1}	Input to nonregistered output delay	$C_L = 35$ pF		25		30	ns
t_{pd2}	I/O input to nonregistered output delay			28		34	ns
t_{su}	System clock setup time		17		21		ns
t_{hs}	System clock hold time		0		0		ns
t_{ch}	System clock high		10		12		ns
t_{cl}	System clock low		10		12		ns
t_{co1}	System clock to output delay	$C_L = 35$ pF		18		21	ns
t_{asu}	Array clock setup time		10		12		ns
t_{ah}	Array clock hold time		10		12		ns
t_{aco1}	Array clock to output delay			25		30	ns
t_{cnt}	Minimum system clock period			25		30	ns

turbo-bit off (non-turbo mode)

PARAMETER†		TEST CONDITIONS	EP1830-25I		EP1830-30I		UNIT
			MIN	MAX	MIN	MAX	
f_{max}	Maximum clock frequency	See Note 6	50		41.7		MHz
f_{cnt}	Maximum internal frequency	See Note 7	40		33.3		MHz
t_{pd1}	Input to nonregistered output delay	$C_L = 35$ pF		60		55	ns
t_{pd2}	I/O input to nonregistered output delay			53		59	ns
t_{su}	System clock setup time		42		46		ns
t_{hs}	System clock hold time		0		0		ns
t_{ch}	System clock high		10		12		ns
t_{cl}	System clock low		10		12		ns
t_{co1}	System clock to output delay	$C_L = 35$ pF		18		21	ns
t_{asu}	Array clock setup time		35		37		ns
t_{ah}	Array clock hold time		10		12		ns
t_{aco1}	Array clock to output delay			50		55	ns
t_{cnt}	Minimum system clock period			25		30	ns

† Letter symbols for switching characteristics and timing requirements in this data sheet have been chosen for compatibility with those used in other documentation previously prepared by another supplier for similar products. Any similarity to symbols used on other TI data sheets or to those shown in glossaries in TI data books is coincidental. The meanings may not be the same.

NOTES: 6. The f_{max} values shown represent the highest frequency of operation without feedback.
7. This parameter is measured with the device programmed as four 12-bit counters.

internal timing requirements over recommended ranges of supply voltage and operating free air temperature (unless otherwise noted)

turbo-bit on (turbo mode)

PARAMETER†		TEST CONDITIONS	EP1830-25I		EP1830-30I		UNIT
			MIN	MAX	MIN	MAX	
t_{in}	Input pad and buffer delay			7		9	ns
t_{io}	I/O input pad and buffer delay			3		4	ns
t_{lad}	Logic array delay			12		15	ns
t_{od}	Output pad and buffer delay	C_L = 35 pF		6		6	ns
t_{zx}	Output buffer enable time	C_L = 35 pF		6		6	ns
t_{xz}	Output buffer disable time	C_L = 5 pF, See Note 8		6		6	ns
t_{su}	Register setup time		10		12		ns
t_h	Register hold time		10		12		ns
t_{ic}	Array clock delay			12		15	ns
t_{ics}	System clock delay			5		6	ns
t_{fd}	Feedback delay			3		3	ns
t_{clr}	Register clear delay			12		15	ns

turbo-bit off (non-turbo mode)

PARAMETER†		TEST CONDITIONS	EP1830-25I		EP1830-30I		UNIT
			MIN	MAX	MIN	MAX	
t_{in}	Input pad and buffer delay			7		9	ns
t_{io}	I/O input pad and buffer delay			3		4	ns
t_{lad}	Logic array delay			37		40	ns
t_{od}	Output pad and buffer delay	C_L = 35 pF		6		6	ns
t_{zx}	Output buffer enable time	C_L = 35 pF		6		6	ns
t_{xz}	Output buffer disable time	C_L = 5 pF, See Note 8		6		6	ns
t_{su}	Register setup time		10		12		ns
t_h	Register hold time		10		12		ns
t_{ic}	Array clock delay			37		40	ns
t_{ics}	System clock delay			5		6	ns
t_{fd}	Feedback delay	See Note 9		–22		–22	ns
t_{clr}	Register clear delay			37		40	ns

† Letter symbols for switching characteristics and timing requirements in this data sheet have been chosen for compatibility with those used in other documentation previously prepared by another supplier for similar products. Any similarity to symbols used on other TI data sheets or to those shown in glossaries in TI data books is coincidental. The meanings may not be the same.

NOTES: 8. This is for an output voltage change of 500 mV.

9. The negative number shown for this specification is to compensate for the 30 ns that is being added to the t_{lad} parameter in the turbo-bit off mode. In the non-turbo mode, t_{fd} is not affected by the additional propagation delay because the logic array is already taken out of the non-turbo mode by the first transition into the array. See the section on delay elements.

design security

The EP1830 contains a programmable design security feature that controls the access to the data programmed into the device. If this programmable feature is used, a proprietary design implemented in the device cannot be copied or retrieved. This enables a high level of design control to be obtained since programmed data within the EPROM cells is invisible.

turbo bit

The EP1830 contains a programmable option to control the automatic power-down feature that enables the low-standby-power mode of the device. This option is controlled by a turbo bit that can be set during programming. When the turbo bit is on, the low-standby-power mode is disabled. The typical I_{CC} versus frequency data for both the turbo-bit-on mode and the turbo-bit-off (low power) mode is shown in Figure 10.

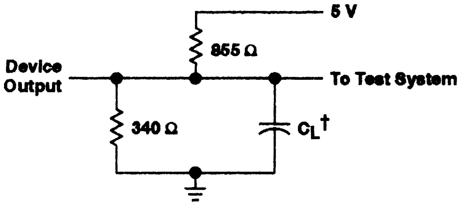
device programming

The EP1830 can be programmed using certified third-party programming equipment. Please contact Texas Instruments applications hotline at (214) 997-5666 for current status of third-party programming support.

functional testing

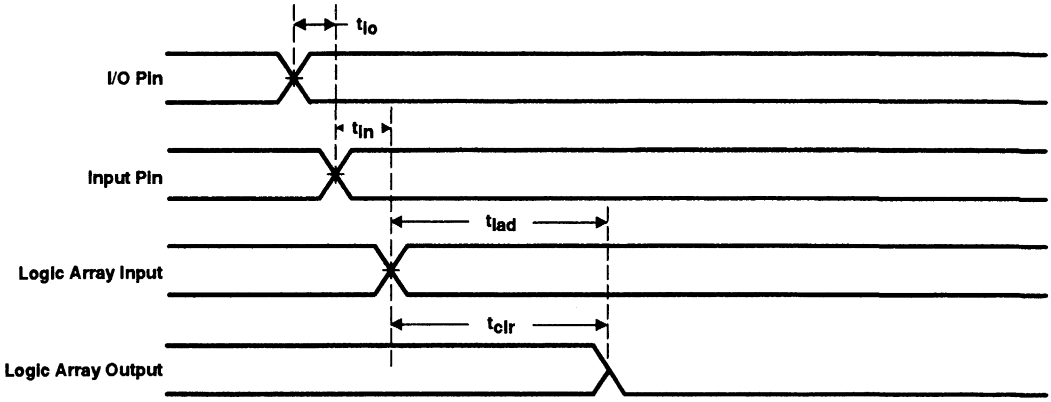
The EP1830 is functionally tested including complete testing of each programmable EPROM bit and all internal logic elements. The erasable nature (in wafer form) of the EP1830 allows test program patterns to be used and then erased.

Figure 5 shows the dynamic load circuit and the conditions under which dynamic measurements are made. Because power supply transients can affect dynamic measurements, simultaneous transitions of multiple outputs should be avoided to ensure accurate measurement. The performance of threshold tests under dynamic conditions should not be attempted. Large-amplitude fast ground-current transients normally occur as the device outputs discharge the load capacitances. These transients flowing through the parasitic inductance between the device ground terminal and the test-system ground can create significant reductions in observable input noise immunity.

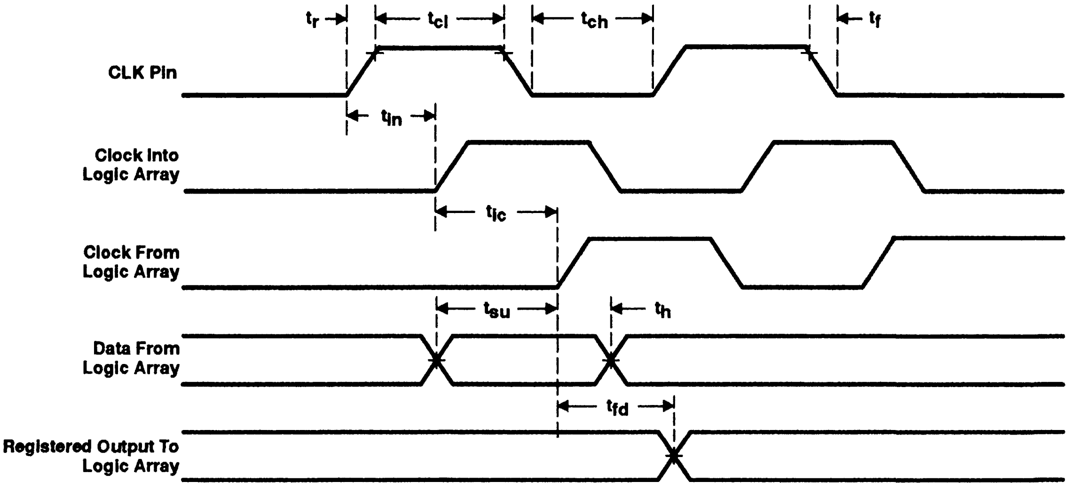


† Includes jig capacitance
All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f \leq 3$ ns, duty cycle = 50%.
Equivalent loads may be used for testing

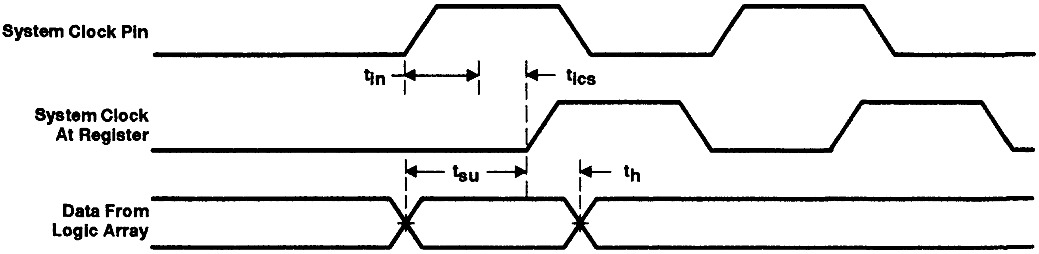
Figure 5. Dynamic Load Circuit



(a) INPUT MODE

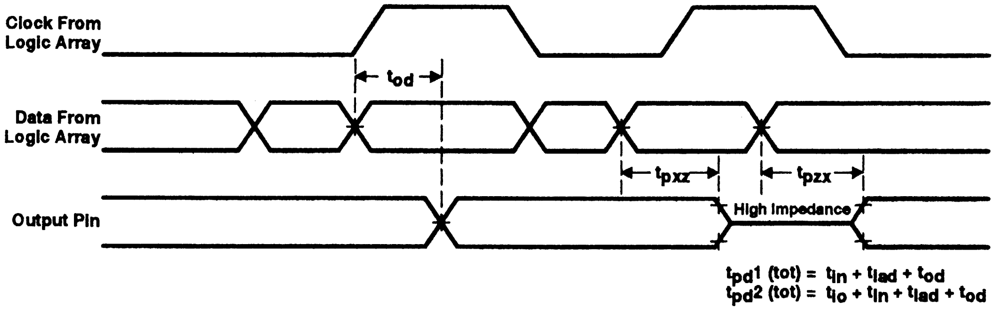


(b) CLOCK MODE



(c) SYSTEM CLOCK MODE

Figure 6. Switching Waveforms



(d) OUTPUT MODE

Figure 6. Switching Waveforms (continued)

understanding EP1830 timing characteristics

introduction

One of the most important benefits of using an EP1830 in any design is the integration of complex logic functions into single-chip solutions. In most cases, however, when the functional compatibility of a design has been determined, timing analysis should be completed to ensure dynamic parameter compatibility.

The purpose of this applications supplement is to discuss the timing delays which exist when using an EP1830. The focus here is on the inherent delay paths that exist in every EP1830 and their relation to the data sheet switching specifications. This should aid designers in modelling and simulating their logic designs.

gate delays versus timing characteristics

Accurate modelling of the timing characteristics requires an understanding of how a given application is implemented within the EP1830. Most designs contain basic gates, and TTL macrofunctions, which are emulated by the general macrocell structure. The macrocell structure is an array of logic in an AND/OR configuration with a programmable inversion followed by an optional flip-flop and feedback, (See Figure 7).

When designing with EP1830s, the term “gate delay” is not a useful measure. Within the EP1830 AND array are product terms. A product term is simply an n input AND gate where n is the number of connections. Depending on the logic implemented, a single product term may represent one to several gate equivalents. Therefore, gate delays do not necessarily provide EP1830 timing characteristics.

summary

To understand timing relationships of the EP1830, it is very important to break up the internal paths into meaningful microparameters that model portions of the architecture. Once internal paths are decomposed, it is then possible to obtain accurate timing information by summing the appropriate combinations of these microparameters. The EP1830 data sheet provides architectural information on which the parameters apply. Knowledge of the architecture allows characterization of any timing path within the EP1830.

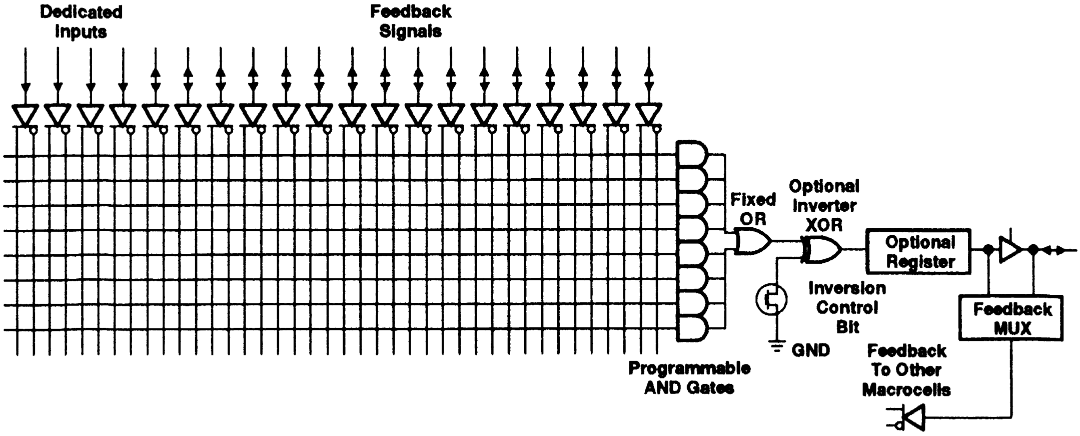
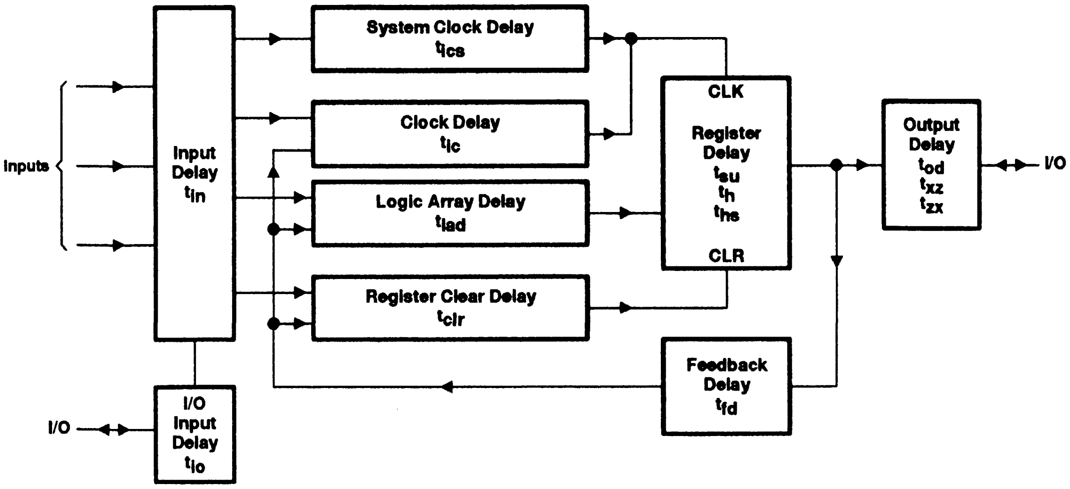


Figure 7. Macrocell

If the design requires low-power operation, the turbo bit should be off (disabled). When operating in this mode, some dynamic parameters are subject to increase.



For combinational outputs, the delay between the logic array and the output buffer is zero. (i. e., $t_{su} = 0$ or $t_h = 0$)

Figure 8. Macrocell Delay Paths Model

delay elements

The simplest solution to the architectural requirements is to model time through the logic array as a constant. This parameter is called t_{lad}. The rest of the elements in the timing model are similar to those found in conventional logic. There are input and output delay parameters (t_{in}, t_{io}, t_{od}); register parameters t_{su}, t_h, t_{clr}, t_{hs}, t_{ics}, t_{ic}); and internal connection parameters (t_{fd}). A detailed diagram of an Macrocell Delay Paths Model is shown in Figure 8 with a description of the signals.

glossary – internal delay elements

t_{clr} – Asynchronous register clear time. This is the amount of time it takes for a low signal to appear at the output of a register after the transition of the logic array, including the time required to go through the logic array.

t_{fd} – Feedback delay. In registered applications, this is the delay from the output of the register to the input of the logic array. In combinational applications, it is the delay from the combinational feedback to the input of the logic array.

t_h – Register hold time. This is the internal hold time of the register inside a macrocell – measured from the register clock to the register data input.

t_{lad} – Logic array delay. This parameter incorporates all delay from an input or feedback through the AND/OR structure.

t_{ic} – Clock delay. This delay incorporates all the delay incurred between the output of an input pad or I/O pad and the clock input of a register including the time required to go through the logic array.

t_{ics} – System clock delay. This delay incorporates all delays incurred between the output of the input pad and the clock input of the registers for dedicated clock pins.

t_{in} – Input delay. This is the delay from input pads through the buffers that direct the true and complement data input signals into the AND array.

t_{io} – I/O input pad delay. This delay applies to I/O pins committed as inputs.

t_{od} – Output buffer and pad delay. For registered applications, this incorporates the clock to output delay of the flip-flop. In combinational applications, it incorporates delay from the output of the array to the output of the device.

t_{su} – Register setup time. This is the internal setup time of the register inside a macrocell – measured from the register data input until the register clock.

t_{xz} – Time to high-impedance-state output delay. This delay incorporates the time between a high-to-low transition on the enable input of the 3-state buffer to assertion of a high impedance value at an output pin.

t_{zx} – 3-state to active output delay. This delay incorporates the time between a low-to-high transition on the enable input of the 3-state buffer to assertion of a high or low logic level at an output pin.

glossary – external delay elements

$t_{aco1(tot)}$ – Asynchronous clock to output delay. This is the time required to obtain a valid output after a clock is asserted on an input pin. This delay is the sum of the input delay (t_{in}), the clock delay (t_{ic}), and the output delay (t_{od}).

$t_{acnt(tot)}$ – Asynchronous clocked counter period. This is the minimum period a counter can maintain when asynchronously clocked. This delay is the sum of the feedback delay (t_{fd}), the logic array delay (t_{lad}), and the register setup time (tsu).

$t_{ah(tot)}$ – Asynchronous hold time. This is the amount of time required for data to be present after an asynchronous clock. This value is the difference between the sum of the input delay (t_{in}), the clock delay (t_{ic}), and the hold time (t_h) and the sum of the input delay (t_{in}) and logic array delay (t_{lad}).

$t_{asu(tot)}$ – Asynchronous setup time. This is the time required for data to be present at the input to the register before an asynchronous clock. This value is the difference between the sum of the input delay (t_{in}), array delay (t_{lad}), the register setup time (t_{su}), the sum of the input delay (t_{in}), and the clock delay (t_{ic}).

$t_{co1(tot)}$ – System clock to output delay. This is the time required to obtain a valid output after the system clock is asserted on an input pin. This delay is the sum of the input delay (t_{in}), the system clock delay (t_{ics}), and the output delay (t_{od}).

$t_{clr(tot)}$ – Delay required to clear register. This is the time required to change the output from high to low through a register clear measured from an input transition. This delay is the sum of input delay (t_{in}), register clear delay (t_{clr}), and the output delay (t_{od}).

$t_{cnt(tot)}$ – System clock counter period. This is the minimum period a counter can maintain. This delay is the sum of the feedback delay (t_{fd}), the logic array delay (t_{lad}), and the internal register setup time (t_{su}).

$t_{h(tot)}$ – Hold time for the register. This is the amount of time the data must be valid after the system clock. It is the difference between the sum of the internal input delay (t_{in}), the system clock (t_{ics}), and the system clock hold time (t_{hs}) and the sum of the input delay (t_{in}) and logic array delay (t_{lad}).

$t_{pd1(tot)}$ – Propagation Delay period; This is the delay from a dedicated input to a nonregistered output. This is the time required for data to propagate through the logic array and appear at the external output pin. This delay is the sum of input delay (t_{in}), array delay (t_{lad}), and output delay (t_{od}).

$t_{pd2(tot)}$ – Propagation Delay period; This is the delay from I/O pin to a non-registered output. This is the time required for data from any external I/O input to propagate through any combinational logic and appear at the external output pin. This delay is the sum of the I/O delay (t_{io}), input delay (t_{in}), array delay (t_{lad}), and the output delay (tod).

$t_{PXZ(tot)}$ – Time to enter into the high-impedance state. This is the time required to change an external output from a valid high or low logic level to the high-impedance state from an input transition. This delay is the sum of input delay (t_{in}), array delay (t_{lad}), and the time to disable the 3-state buffer (t_{xz}).

$t_{PZX(tot)}$ – Delay from high impedance to active output. This is the time required to change an external output from the high-impedance state to a valid high or low logic level measured from an input transition. This delay is the sum of input delay (t_{in}), array delay (t_{lad}), and the time to enable the 3-state buffer (t_{ZX}).

$t_{su(tot)}$ – Set up time for the register. This is the time required for data to be present at the register before the system clock. This value is the difference between the sum of input delay (t_{in}), array delay (t_{lad}), and an internal register setup time (t_{su}) and the sum of the input delay (t_{in}) and the system clock delay (t_{ics}).

explaining the data sheet specifications

The data sheet references timing parameters that characterize the switching operating specifications. These parameters are measured values, derived from extensive device characterization and 100% device testing. Among the switching characteristics are the following: $t_{aco(tot)}$, $t_{acnt(tot)}$, $t_{ah(tot)}$, $t_{asu(tot)}$, $t_{co1(tot)}$, $t_{clr(tot)}$, $t_{cnt(tot)}$, $t_{h(tot)}$, $t_{pd1(tot)}$, $t_{pd2(tot)}$, $t_{PXZ(tot)}$, $t_{PZX(tot)}$, $t_{su(tot)}$. These parameters, described below in detail, may be represented by the internal delay elements. (See Figure 9)

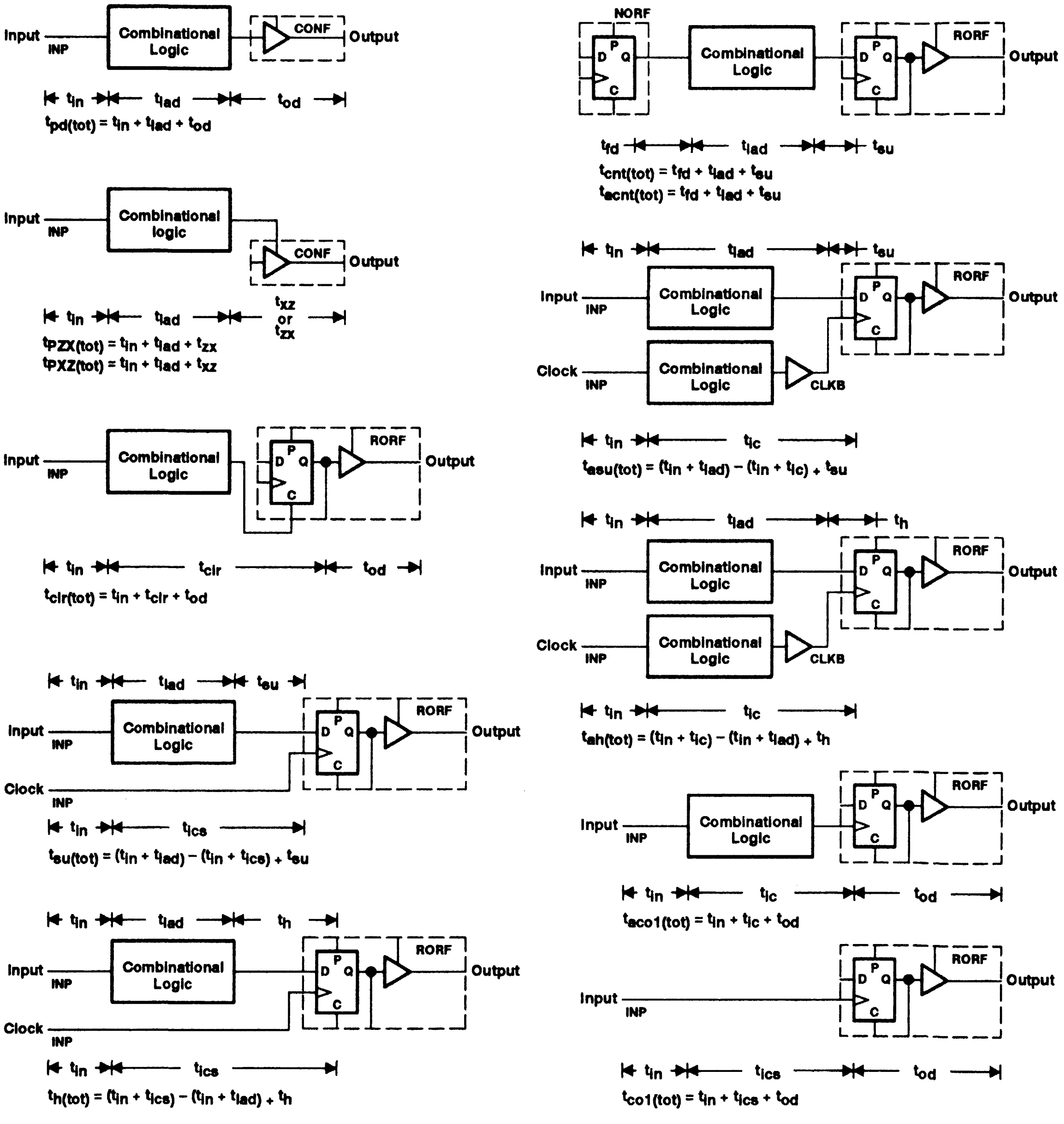


Figure 9. Timing Equations

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
MAXIMUM FREQUENCY

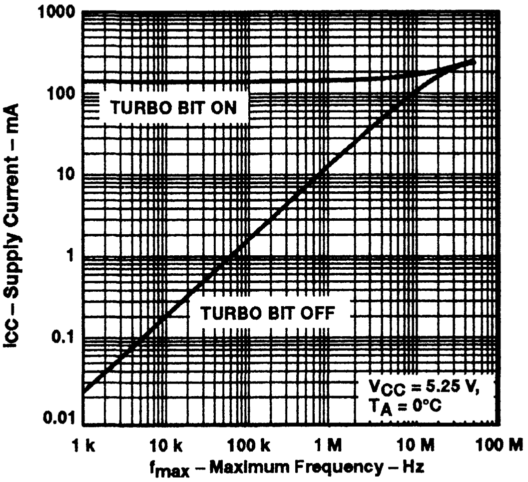


Figure 10

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

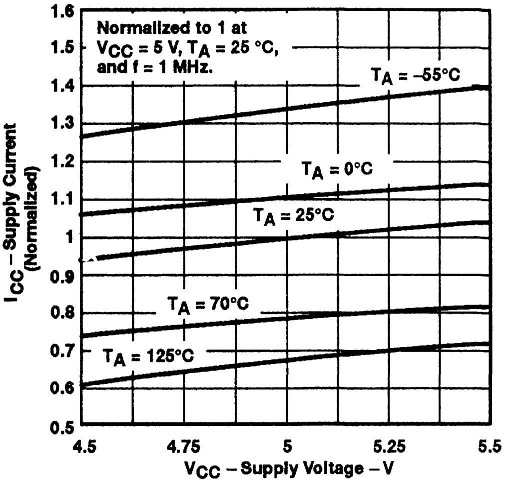


Figure 11

PROPAGATION DELAY TIME
vs
SUPPLY VOLTAGE

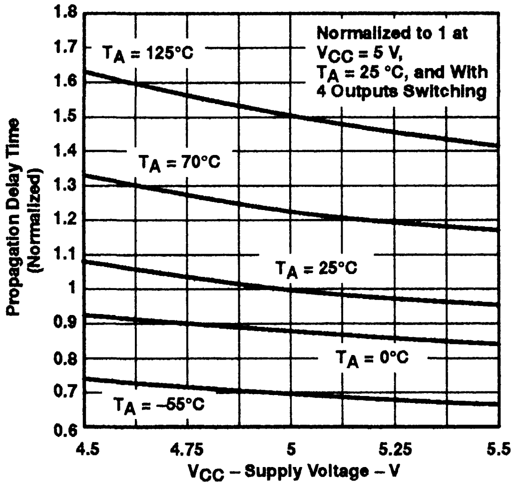


Figure 12

PROPAGATION DELAY TIME
vs
NUMBER OF OUTPUTS SWITCHING

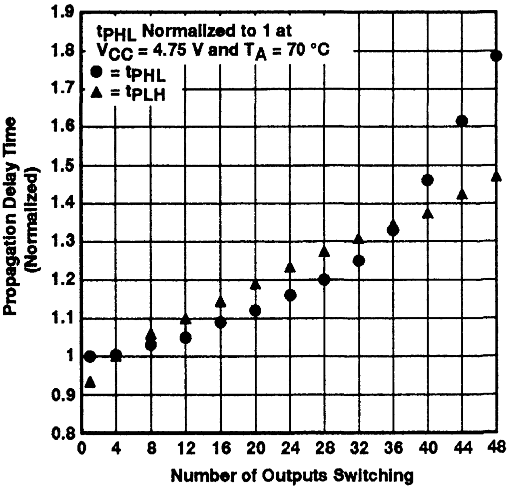
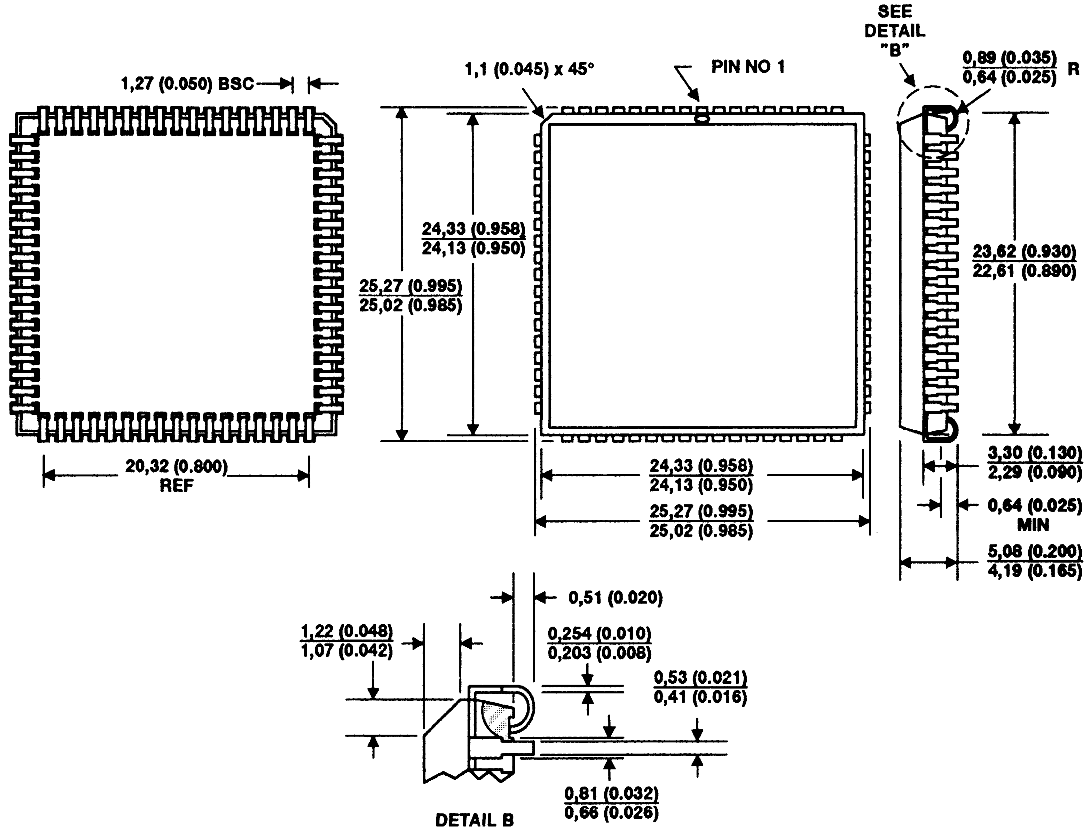


Figure 13

MECHANICAL DATA



ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES.

PAL16L8AM, PAL16L8A-2M, PAL16R4AM, PAL16R4A-2M PAL16R6AM, PAL16R6A-2M, PAL16R8AM, PAL16R8A-2M STANDARD HIGH-SPEED *PAL*® CIRCUITS

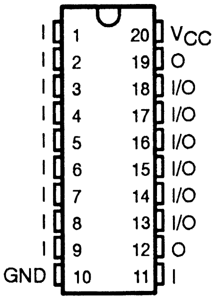
SRPS016 – D2705, FEBRUARY 1984 – REVISED MARCH 1992

- **Choice of Operating Speeds**
  High-Speed, A Devices . . . 25 MHz Min
  Half-Power, A-2 Devices . . . 16 MHz Min
- **Choice of Input/Output Configuration**
- **Package Options Include Both Ceramic DIP and Chip Carrier in Addition to Ceramic Flat Package**

DEVICE	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
PAL16L8	10	2	0	6
PAL16R4	8	0	4 (3-state buffers)	4
PAL16R6	8	0	6 (3-state buffers)	2
PAL16R8	8	0	8 (3-state buffers)	0

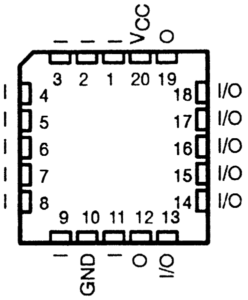
PAL16L8'
J OR W PACKAGE

(TOP VIEW)



PAL16L8'
FK PACKAGE

(TOP VIEW)



description

These programmable array logic devices feature high speed and a choice of either standard or half-power devices. They combine Advanced Low-Power Schottky technology with proven titanium-tungsten fuses. These devices will provide reliable, high-performance substitutes for conventional TTL logic. Their easy programmability allow for quick design of "custom" functions and typically results in a more compact circuit board. In addition, chip carriers are available for further reduction in board space.

The Half-Power versions offer a choice of operating frequency, switching speeds, and power dissipation. In many cases, these Half-Power devices can result in significant power reduction from an overall system level.

The PAL16' M series is characterized for operation over the full military temperature range of –55°C to 125°C.

PAL is a registered trademark of Advanced Micro Devices Inc.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

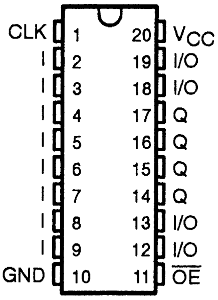
Copyright © 1992, Texas Instruments Incorporated

PAL16R4AM, PAL16R4A-2M, PAL16R6AM, PAL16R6A-2M, PAL16R8AM, PAL16R8A-2M STANDARD HIGH-SPEED *PAL*® CIRCUITS

SRPS016 – D2705, FEBRUARY 1984 – REVISED MARCH 1992

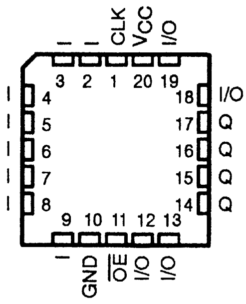
PAL16R4'
J OR W PACKAGE

(TOP VIEW)



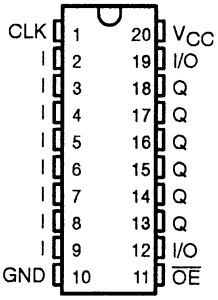
PAL16R4'
FK PACKAGE

(TOP VIEW)



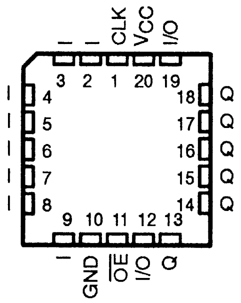
PAL16R6'
J OR W PACKAGE

(TOP VIEW)



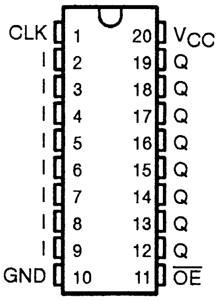
PAL16R6'
FK PACKAGE

(TOP VIEW)



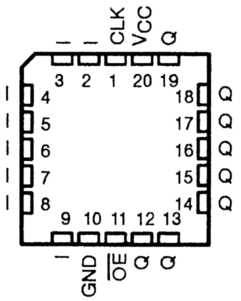
PAL16R8'
J OR W PACKAGE

(TOP VIEW)



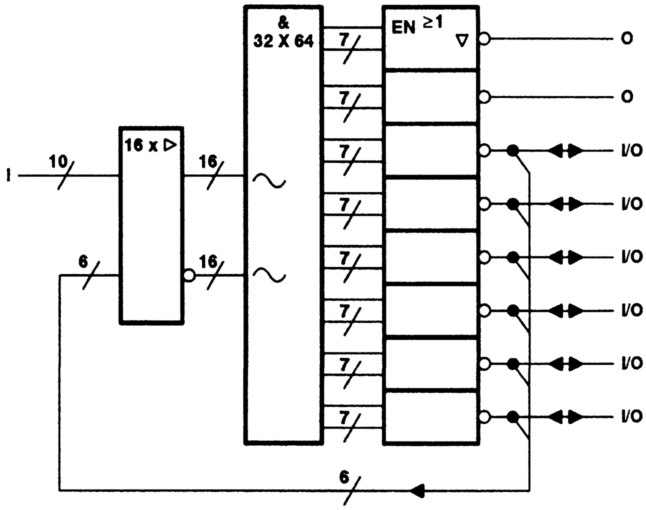
PAL16R8'
FK PACKAGE

(TOP VIEW)

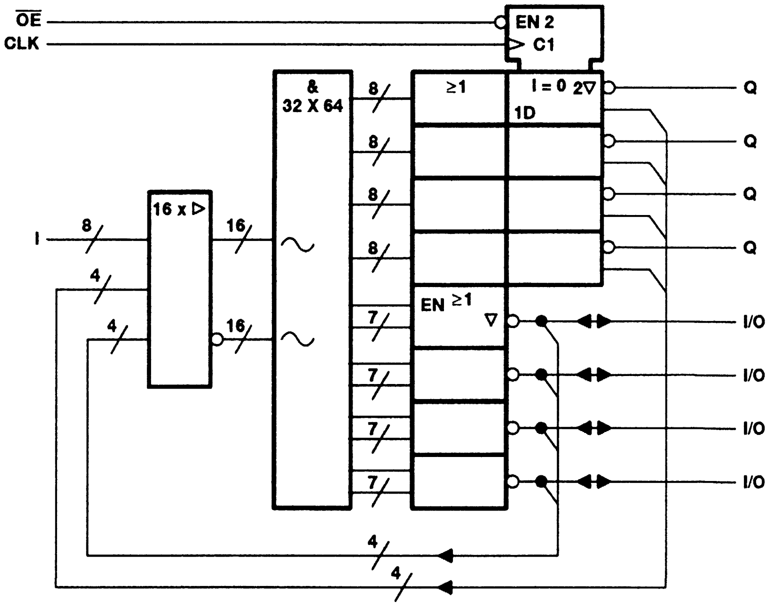


functional block diagrams (positive logic)

PAL16L8AM
PAL16L8A-2M



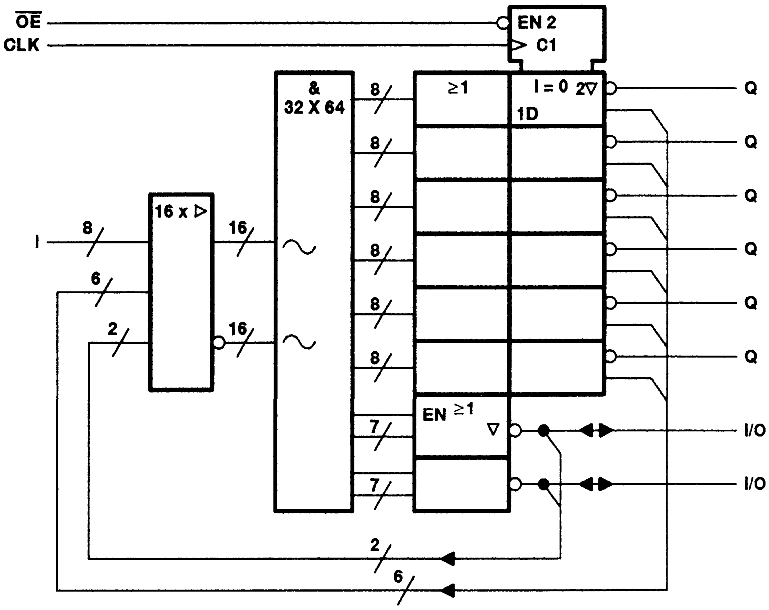
PAL16R4AM
PAL16R4A-2M



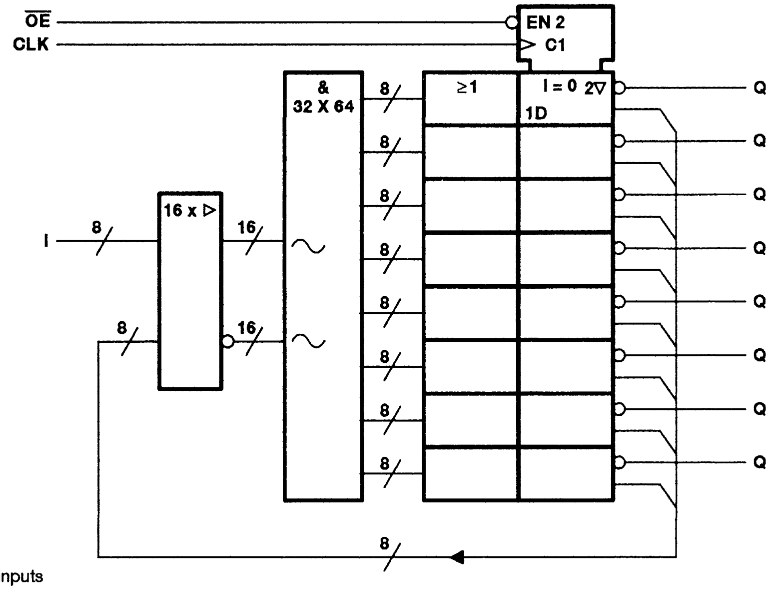
∿ denotes fused inputs

functional block diagrams (positive logic)

PAL16R6AM
PAL16R6A-2M

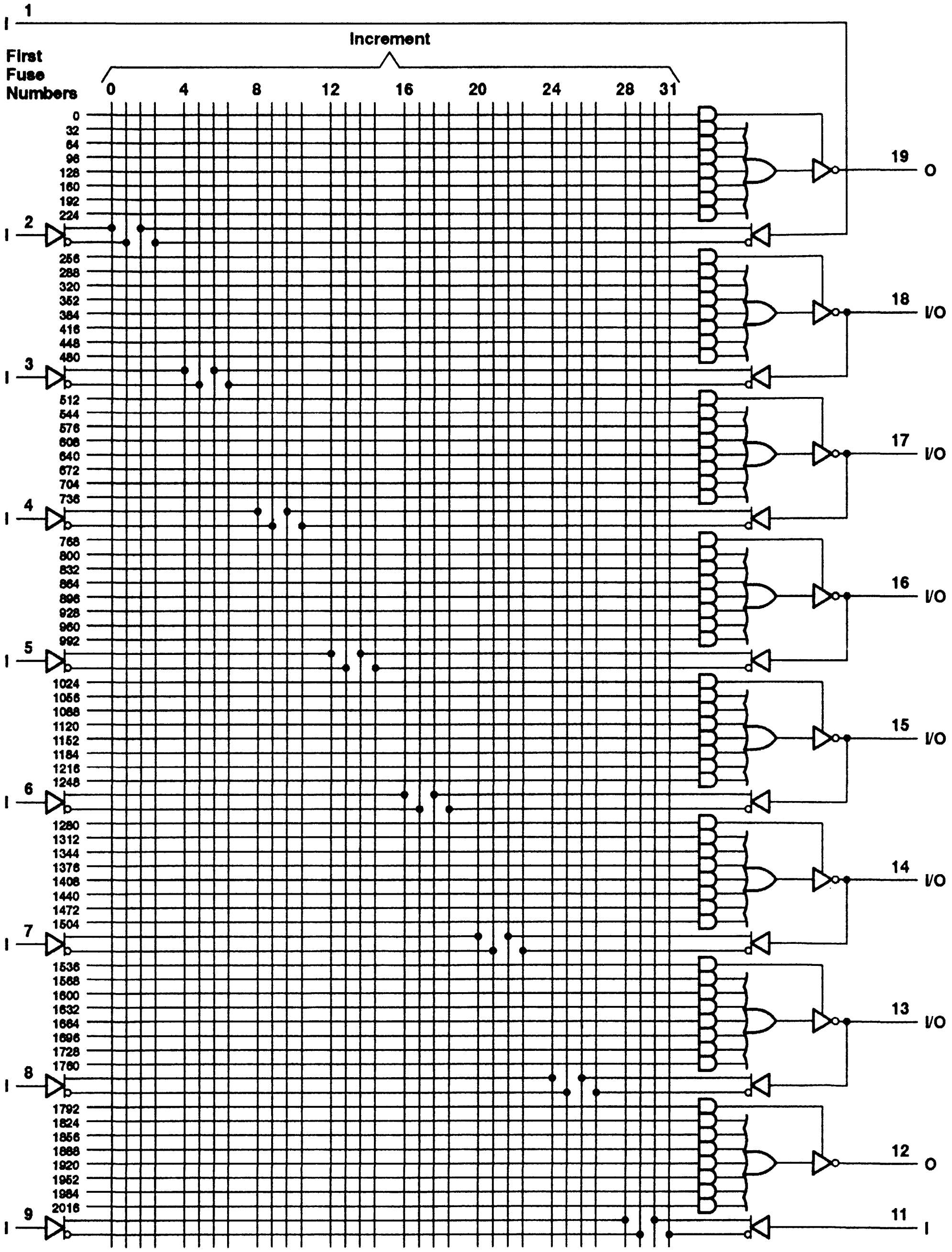


PAL16R8AM
PAL16R8A-2M



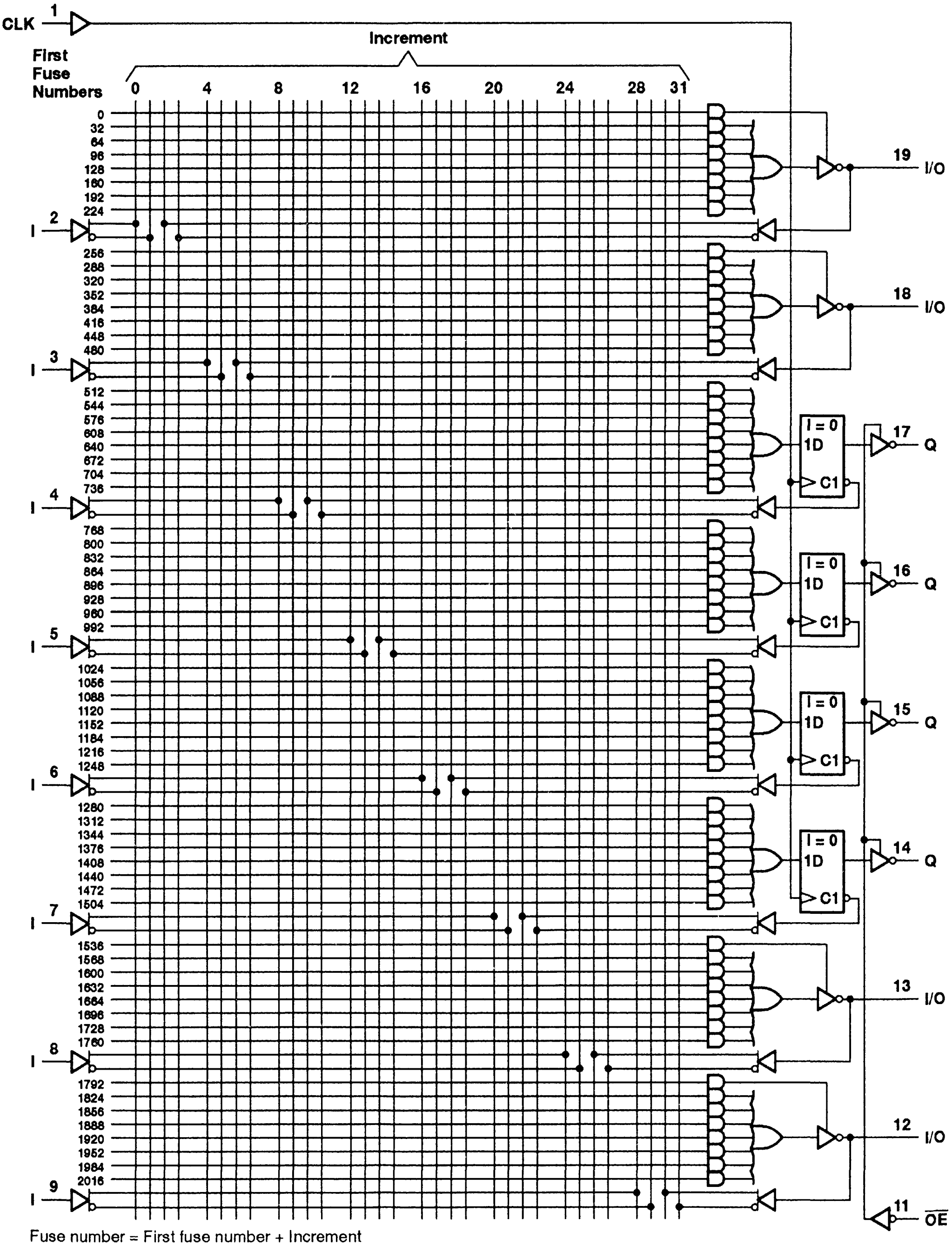
∿ denotes fused inputs

logic diagram (positive logic)



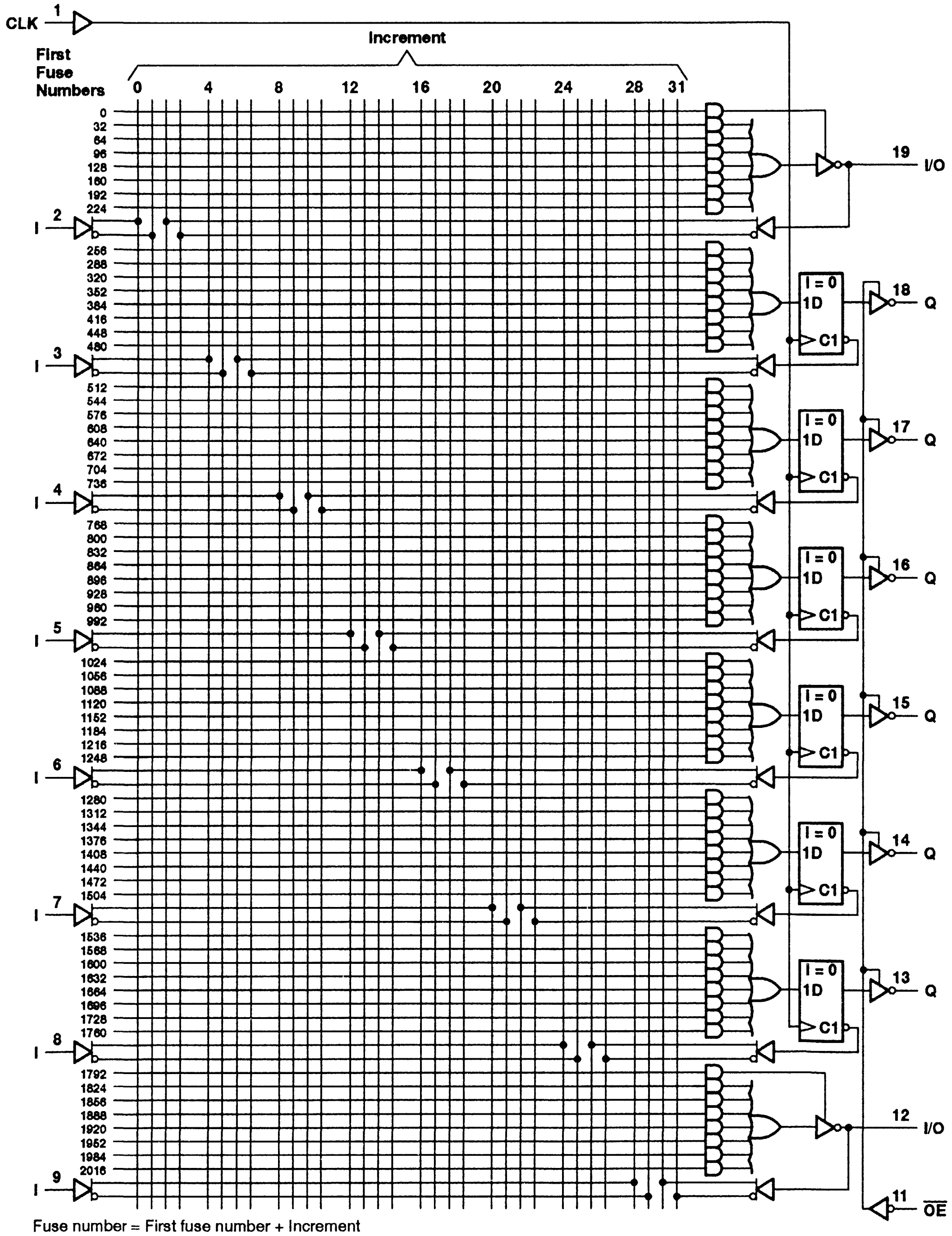
Fuse number = First fuse number + Increment

logic diagram (positive logic)



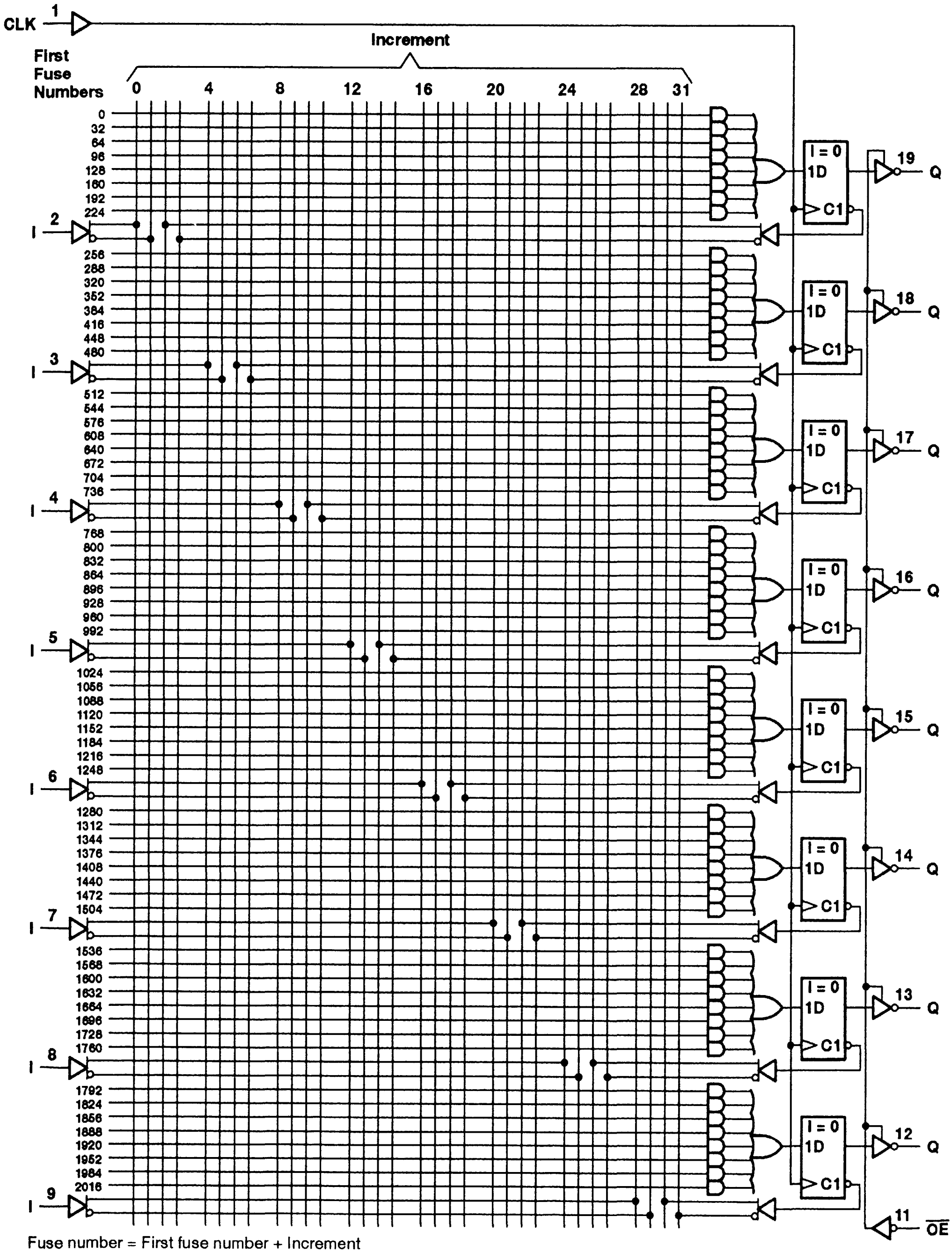
Fuse number = First fuse number + Increment

logic diagram (positive logic)



Fuse number = First fuse number + Increment

logic diagram (positive logic)



Fuse number = First fuse number + Increment

programming information

Texas Instruments programmable logic devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments programmable logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (see Note 1)	5.5 V
Voltage applied to disabled output (see Note 1)	5.5 V
Operating free-air temperature range	–55°C to 125°C
Storage temperature range	–65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.5	5	5.5	V
V_{IH}	High-level input voltage	2		5.5	V
V_{IL}	Low-level input voltage			0.8	V
I_{OH}	High-level output current			–2	mA
I_{OL}	Low-level output current			12	mA
T_A	Operating free-air temperature	–55	25	125	°C

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA				–1.5	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = –2 mA		2.4	3.2		V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA			0.25	0.4	V
I_{OZH}	Outputs	V_{CC} = 5.5 V,	V_O = 2.7 V				20	µA
	I/O ports						100	
I_{OZL}	Outputs	V_{CC} = 5.5 V,	V_O = 0.4 V				–20	µA
	I/O ports						–100	
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V				0.2	mA
I_{IH}	I/O Ports	V_{CC} = 5.5 V,	V_I = 2.7 V				100	µA
	All others						25	
I_{IL}	$\overline{OE}$ input	V_{CC} = 5.5 V,	V_I = 0.4 V				–0.2	mA
	All others						–0.1	
I_{OS}‡		V_{CC} = 5.5 V,	V_O = 0.5 V		–30		–250	mA
I_{CC}		V_{CC} = 5.5 V,	V_I = 0,	Outputs open		75	180	mA

timing requirements

			MIN	MAX	UNIT
f_{clock}	Clock Frequency		0	25	MHz
t_w	Pulse duration (see Note 2)	Clock high	15		ns
		Clock low	20		
t_{su}	Setup time, input or feedback before CLK↑		25		ns
t_h	Hold time, input or feedback after CLK↑		0		ns

NOTE 2: The total clock period of clock high and clock low must not exceed clock frequency, f_{clock}. The minimum pulse durations specified are only for clock high or low, but not for both simultaneously.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	TYP†	MAX	UNIT
f_{max}			R1 = 390 Ω, R2 = 750 Ω, See Figure 1	25	45		MHz
t_{pd}	I, I/O	O, I/O			15	30	ns
t_{pd}	CLK↑	Q			10	20	ns
t_{en}	$\overline{OE}$↓	Q			15	25	ns
t_{dis}	$\overline{OE}$↑	Q			10	25	ns
t_{en}	I, I/O	O, I/O			14	30	ns
t_{dis}	I, I/O	O, I/O			13	30	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second. Set V_O at 0.5 V to avoid test equipment degradation.

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.5	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −2 mA		2.4	3.2		V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA			0.25	0.4	V
I_{OZH}	Outputs	V_{CC} = 5.5 V,	V_O = 2.7 V				20	μA
	I/O ports						100	
I_{OZL}	Outputs	V_{CC} = 5.5 V,	V_O = 0.4 V				−20	μA
	I/O ports						−100	
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V				0.2	mA
I_{IH}	I/O Ports	V_{CC} = 5.5 V,	V_I = 2.7 V				100	μA
	All others						25	
I_{IL}	$\overline{OE}$ input	V_{CC} = 5.5 V,	V_I = 0.4 V				−0.2	mA
	All others						−0.1	
I_{OS}‡		V_{CC} = 5.5 V,	V_O = 0.5 V		−30		−250	mA
I_{CC}		V_{CC} = 5.5 V,	V_I = 0,	Outputs open		75	90	mA

timing requirements

			MIN	MAX	UNIT
f_{clock}	Clock Frequency		0	16	MHz
t_w	Pulse duration (see Note 2)	Clock high	25		ns
		Clock low	25		
t_{su}	Setup time, input or feedback before CLK↑		35		ns
t_h	Hold time, input or feedback after CLK↑		0		ns

NOTE 2: The total clock period of clock high and clock low must not exceed clock frequency, f_{clock}. The minimum pulse durations specified are only for clock high or low, but not for both simultaneously.

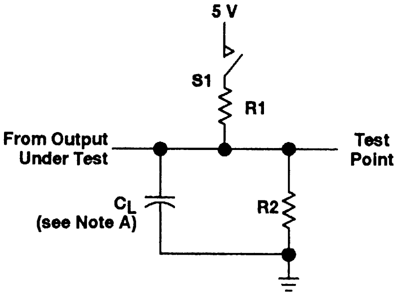
switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	TYP†	MAX	UNIT
f_{max}			R1 = 390 Ω, R2 = 750 Ω, See Figure 1	16	25		MHz
t_{pd}	I, I/O	O, I/O			25	40	ns
t_{pd}	CLK↑	Q			11	25	ns
t_{en}	$\overline{OE}$↓	Q			20	25	ns
t_{dis}	$\overline{OE}$↑	Q			11	25	ns
t_{en}	I, I/O	O, I/O			25	40	ns
t_{dis}	I, I/O	O, I/O			25	35	ns

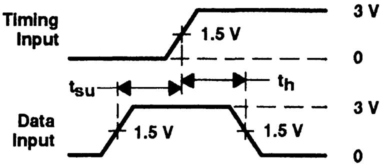
† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second. Set V_O at 0.5 V to avoid test equipment degradation.

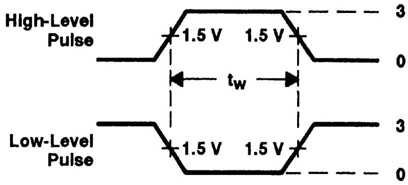
PARAMETER MEASUREMENT INFORMATION



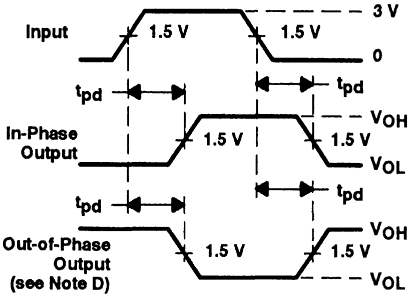
LOAD CIRCUIT FOR
3-STATE OUTPUTS



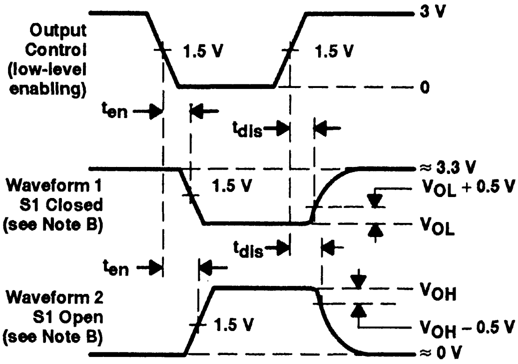
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 10 MHz, t_r and $t_f \leq 2$ ns, duty cycle = 50%
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.
E. Equivalent loads may be used for testing.

Figure 1. Load Circuit and Voltage Waveforms

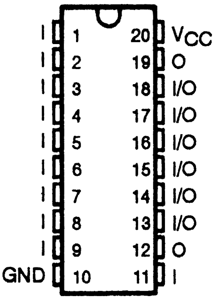
TIBPAL16L8-5C, TIBPAL16R4-5C, TIBPAL16R6-5C, TIBPAL16R8-5C
TIBPAL16L8-7M, TIBPAL16R4-7M, TIBPAL16R6-7M, TIBPAL16R8-7M
HIGH-PERFORMANCE *IMPACT-X*™ *PAL*® CIRCUITS

SRPS011D – D3359, OCTOBER 1989 – REVISED SEPTEMBER 1992

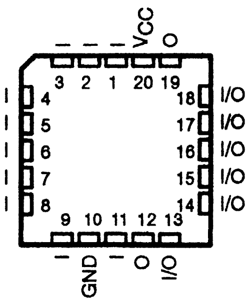
- **High-Performance Operation:**
  f_{max} (no feedback)
    TIBPAL16R' -5C Series . . . 125 MHz Min
    TIBPAL16R' -7M Series . . . 100 MHz Min
  f_{max} (internal feedback)
    TIBPAL16R' -5C Series . . . 125 MHz Min
    TIBPAL16R' -7M Series . . . 100 MHz Min
  f_{max} (external feedback)
    TIBPAL16R' -5C Series . . . 117 MHz Min
    TIBPAL16R' -7M Series . . . 74 MHz Min
  Propagation Delay
    TIBPAL16L8-5C Series . . . 5 ns Max
    TIBPAL16L8-7M Series . . . 7 ns Max
    TIBPAL16R' -5C Series
      (CLK-to-Q) . . . 4 ns Max
    TIBPAL16R' -7M Series
      (CLK-to-Q) . . . 6.5 ns Max
- **Functionally Equivalent, but Faster than, Existing 20-Pin PLDs**
- **Preload Capability on Output Registers Simplifies Testing**
- **Power-Up Clear on Registered Devices (All Register Outputs are Set Low, but Voltage Levels at the Output Pins Go High)**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Security Fuse Prevents Duplication**

DEVICE	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
'PAL16L8	10	2	0	6
'PAL16R4	8	0	4 (3-state buffers)	4
'PAL16R6	8	0	6 (3-state buffers)	2
'PAL16R8	8	0	8 (3-state buffers)	0

TIBPAL16L8'
C SUFFIX . . . J OR N PACKAGE
M SUFFIX . . . J PACKAGE
(TOP VIEW)



TIBPAL16L8'
C SUFFIX . . . FN PACKAGE
M SUFFIX . . . FK PACKAGE
(TOP VIEW)



Pin assignments in operating mode

description

These programmable array logic devices feature high speed and functional equivalency when compared with currently available devices. These IMPACT-X™ circuits combine the latest Advanced Low-Power Schottky technology with proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional TTL logic. Their easy programmability allows for quick design of custom functions and typically results in a more compact circuit board.

The TIBPAL16' C series is characterized from 0°C to 75°C. The TIBPAL16' M series is characterized for operation over the full military temperature range of –55°C to 125°C.

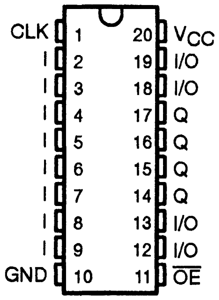
These devices are covered by U.S. Patent 4,410,987.
IMPACT-X is a trademark of Texas Instruments Incorporated.
PAL is a registered trademark of Advanced Micro Devices Inc.

This document contains information on products in more than one phase of development. The status of each device is indicated on the page(s) specifying its electrical characteristics.

Copyright © 1992, Texas Instruments Incorporated

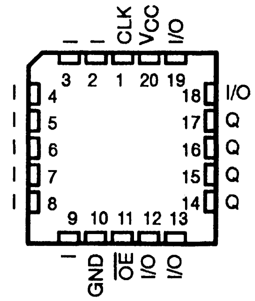
TIBPAL16R4'
C SUFFIX . . . J OR N PACKAGE
M SUFFIX . . . J PACKAGE

(TOP VIEW)



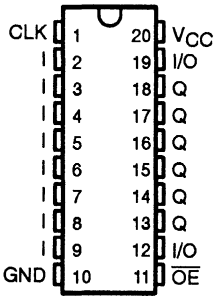
TIBPAL16R4'
C SUFFIX . . . FN PACKAGE
M SUFFIX . . . FK PACKAGE

(TOP VIEW)



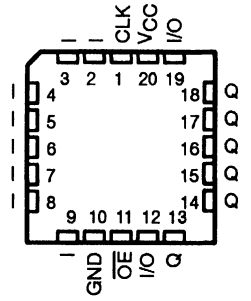
TIBPAL16R6'
C SUFFIX . . . J OR N PACKAGE
M SUFFIX . . . J PACKAGE

(TOP VIEW)



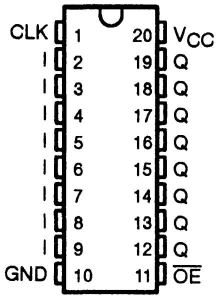
TIBPAL16R6'
C SUFFIX . . . FN PACKAGE
M SUFFIX . . . FK PACKAGE

(TOP VIEW)



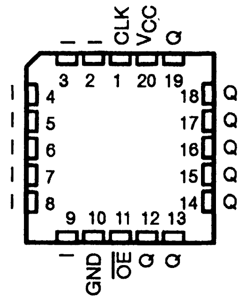
TIBPAL16R8'
C SUFFIX . . . J OR N PACKAGE
M SUFFIX . . . J PACKAGE

(TOP VIEW)



TIBPAL16R8'
C SUFFIX . . . FN PACKAGE
M SUFFIX . . . FK PACKAGE

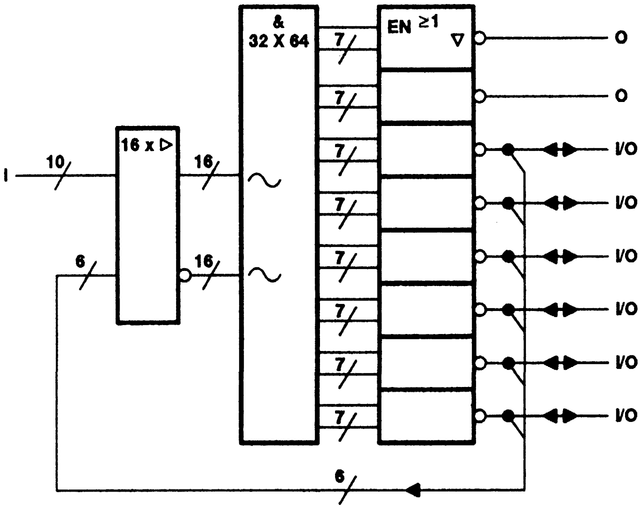
(TOP VIEW)



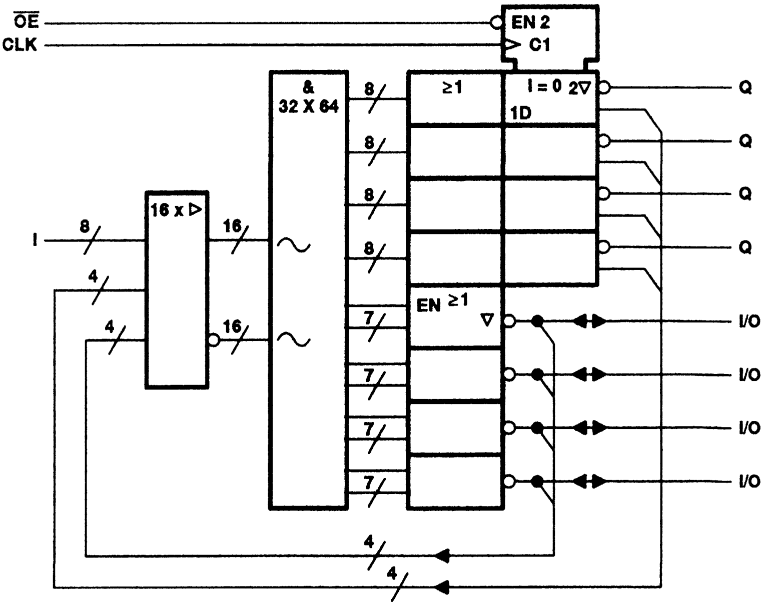
Pin assignments in operating mode

functional block diagrams (positive logic)

TIBPAL16L8'



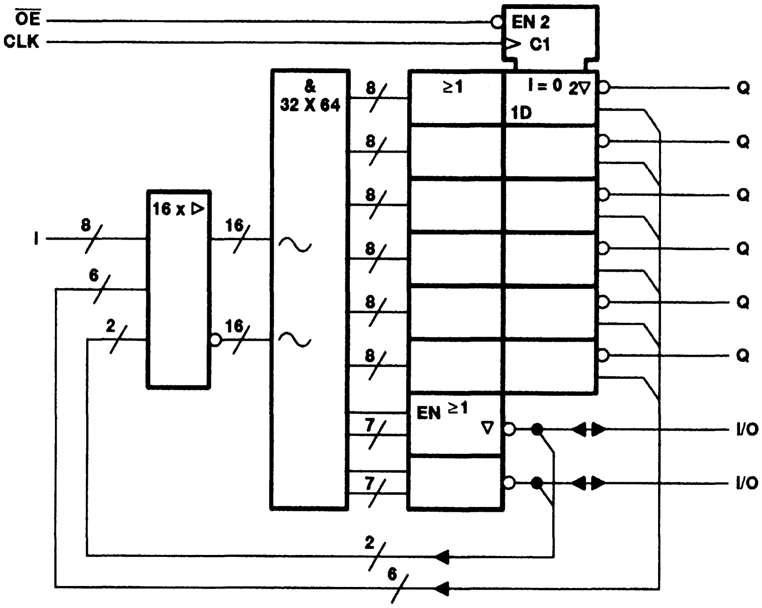
TIBPAL16R4'



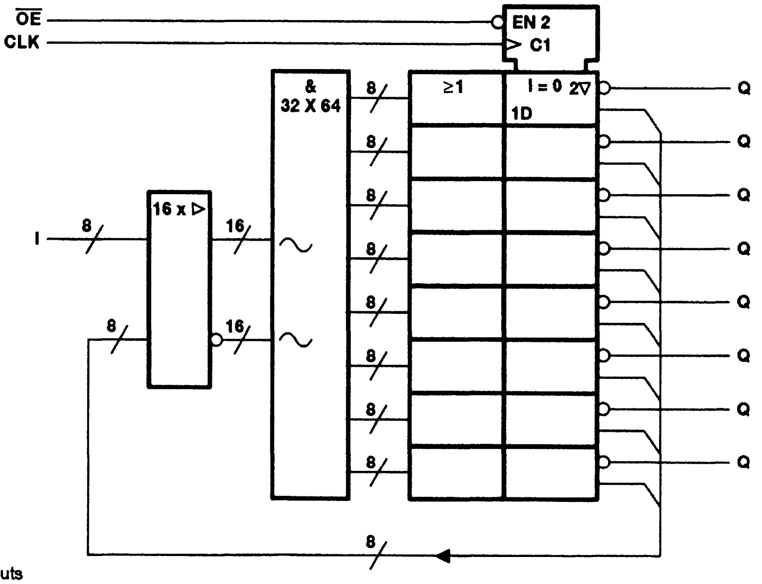
∿ denotes fused inputs

functional block diagrams (positive logic)

TIBPAL16R6'

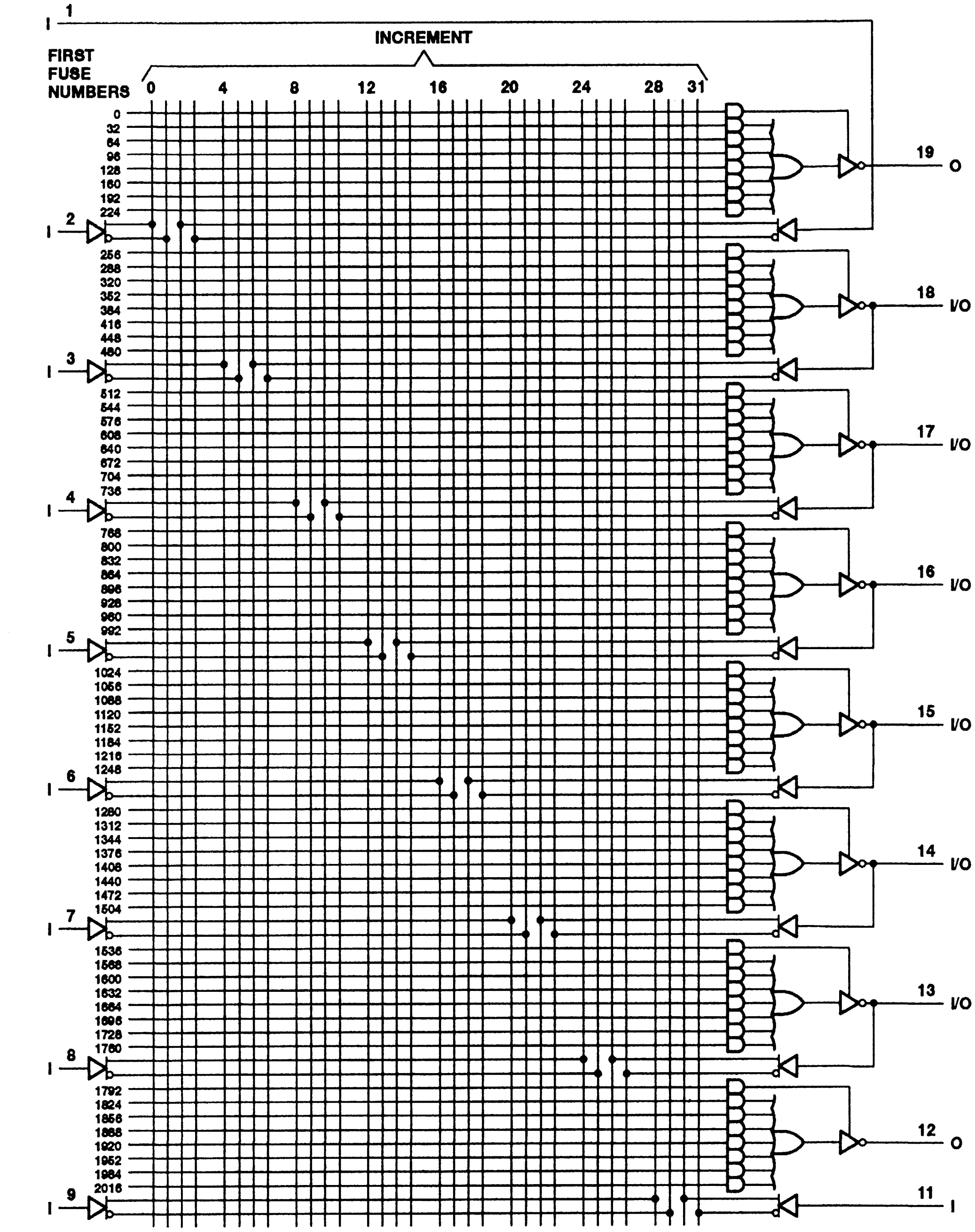


TIBPAL16R8'



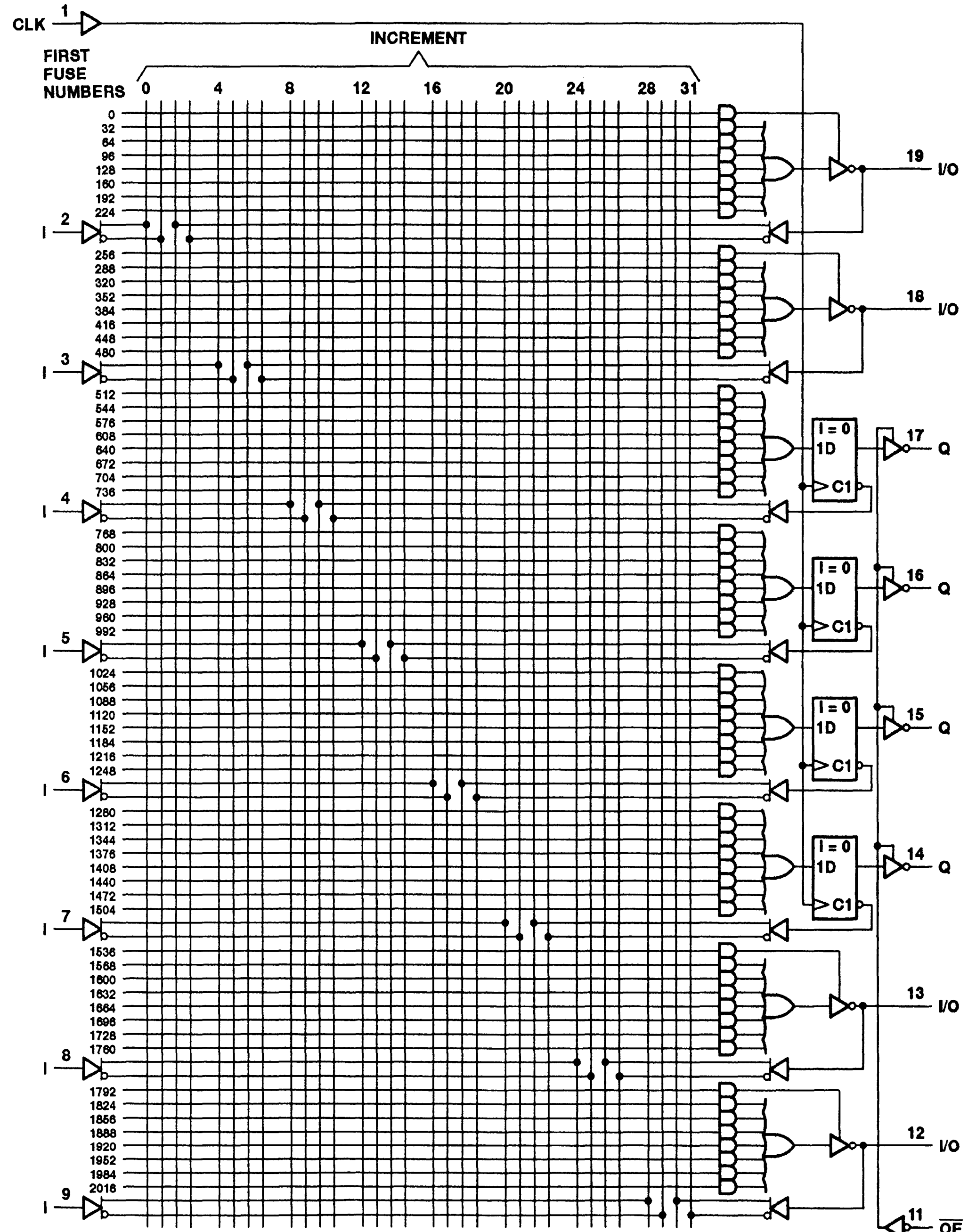
∿ denotes fused inputs

logic diagram (positive logic)



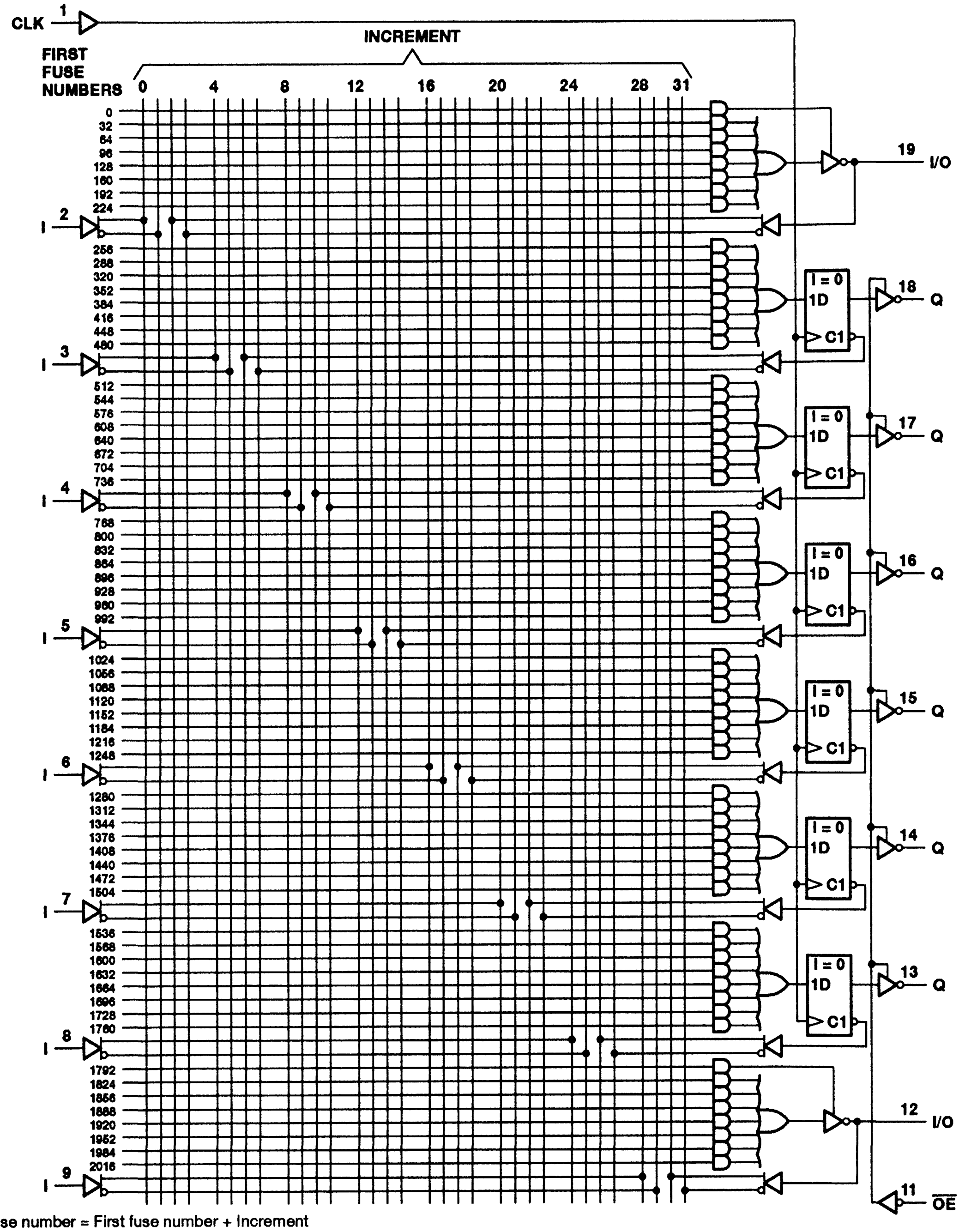
Fuse number = First fuse number + Increment

logic diagram (positive logic)



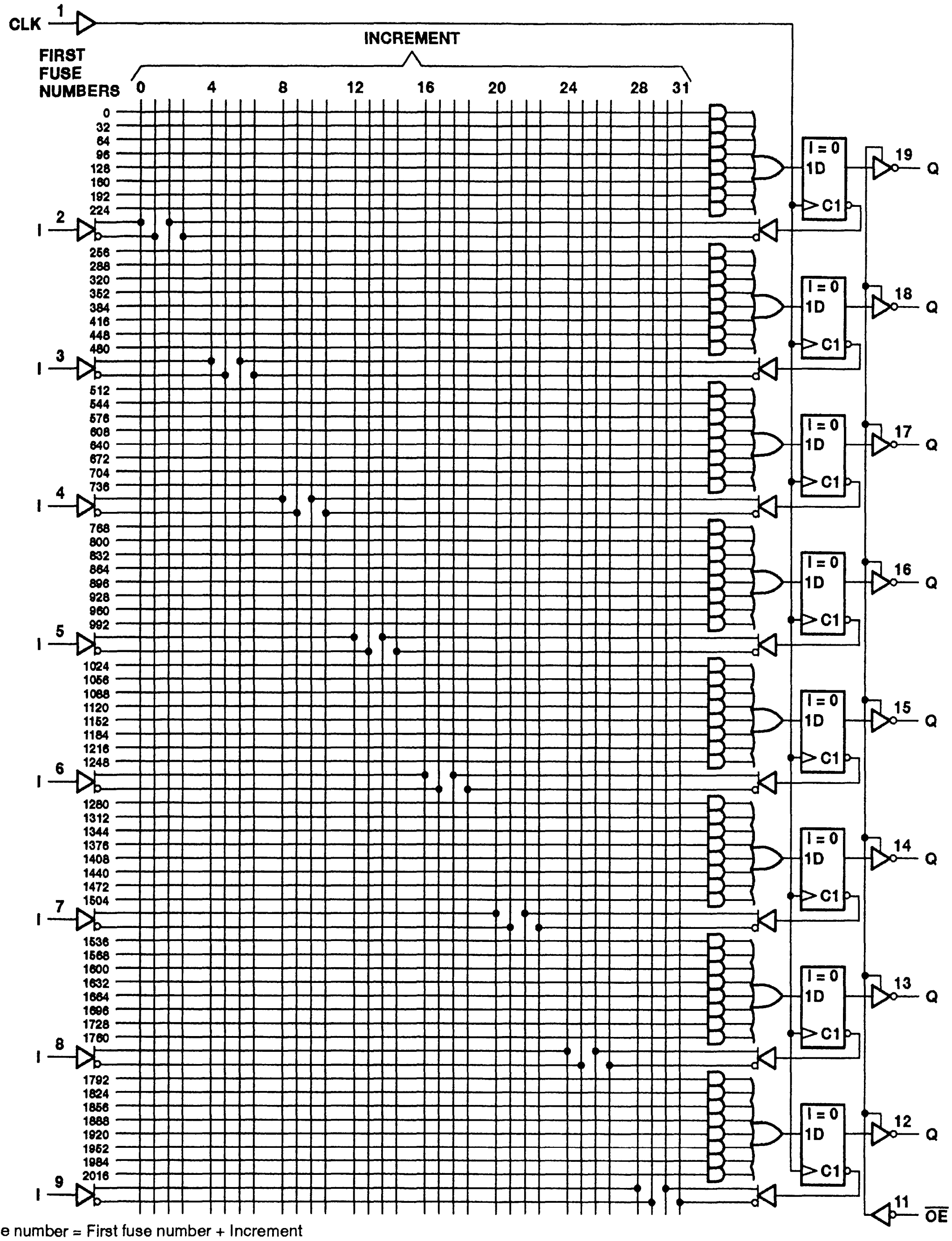
Fuse number = First fuse number + Increment

logic diagram (positive logic)



Fuse number = First fuse number + Increment

logic diagram (positive logic)



Fuse number = First fuse number + Increment

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (see Note 1)	5.5 V
Voltage applied to disabled output (see Note 1)	5.5 V
Operating free-air temperature range	0°C to 75°C
Storage temperature range	–65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle or during a preload cycle.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IH}	High-level input voltage (see Note 2)	2		5.5	V
V_{IL}	Low-level input voltage (see Note 2)			0.8	V
I_{OH}	High-level output current			–3.2	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature	0	25	75	°C

NOTE 2: These are absolute voltage levels with respect to the ground pin of the device and include all overshoots due to system and/or tester noise. Testing these parameters should not be attempted without suitable equipment.

electrical characteristics over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.75 V,	I_I = –18 mA			–0.8	–1.5	V
V_{OH}	V_{CC} = 4.75 V,	I_{OH} = –3.2 mA		2.4	2.7		V
V_{OL}	V_{CC} = 4.75 V,	I_{OL} = 24 mA			0.3	0.5	V
I_{OZH}‡	V_{CC} = 5.25 V,	V_O = 2.7 V				100	µA
I_{OZL}‡	V_{CC} = 5.25 V,	V_O = 0.4 V				–100	µA
I_I	V_{CC} = 5.25 V,	V_I = 5.5 V				100	µA
I_{IH}‡	V_{CC} = 5.25 V,	V_I = 2.7 V				25	µA
I_{IL}‡	V_{CC} = 5.25 V,	V_I = 0.4 V				–250	µA
I_{OS}§	V_{CC} = 5.25 V,	V_O = 0.5 V		–30	–70	–130	mA
I_{CC}	V_{CC} = 5.25 V,	V_I = 0,	Outputs open			180	mA
C_i	f = 1 MHz,	V_I = 2 V			8.5		pF
C_o	f = 1 MHz,	V_O = 2 V			10		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ I/O leakage is the worst case of I_{OZL} and I_{IL} or I_{OZH} and I_{IH}, respectively.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second. V_O is set at 0.5 V to avoid test problems caused by test equipment ground degradation.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		TEST CONDITIONS	TIBPAL16L8-5CFN		TIBPAL16L8-5CJ TIBPAL16L8-5CN		UNIT
					MIN	MAX	MIN	MAX	
t_{pd}	I, I/O	O, I/O	with up to 4 outputs switching	R1 = 200 Ω, R2 = 200 Ω, See Figure 8	1.5	5	1.5	5	ns
	I, I/O	O, I/O	with more than 4 outputs switching		1.5	5	1.5	5.5	
t_{en}	I, I/O	O, I/O			2	7	2	7	ns
t_{dis}	I, I/O	O, I/O			2	7	2	7	ns

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) .... 7 V
Input voltage (see Note 1) .... 5.5 V
Voltage applied to disabled output (see Note 1) .... 5.5 V
Operating free-air temperature range .... 0°C to 75°C
Storage temperature range .... –65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle or during a preload cycle.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage (see Note 2)		2		5.5	V
V_{IL}	Low-level input voltage (see Note 2)				0.8	V
I_{OH}	High-level output current				–3.2	mA
I_{OL}	Low-level output current				24	mA
f_{clock}	Clock frequency		0		125	MHz
t_w	Pulse duration, clock	High	4			ns
		Low	4			
t_{su}	Setup time, input or feedback before clock↑		4.5			ns
t_h	Hold time, input or feedback after clock↑		0			ns
T_A	Operating free-air temperature		0	25	75	°C

NOTE 2: These are absolute voltage levels with respect to the ground pin of the device and include all overshoots due to system and/or tester noise. Testing these parameters should not be attempted without suitable equipment.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.75 V, I_I = –18 mA		–0.8	–1.5	V
V_{OH}		V_{CC} = 4.75 V, I_{OH} = –3.2 mA	2.4	2.7		V
V_{OL}		V_{CC} = 4.75 V, I_{OL} = 24 mA		0.3	0.5	V
I_{OZH}‡		V_{CC} = 5.25 V, V_O = 2.7 V			100	µA
I_{OZL}‡		V_{CC} = 5.25 V, V_O = 0.4 V			–100	µA
I_I		V_{CC} = 5.25 V, V_I = 5.5 V			100	µA
I_{IH}‡		V_{CC} = 5.25 V, V_I = 2.7 V			25	µA
I_{IL}‡		V_{CC} = 5.25 V, V_I = 0.4 V			–250	µA
I_{OS}§		V_{CC} = 5.25 V, V_O = 0.5 V	–30	–70	–130	mA
I_{CC}		V_{CC} = 5.25 V, V_I = 0, Outputs open			200	mA
C_i	I	f = 1 MHz, V_I = 2 V		7		pF
	CLK/$\overline{OE}$			5		
C_o	I/O	f = 1 MHz, V_O = 2 V		10		pF
	Q			7		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TIBPAL16R4-5CFN TIBPAL16R6-5CFN			TIBPAL16R4-5CJ TIBPAL16R6-5CJ TIBPAL16R4-5CN TIBPAL16R6-5CN			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}¶	without feedback		R1 = 200 Ω, R2 = 200 Ω, See Figure 8	125			125			MHz
	with internal feedback (counter configuration)			125			125			
	with external feedback			117			111			
t_{pd}	CLK↑	Q		1.5		4	1.5		4.5	ns
t_{pd}	CLK↑	Internal feedback				3.5			3.5	ns
t_{pd}	I, I/O	I/O		1.5		5	1.5		5	ns
t_{en}	$\overline{OE}$↓	Q		1.5		6	1.5		6	ns
t_{dis}	$\overline{OE}$↑	Q		1		6.5	1		7	ns
t_{en}	I, I/O	I/O		2		7	2		7	ns
t_{dis}	I, I/O	I/O		2		7	2		7	ns
t_r					1.5			1.5		ns
t_f					1.5			1.5		ns
$t_{sk(o)}$#	Skew between registered outputs				0.5			0.5		ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ I/O leakage is the worst case of I_{OZL} and I_{IL} or I_{OZH} and I_{IH}, respectively.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second. V_O is set at 0.5 V to avoid test problems caused by test equipment ground degradation.

¶ See 'f_{max} Specification' near the end of this data sheet.

\# $t_{sk(o)}$ is the skew time between registered outputs.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (see Note 1)	5.5 V
Voltage applied to disabled output (see Note 1)	5.5 V
Operating free-air temperature range	0°C to 75°C
Storage temperature range	–65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle or during a preload cycle.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage (see Note 2)		2		5.5	V
V_{IL}	Low-level input voltage (see Note 2)				0.8	V
I_{OH}	High-level output current				–3.2	mA
I_{OL}	Low-level output current				24	mA
f_{clock}	Clock frequency		0		125	MHz
t_w	Pulse duration, clock	High	4			ns
		Low	4			
t_{su}	Setup time, input or feedback before clock↑		4.5			ns
t_h	Hold time, input or feedback after clock↑		0			ns
T_A	Operating free-air temperature		0	25	75	°C

NOTE 2: These are absolute voltage levels with respect to the ground pin of the device and include all overshoots due to system and/or tester noise. Testing these parameters should not be attempted without suitable equipment.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		TIBPAL16R8-5CFN			TIBPAL16R8-5CJ TIBPAL16R8-5CN			UNIT
				MIN	TYP[†]	MAX	MIN	TYP[†]	MAX	
V_{IK}		V_{CC} = 4.75 V,	I_I = –18 mA		–0.8	–1.5		–0.8	–1.5	V
V_{OH}		V_{CC} = 4.75 V,	I_{OH} = –3.2 mA	2.4	2.7		2.4	2.7		V
V_{OL}		V_{CC} = 4.75 V,	I_{OL} = 24 mA		0.3	0.5		0.3	0.5	V
I_{OZH}		V_{CC} = 5.25 V,	V_O = 2.7 V			100			100	µA
I_{OZL}		V_{CC} = 5.25 V,	V_O = 0.4 V			–100			–100	µA
I_I		V_{CC} = 5.25 V,	V_I = 5.5 V			100			100	µA
I_{IH}		V_{CC} = 5.25 V,	V_I = 2.7 V			25			25	µA
I_{IL}		V_{CC} = 5.25 V,	V_I = 0.4 V			–250			–250	µA
I_{OS}[‡]		V_{CC} = 5.25 V,	V_O = 0.5 V	–30	–70	–130	–30	–70	–130	mA
I_{CC}		V_{CC} = 5.25 V,	V_I = 0, Outputs open			180			180	mA
C_i	I	f = 1 MHz,	V_I = 2 V		8.5			6.5		pF
	CLK/$\overline{\mathrm{OE}}$				7.5			5.5		
C_o		f = 1 MHz,	V_O = 2 V		10			8		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		TEST CONDITIONS	TIBPAL16R8-5CFN			TIBPAL16R8-5CJ TIBPAL16R8-5CN			UNIT
					MIN	TYP[†]	MAX	MIN	TYP[†]	MAX	
f_{max}[§]	without feedback			R1 = 200 Ω, R2 = 200 Ω, See Figure 8	125			125			MHz
	with internal feedback (counter configuration)				125			125			
	with external feedback				117			111			
t_{pd}	CLK↑	Q	with up to 4 outputs switching		1.5		4	1.5		4	ns
	CLK↑	Q	with more than 4 outputs switching		1.5		4	1.5		4.5	
t_{pd}[¶]	CLK↑	Internal feedback					3.5			3.5	ns
t_{en}	$\overline{\mathrm{OE}}$↓	Q			1.5		6	1.5		6	ns
t_{dis}	$\overline{\mathrm{OE}}$↑	Q			1		6.5	1		7	ns
t_r						1.5			1.5		ns
t_f						1.5			1.5		ns
$t_{sk(o)}$[#]	Skew between outputs					0.5			0.5		ns

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[‡] Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second. V_O is set at 0.5 V to avoid test problems caused by test equipment ground degradation.

[§] See 'f_{max} Specification' near the end of this data sheet.

[¶] This parameter is calculated from the measured f_{max} with internal feedback in a counter configuration (see Figure 2 for illustration).

[#] $t_{sk(o)}$ is the skew time between registered outputs.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) .... 7 V
Input voltage (see Note 1) .... 5.5 V
Voltage applied to disabled output (see Note 1) .... 5.5 V
Operating free-air temperature range .... –55°C to 125°C
Storage temperature range .... –65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle or during a preload cycle.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage (see Note 2)		2		5.5	V
V_{IL}	Low-level input voltage (see Note 2)				0.8	V
I_{OH}	High-level output current				–2	mA
I_{OL}	Low-level output current				12	mA
f_{clock}†	Clock frequency		0		100	MHz
t_w†	Pulse duration, clock	High	5			ns
		Low	5			
t_{su}†	Setup time, input or feedback before clock↑		7			ns
t_h†	Hold time, input or feedback after clock↑		0			ns
T_A	Operating free-air temperature		–55	25	125	°C

† f_{clock}, t_w, t_{su}, and t_h do not apply to TIBPAL16L8'

NOTE 2: These are absolute voltage levels with respect to the ground pin of the device and include all overshoots due to system and/or tester noise. Testing these parameters should not be attempted without suitable equipment.

PRODUCT PREVIEW

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

TEXAS INSTRUMENTS

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA			–0.8	–1.5	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = –2 mA		2.4	2.7		V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA			0.25	0.5	V
I_{OZH}	0, Q outputs	V_{CC} = 5.5 V,	V_O = 2.7 V				20	μA
	I/O ports						100	
I_{OZL}	0, Q outputs	V_{CC} = 5.5 V,	V_O = 0.4 V				–20	μA
	I/O ports						–250	
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V				1	mA
I_{IH}	I/O ports	V_{CC} = 5.5 V,	V_I = 2.7 V				100	μA
	All others						25	
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V				–250	μA
I_{OS}‡		V_{CC} = 5.5 V,	V_O = 0.5 V		–30	–70	–130	mA
I_{CC}		V_{CC} = 5.5 V,	V_I = GND,	$\overline{OE}$ = V_{IH}, Outputs open			210	mA
C_i	I	f = 1 MHz,	V_I = 2 V			8.5		pF
	CLK/$\overline{OE}$					7.5		
C_o		f = 1 MHz,	V_O = 2 V			10		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second. V_O is set at 0.5 V to avoid test problems caused by test equipment ground degradation.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	MAX	UNIT
f_{max}§	without feedback		R1 = 390 Ω, R2 = 750 Ω, See Figure 8	100		MHz
	with internal feedback (counter configuration)			100		
	with external feedback			74		
t_{pd}	I, I/O	O, I/O		1	7	ns
t_{pd}	CLK	Q		1	7	ns
t_{en}	OE↓	Q		1	8	ns
t_{dis}	OE↑	Q		1	10	ns
t_{en}	I, I/O	O, I/O		1	9	ns
t_{dis}	I, I/O	O, I/O		1	10	ns

§ See 'f_{max} Specification' near the end of this data sheet. f_{max} does not apply for TIBPAL16L8'. f_{max} with external feedback is not production tested and is calculated from the equation located in the f_{max} specifications section.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

programming information

Texas Instruments programmable logic devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments programmable logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

asynchronous preload procedure for registered outputs (see Figure 1 and Note 3)†

The output registers can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below.

Step 1. With V_{CC} at 5 volts and Pin 1 at V_{IL}, raise Pin 11 to V_{IHH}.
Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.
Step 3. Lower Pin 11 to 5 V.
Step 4. Remove output voltage, then lower Pin 11 to V_{IL}. Preload can be verified by observing the voltage level at the output pin.

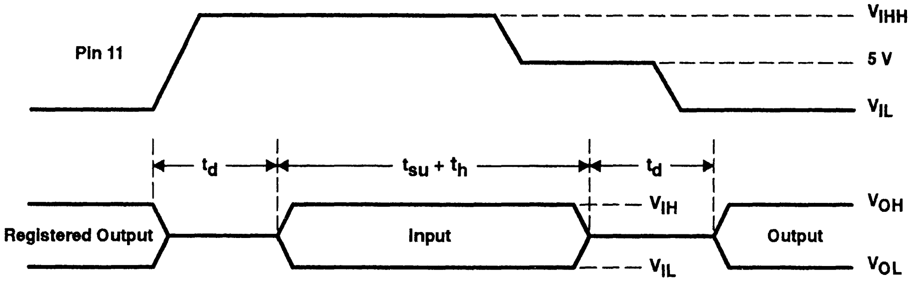


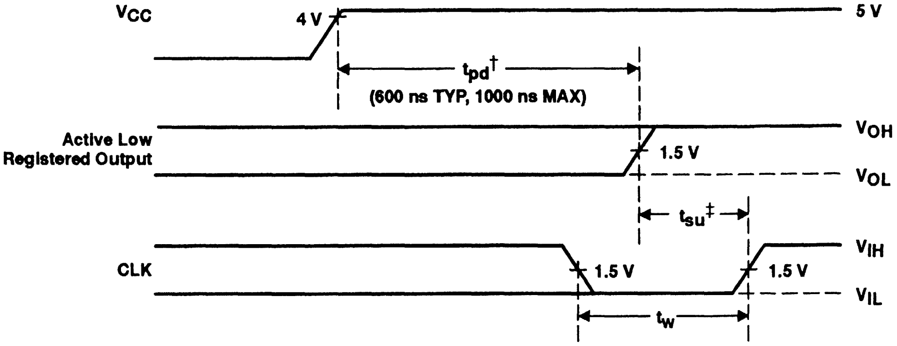
Figure 1. Asynchronous Preload Waveforms †

---

† Not applicable for TIBPAL16L8-5C and TIBPAL16L8-7M.
NOTE 3: $t_d = t_{su} = t_h$ = 100 ns to 1000 ns
V_{IHH} = 10.25 V to 10.75 V

power-up reset (see Figure 2)

Following power up, all registers are reset to zero. This feature provides extra flexibility to the system designer and is especially valuable in simplifying state-machine initialization. To ensure a valid power-up reset, it is important that the rise of V_{CC} be monotonic. Following power-up reset, a low-to-high clock transition must not occur until all applicable input and feedback setup times are met.



† This is the power-up reset time and applies to registered outputs only. The values shown are from characterization data.
‡ This is the setup time for input or feedback.

Figure 2. Power-Up Reset Waveforms

f_{max} SPECIFICATIONS

f_{max} without feedback (see Figure 3)

In this mode, data is presented at the input to the flip-flop and clocked through to the Q output with no feedback. Under this condition, the clock period is limited by the sum of the data setup time and the data hold time ($t_{su} + t_h$). However, the minimum fmax is determined by the minimum clock period (t_w high + t_w low).

$$\text{Thus, fmax without feedback} = \frac{1}{(t_w\text{high} + t_w\text{low})} \text{ or } \frac{1}{(t_{su} + t_h)}.$$

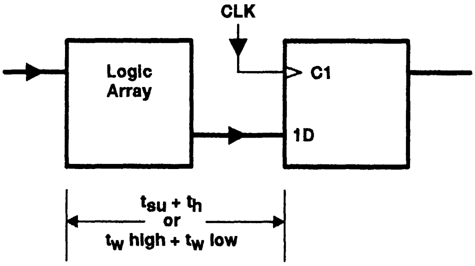


Figure 3. f_{max} Without Feedback

f_{max} with internal feedback (see Figure 4)

This configuration is most popular in counters and on-chip state-machine designs. The flip-flop inputs are defined by the device inputs and flip-flop outputs. Under this condition, the period is limited by the internal delay from the flip-flop outputs through the internal feedback and logic array to the inputs of the next flip-flop.

$$\text{Thus, fmax with internal feedback} = \frac{1}{(t_{su} + t_{pd}\ \text{CLK} - \text{to} - \text{FB})}.$$

Where tpd CLK-to-FB is the deduced value of the delay from CLK to the input of the logic array.

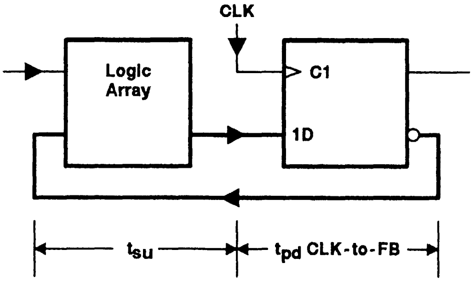


Figure 4. f_{max} With Internal Feedback

f_{max} SPECIFICATIONS

f_{max} with external feedback (see Figure 5)

This configuration is a typical state-machine design with feedback signals sent off-chip. This external feedback could go back to the device inputs or to a second device in a multi-chip state machine. The slowest path defining the period is the sum of the clock-to-output time and the input setup time for the external signals (t_{su} + t_{pd} CLK-to-Q).

Thus, f_{max} with external feedback $= \dfrac{1}{(t_{su} + t_{pd}\ \text{CLK}-\text{to}-\text{Q})}$.

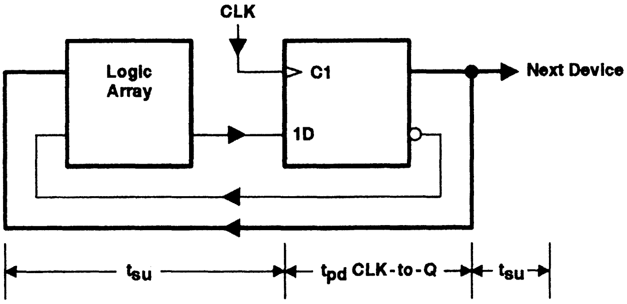


Figure 5. f_{max} With External Feedback

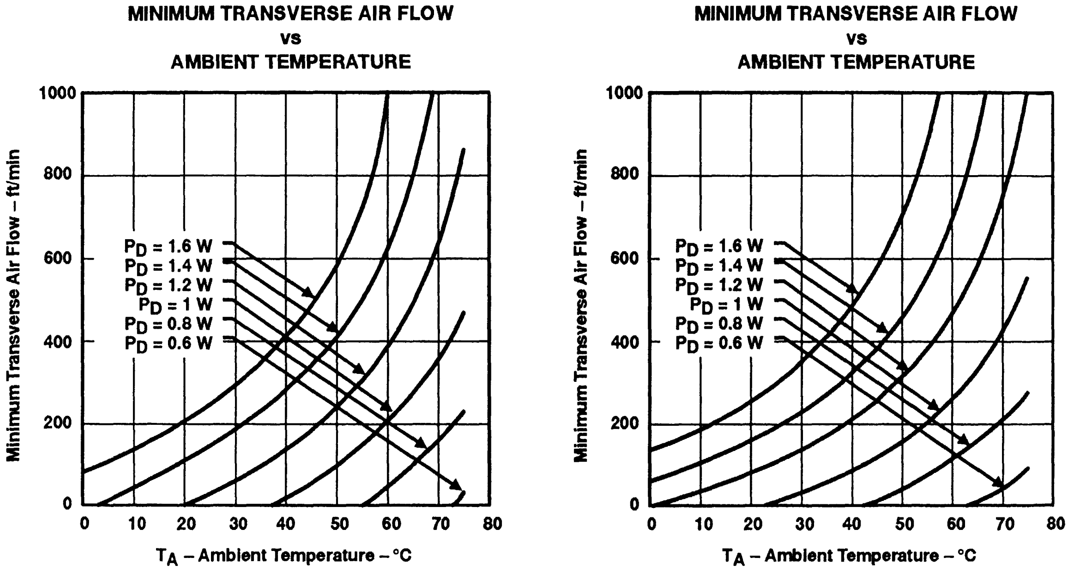
THERMAL INFORMATION

thermal management of the TIBPAL16R8-5C

Thermal management of the TIBPAL16R8-5CN and TIBPAL16R8-5CFN is necessary when operating at certain conditions of frequency, output loading, and outputs switching simultaneously. The device and system application will determine the appropriate level of management.

Determining the level of thermal management is based on factors such as power dissipation (P_D), ambient temperature (T_A), and transverse airflow (FPM). Figures 6 (a) and 6 (b) show the relationship between ambient temperature and transverse airflow at given power dissipation levels. The required transverse airflow can be determined at a particular ambient temperature and device power dissipation level in order to ensure the device specifications.

Figure 7 illustrates how power dissipation varies as a function of frequency and the number of outputs switching simultaneously. It should be noted that all outputs are fully loaded (C_L = 50 pF). Since the condition of eight fully loaded outputs represents the worst-case condition, each application must be evaluated accordingly.



(a) TIBPAL16R8-5CN

(b) TIBPAL16R8-5CFN

Figure 6

THERMAL INFORMATION

POWER DISSIPATION vs FREQUENCY

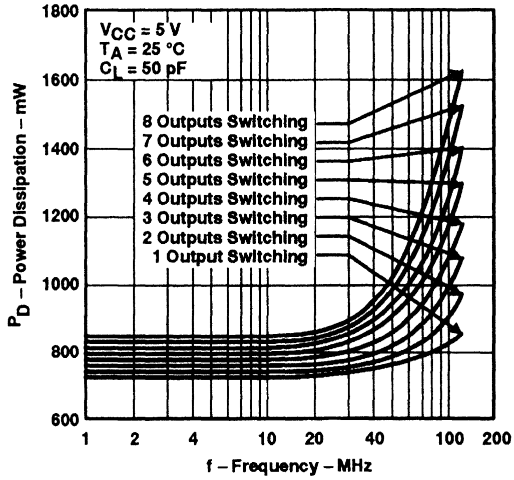
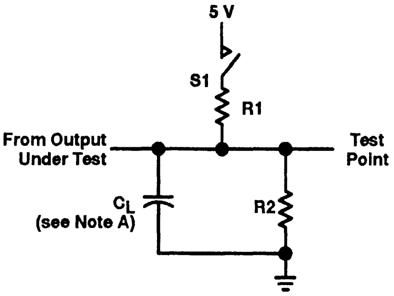
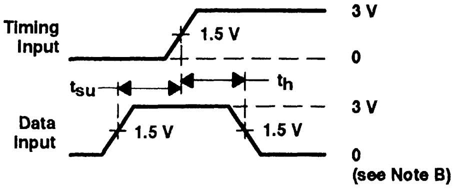


Figure 7

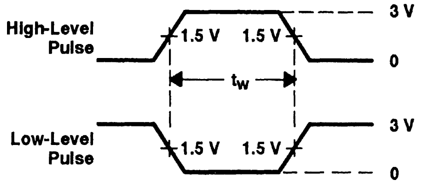
PARAMETER MEASUREMENT INFORMATION



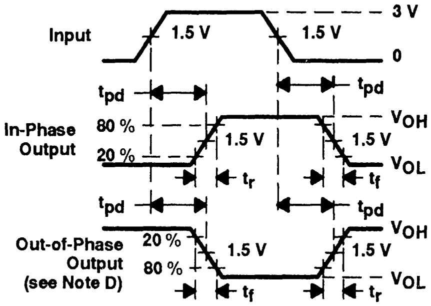
**LOAD CIRCUIT FOR
3-STATE OUTPUTS**



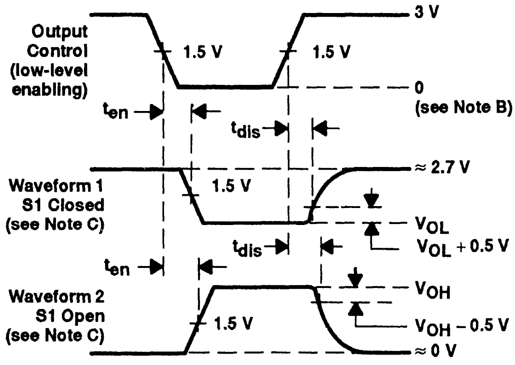
**VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES**



**VOLTAGE WAVEFORMS
PULSE DURATIONS**



**VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES**



**VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS**

NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
B. All input pulses have the following characteristics: For C suffix, PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%; For M suffix, PRR ≤ 10 MHz, $t_r = t_f \le 2$ ns, duty cycle = 50%
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.
E. Equivalent loads may be used for testing.

Figure 8. Load Circuit and Voltage Waveforms

metastable characteristics of TIBPAL16R4-5C, TIBPAL16R6-5C, and TIBPAL16R8-5C

At some point a system designer is faced with the problem of synchronizing two digital signals operating at two different frequencies. This problem is typically overcome by synchronizing one of the signals to the local clock through use of a flip-flop. However, this solution presents an awkward dilemma since the setup and hold time specifications associated with the flip-flop are sure to be violated. The metastable characteristics of the flip-flop can influence overall system reliability.

Whenever the setup and hold times of a flip-flop are violated, its output response becomes uncertain and is said to be in the metastable state if the output hangs up in the region between V_{IL} and V_{IH}. This metastable condition lasts until the flip-flop falls into one of its two stable states, which takes longer than the specified maximum propagation delay time (CLK to Q max).

From a system engineering standpoint, a designer cannot use the specified data sheet maximum for propagation delay time when using the flip-flop as a data synchronizer – how long to wait after the specified data sheet maximum must be known before using the data in order to guarantee reliable system operation.

The circuit shown in Figure 9 can be used to evaluate MTBF (Mean Time Between Failure) and Δt for a selected flip-flop. Whenever the Q output of the DUT is between 0.8 V and 2 V, the comparators are in opposite states. When the Q output of the DUT is higher than 2 V or lower than 0.8 V, the comparators are at the same logic level. The outputs of the two comparators are sampled a selected time (Δt) after system clock (SCLK). The exclusive OR gate detects the occurrence of a failure and increments the failure counter.

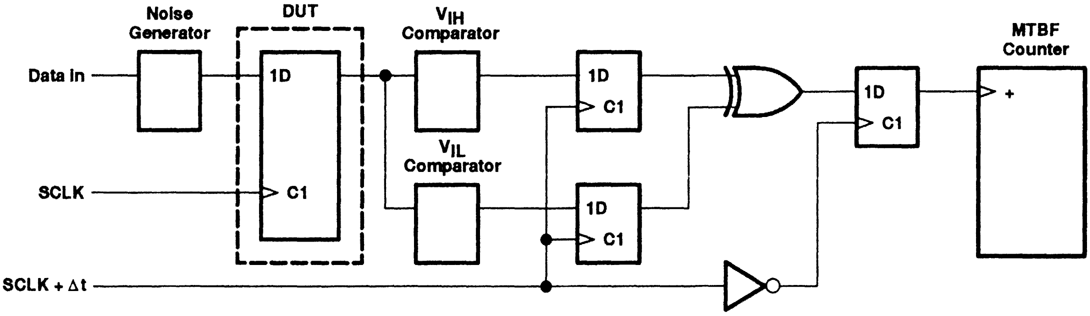
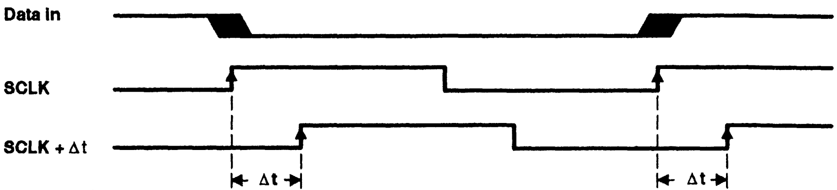


Figure 9. Metastable Evaluation Test Circuit

In order to maximize the possibility of forcing the DUT into a metastable state, the input data signal is applied so that it always violates the setup and hold time. This condition is illustrated in the timing diagram in Figure 10. Any other relationship of SCLK to data will provide less chance for the device to enter into the metastable state.



$$\text{MTBF} = \frac{\text{Time (sec)}}{\text{\# Failures}}$$

$$t_{rec} = \Delta t - \text{CLK to Q (max)}$$

Figure 10. Timing Diagram

By using the described test circuit, MTBF can be determined for several different values of Δt (see Figure 9). Plotting this information on semilog scale demonstrates the metastable characteristics of the selected flip-flop. Figure 11 shows the results for the TIBPAL16'-5C operating at 1 MHz.

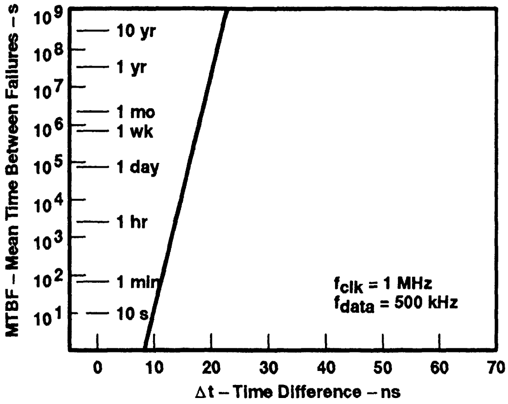


Figure 11. Metastable Characteristics

From the data taken in the above experiment, an equation can be derived for the metastable characteristics at other clock frequencies.

The metastable equation: $\frac{1}{\text{MTBF}} = f_{\text{SCLK}} \times f_{\text{data}} \times C1\ e^{(-C2 \times \Delta t)}$

The constants C1 and C2 describe the metastable characteristics of the device. From the experimental data, these constants can be solved for: $C1 = 4.37 \times 10^{-3}$ and $C2 = 2.01$

Therefore

$$\frac{1}{\text{MTBF}} = f_{\text{SCLK}} \times f_{\text{data}} \times 4.37 \times 10^{-3}\ e^{(-2.01 \times \Delta t)}$$

definition of variables

DUT (Device Under Test): The DUT is a 5-ns registered PLD programmed with the equation Q : = D.

MTBF (Mean Time Between Failures): The average time (s) between metastable occurrences that cause a violation of the device specifications.

f_{SCLK} (system clock frequency): Actual clock frequency for the DUT.

f_{data} (data frequency): Actual data frequency for a specified input to the DUT.

C1: Calculated constant that defines the magnitude of the curve.

C2: Calculated constant that defines the slope of the curve.

t_{rec} (metastability recovery time): Minimum time required to guarantee recovery from metastability, at a given MTBF failure rate. $t_{\text{rec}} = \Delta t - t_{\text{pd}}$ (CLK to Q, max)

Δt: The time difference (ns) from when the synchronizing flip-flop is clocked to when its output is sampled.

The test described above has shown the metastable characteristics of the TIBPAL16R4/R6/R8-5C series. For additional information on metastable characteristics of Texas Instruments logic circuits, please refer to TI Applications publication SDAA004, "Metastable Characteristics, Design Considerations for ALS, AS, and LS Circuits."

TYPICAL CHARACTERISTICS

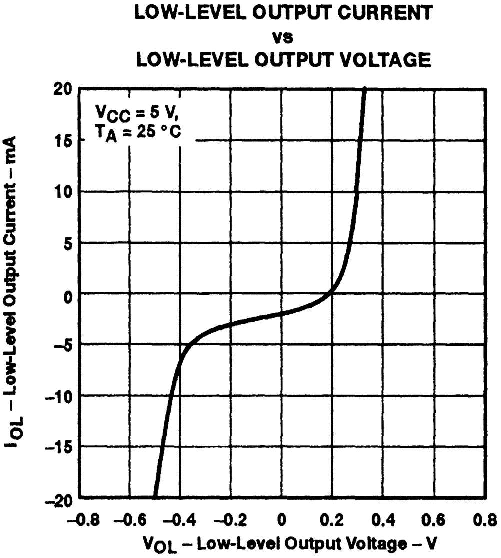


Figure 12

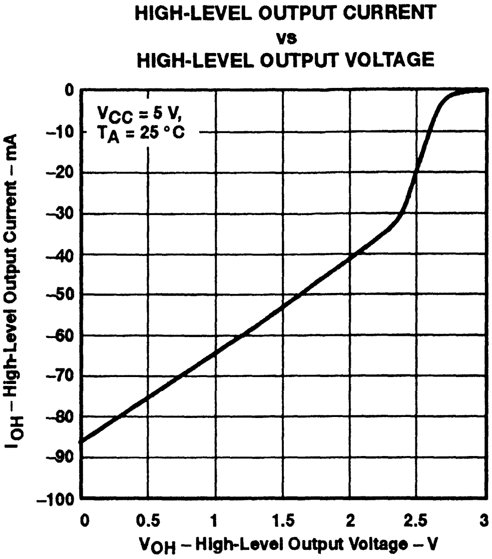


Figure 13

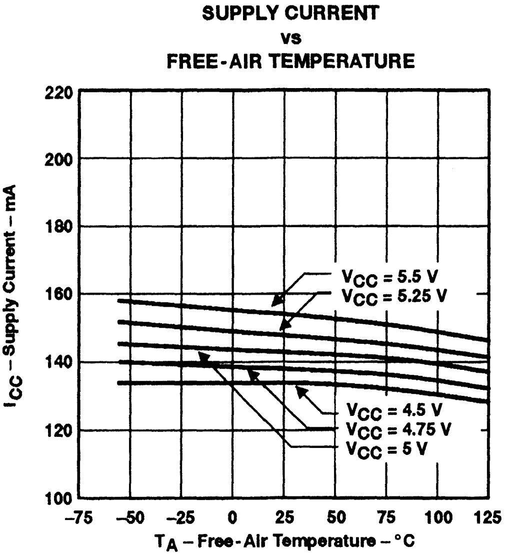


Figure 14

TYPICAL CHARACTERISTICS

POWER DISSIPATION vs FREQUENCY 8-BIT COUNTER MODE

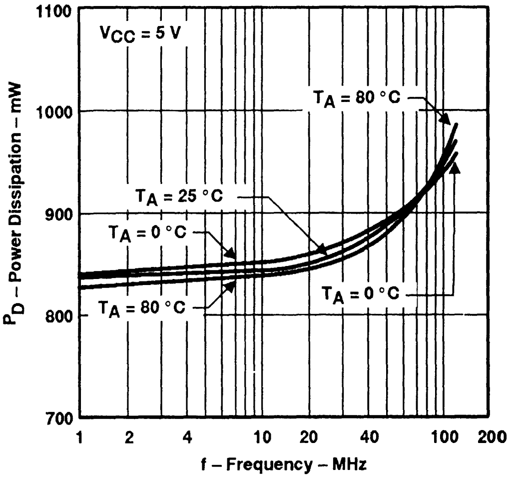


Figure 15

PROPAGATION DELAY TIME vs SUPPLY VOLTAGE

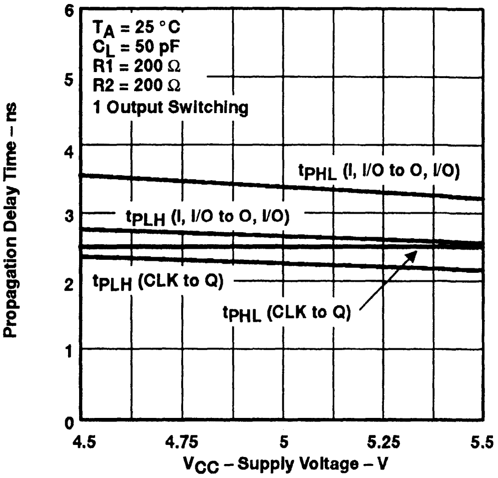


Figure 16

PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE

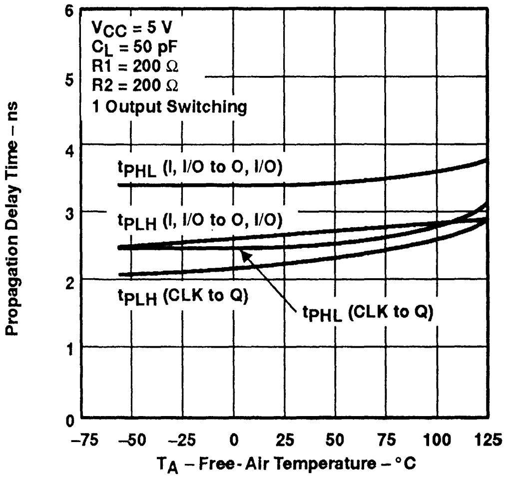


Figure 17

PROPAGATION DELAY TIME vs LOAD CAPACITANCE

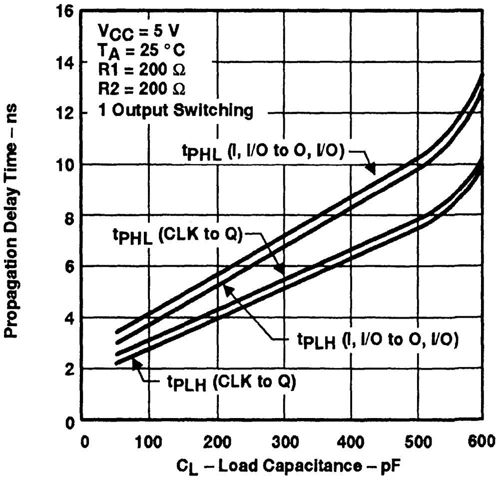


Figure 18

TYPICAL CHARACTERISTICS

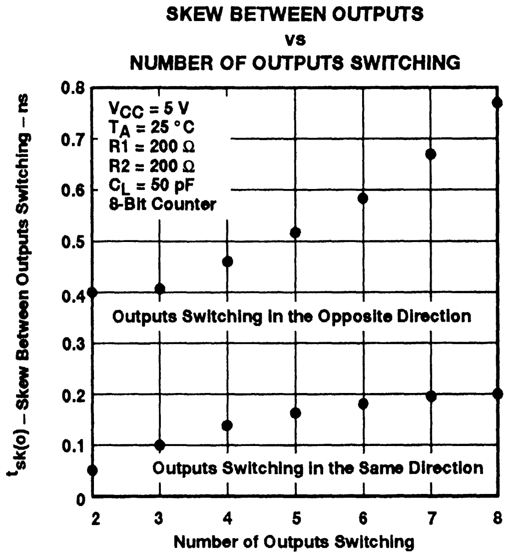

SKEW BETWEEN OUTPUTS
vs
NUMBER OF OUTPUTS SWITCHING

Figure 19

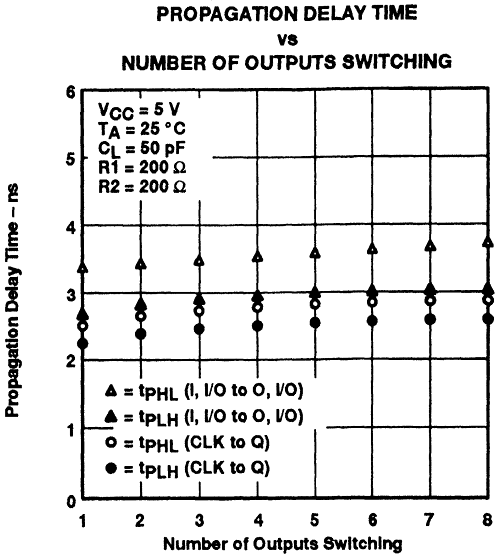

PROPAGATION DELAY TIME
vs
NUMBER OF OUTPUTS SWITCHING

Figure 20

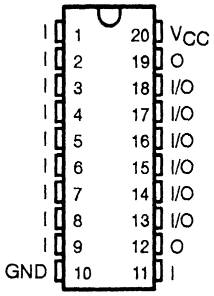
TIBPAL16L8-7C, TIBPAL16R4-7C, TIBPAL16R6-7C, TIBPAL16R8-7C
TIBPAL16L8-10M, TIBPAL16R4-10M, TIBPAL16R6-10M, TIBPAL16R8-10M
HIGH-PERFORMANCE *IMPACT-X*™ *PAL*® CIRCUITS

SRPS006D – D3115, MAY 1988 – REVISED MARCH 1992

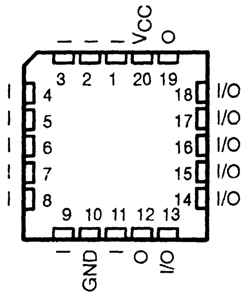
- **High-Performance Operation:**
  f_{max} (no feedback)
    TIBPAL16R'-7C Series . . . 100 MHz Min
    TIBPAL16R'-10M Series . . . 62.5 MHz Min
  f_{max} (internal feedback)
    TIBPAL16R'-7C Series . . . 100 MHz Min
    TIBPAL16R'-10M Series . . . 62.5 MHz Min
  f_{max} (external feedback)
    TIBPAL16R'-7C Series . . . 74 MHz Min
    TIBPAL16R'-10M Series . . . 52.5 MHz Min
  Propagation Delay
    TIBPAL16L'-7C Series . . . 7 ns Max
    TIBPAL16L'-10M Series . . . 10 ns Max
- **Functionally Equivalent, but Faster than, Existing 20-Pin PLDs**
- **Preload Capability on Output Registers Simplifies Testing**
- **Power-Up Clear on Registered Devices (All Register Outputs are Set Low, but Voltage Levels at the Output Pins Go High)**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Security Fuse Prevents Duplication**
- **Dependable Texas Instruments Quality and Reliability**

DEVICE	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
PAL16L8	10	2	0	6
PAL16R4	8	0	4 (3-state buffers)	4
PAL16R6	8	0	6 (3-state buffers)	2
PAL16R8	8	0	8 (3-state buffers)	0

TIBPAL16L8'
C SUFFIX . . . J OR N PACKAGE
M SUFFIX . . . J PACKAGE
(TOP VIEW)



TIBPAL16L8'
C SUFFIX . . . FN PACKAGE
M SUFFIX . . . FK PACKAGE
(TOP VIEW)



Pin assignments in operating mode

description

These programmable array logic devices feature high speed and functional equivalency when compared with currently available devices. These IMPACT-X™ circuits combine the latest Advanced Low-Power Schottky technology with proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional TTL logic. Their easy programmability allows for quick design of custom functions and typically results in a more compact circuit board. In addition, chip carriers are available for futher reduction in board space.

All of the register outputs are set to a low level during power-up. Extra circuitry has been provided to allow loading of each register asynchronously to either a high or low state. This feature simplifies testing because the registers can be set to an initial state prior to executing the test sequence.

The TIBPAL16' C series is characterized from 0°C to 75°C. The TIBPAL16' M series is characterized for operation over the full military temperature range of –55°C to 125°C.

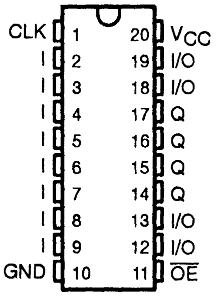
These devices are covered by U.S. Patent 4,410,987.
IMPACT-X is a trademark of Texas Instruments Incorporated.
PAL is a registered trademark of Advanced Micro Devices Inc.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 1992, Texas Instruments Incorporated

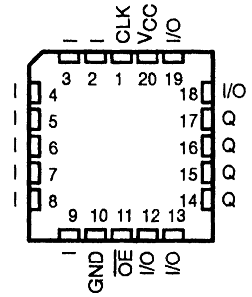
TIBPAL16R4'
C SUFFIX . . . J OR N PACKAGE
M SUFFIX . . . J PACKAGE

(TOP VIEW)



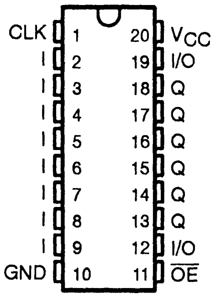
TIBPAL16R4'
C SUFFIX . . . FN PACKAGE
M SUFFIX . . . FK PACKAGE

(TOP VIEW)



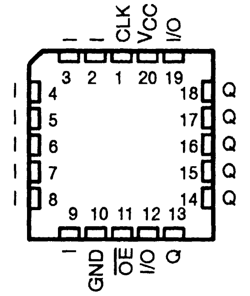
TIBPAL16R6'
C SUFFIX . . . J OR N PACKAGE
M SUFFIX . . . J PACKAGE

(TOP VIEW)



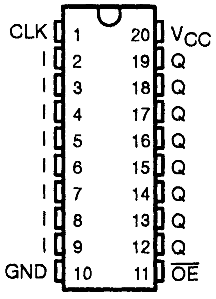
TIBPAL16R6'
C SUFFIX . . . FN PACKAGE
M SUFFIX . . . FK PACKAGE

(TOP VIEW)



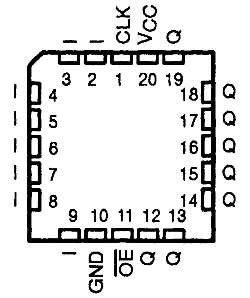
TIBPAL16R8'
C SUFFIX . . . J OR N PACKAGE
M SUFFIX . . . J PACKAGE

(TOP VIEW)



TIBPAL16R8'
C SUFFIX . . . FN PACKAGE
M SUFFIX . . . FK PACKAGE

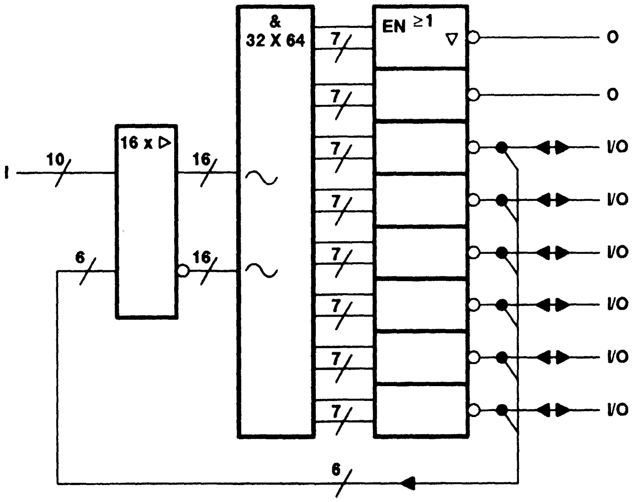
(TOP VIEW)



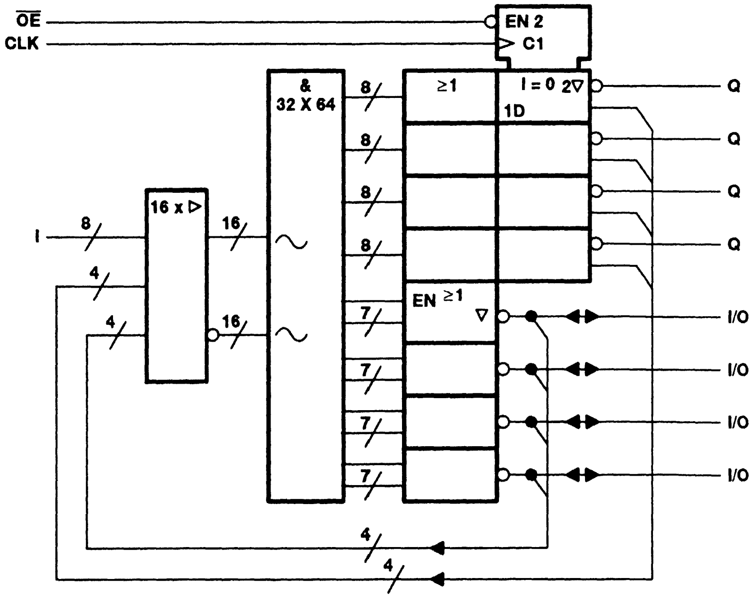
Pin assignments in operating mode

functional block diagrams (positive logic)

TIBPAL16L8'



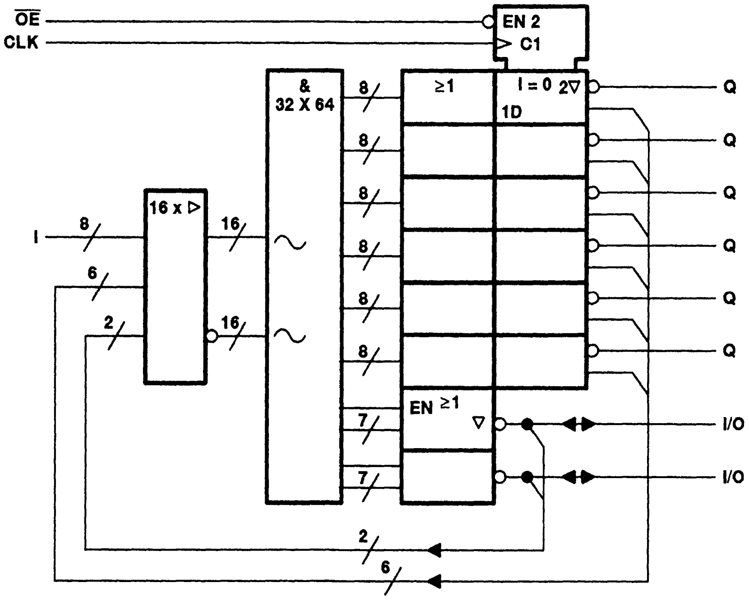
TIBPAL16R4'



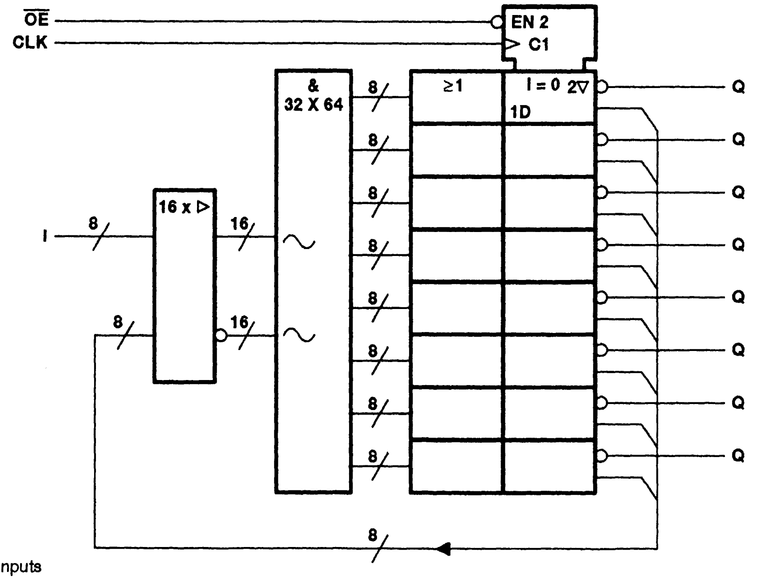
∿ denotes fused inputs

functional block diagrams (positive logic)

TIBPAL16R6'

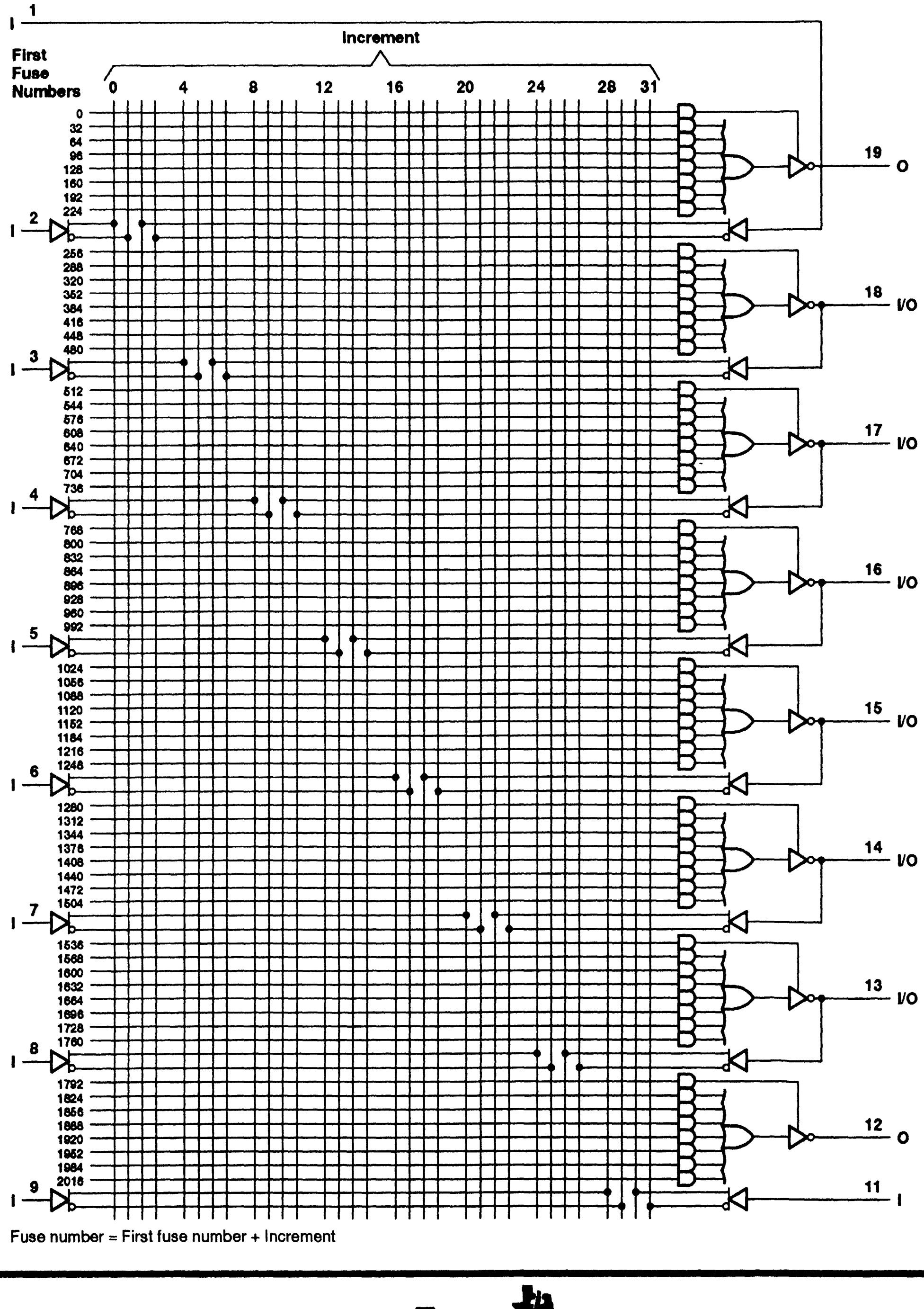


TIBPAL16R8'



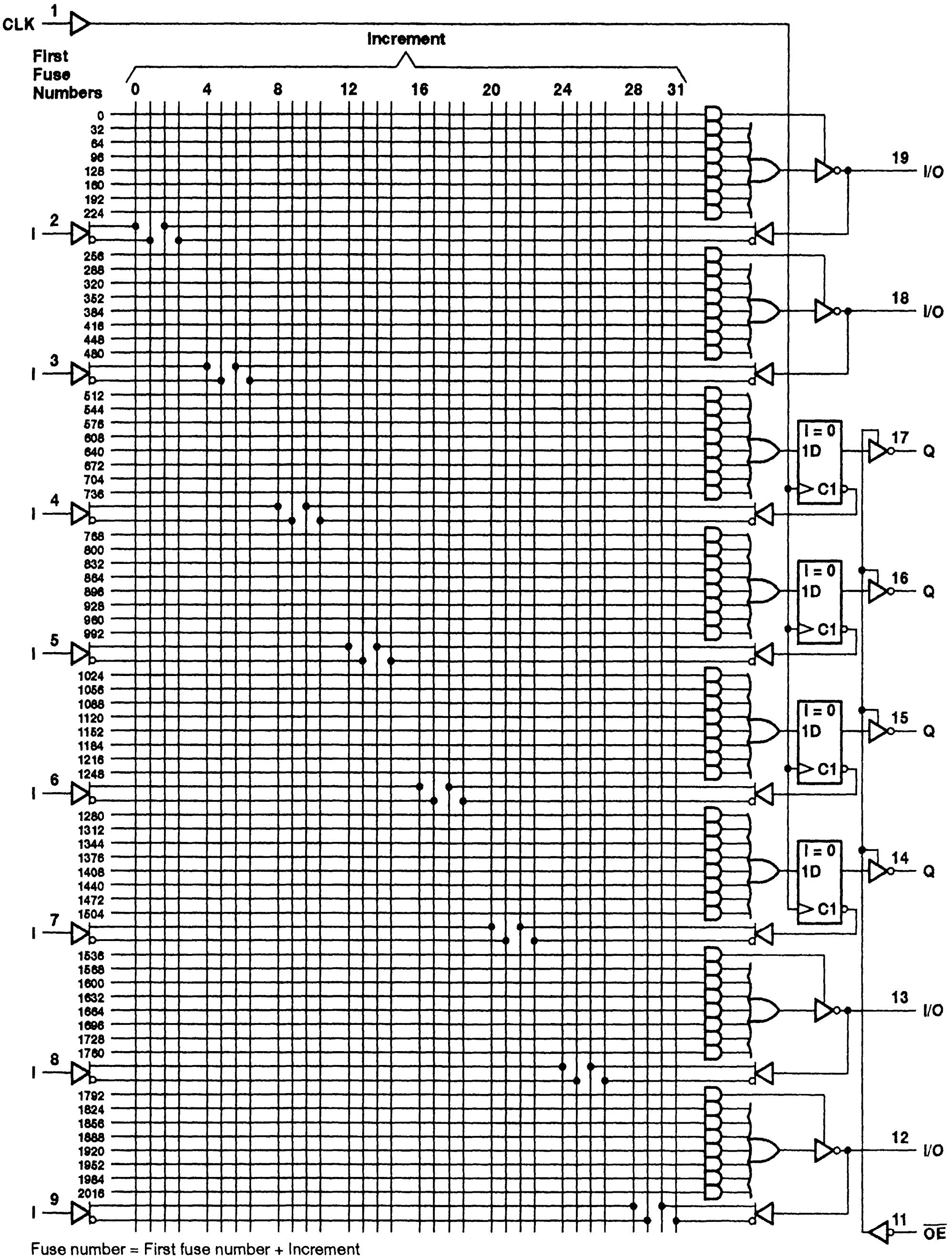
∿ denotes fused inputs

logic diagram (positive logic)



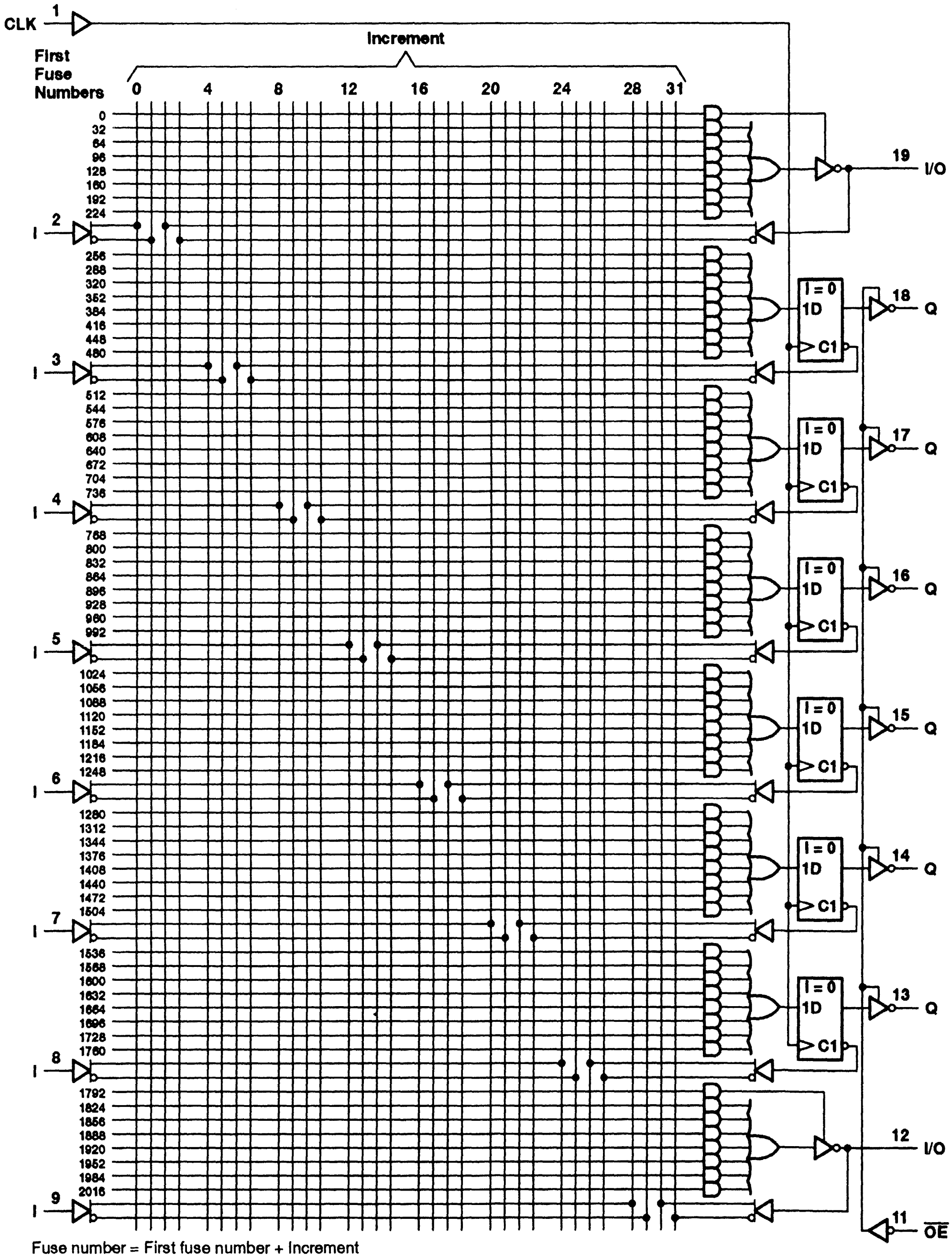
Fuse number = First fuse number + Increment

logic diagram (positive logic)



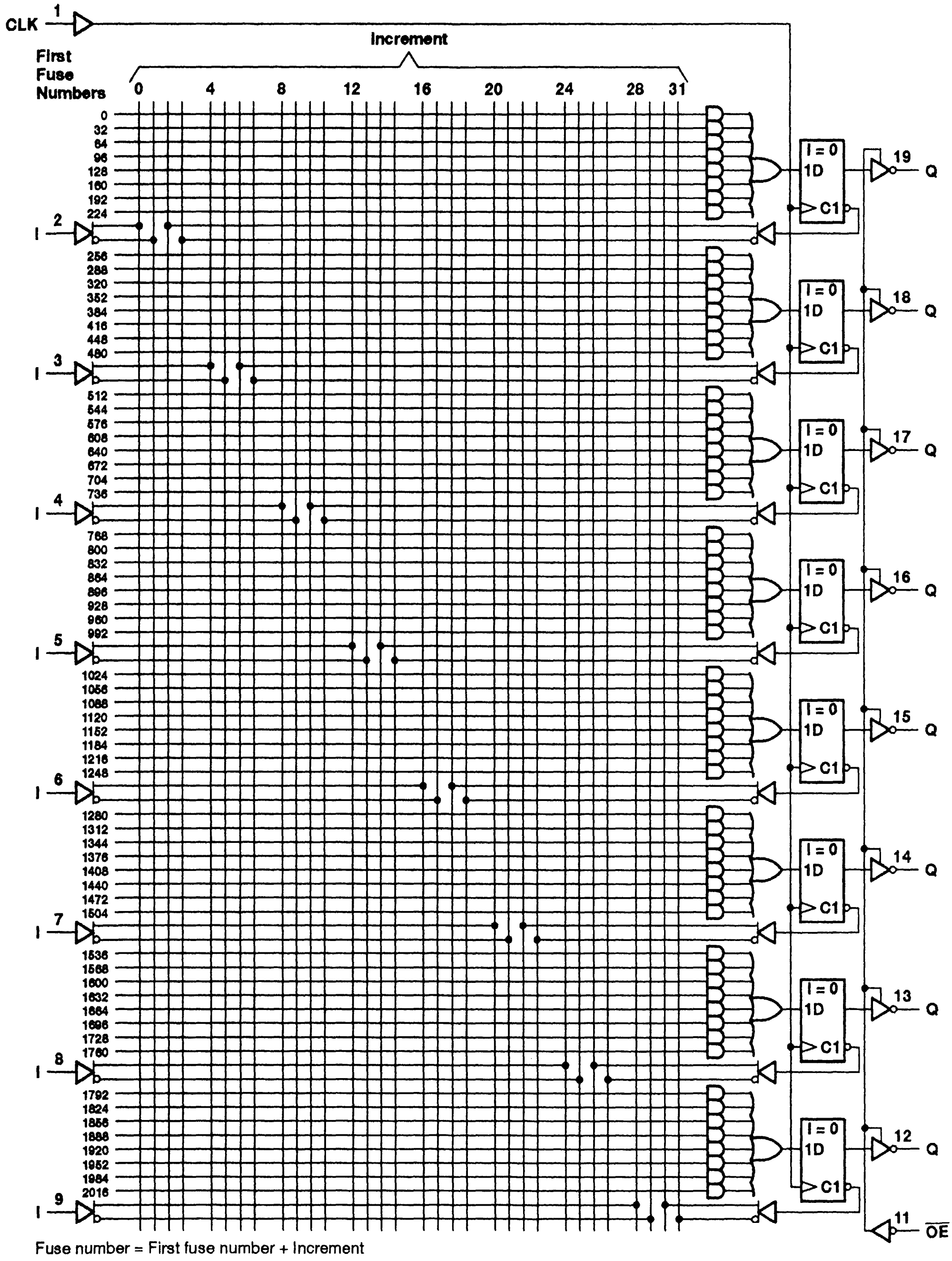
Fuse number = First fuse number + Increment

logic diagram (positive logic)



Fuse number = First fuse number + Increment

logic diagram (positive logic)



Fuse number = First fuse number + Increment

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (see Note 1)	5.5 V
Voltage applied to disabled output (see Note 1)	5.5 V
Operating free-air temperature range	0°C to 75°C
Storage temperature range	–65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage (see Note 2)		2		5.5	V
V_{IL}	Low-level input voltage (see Note 2)				0.8	V
I_{OH}	High-level output current				–3.2	mA
I_{OL}	Low-level output current				24	mA
f_{clock}	Clock frequency		0		100	MHz
t_w	Pulse duration, clock (see Note 2)	High	5			ns
		Low	5			
t_{su}	Setup time, input or feedback before clock↑		7			ns
t_h	Hold time, input or feedback after clock↑		0			ns
T_A	Operating free-air temperature		0	25	75	°C

NOTE 2: These are absolute voltage levels with respect to the ground pin of the device and include all overshoots due to system and/or tester noise. Testing these parameters should not be attempted without suitable equipment.

electrical characteristics over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.75 V,	I_I = –18 mA			–0.8	–1.5	V
V_{OH}	V_{CC} = 4.75 V,	I_{OH} = –3.2 mA		2.4	3.2		V
V_{OL}	V_{CC} = 4.75 V,	I_{OL} = 24 mA			0.3	0.5	V
I_{OZH}‡	V_{CC} = 5.25 V,	V_O = 2.7 V				100	µA
I_{OZL}‡	V_{CC} = 5.25 V,	V_O = 0.4 V				–100	µA
I_I	V_{CC} = 5.25 V,	V_I = 5.5 V				100	µA
I_{IH}‡	V_{CC} = 5.25 V,	V_I = 2.7 V				25	µA
I_{IL}‡	V_{CC} = 5.25 V,	V_I = 0.4 V			–80	–250	µA
I_{OS}§	V_{CC} = 5.25 V,	V_O = 0.5 V		–30	–70	–130	mA
I_{CC}	V_{CC} = 5.25 V,	V_I = 0,	Outputs open		160	180	mA
C_i	f = 1 MHz,	V_I = 2 V			5		pF
C_o	f = 1 MHz,	V_O = 2 V			6		pF
C_{clk}	f = 1 MHz,	V_{CLK} = 2 V			6		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ I/O leakage is the worst case of I_{OZL} and I_{IL} or I_{OZH} and I_{IH} respectively.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second. V_O is set at 0.5 V to avoid test problems caused by test equipment ground degradation.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		TEST CONDITION	MIN	TYP†	MAX	UNIT
f_{max}‡	without feedback			R1 = 200 Ω, R2 = 390 Ω, See Figure 6	100			MHz
	with internal feedback (counter configuration)				100			
	with external feedback				74			
t_{pd}	I, I/O	O, I/O	1 or 2 outputs switching		3	5.5	7	ns
			8 outputs switching		3	6	7.5	
t_{pd}	CLK↑	Q			2	4	6.5	ns
t_{pd}§	CLK↑	Feedback input					3	ns
t_{en}	OE↓	Q				4	7.5	ns
t_{dis}	OE↑	Q				4	7.5	ns
t_{en}	I, I/O	O, I/O				6	9	ns
t_{dis}	I, I/O	O, I/O				6	9	ns
$t_{sk(o)}$¶	Skew between registered outputs					0.5		ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ See section for f_{max} specifications.

§ This parameter applies to TIBPAL16R4' and TIBPAL16R6' only (see Figure 4 for illustration) and is calculated from the measured f_{max} with internal feedback in the counter configuration.

¶ This parameter is the measurement of the difference between the fastest and slowest t_{pd} (CLK-to-Q) observed when multiple registered outputs are switching in the same direction.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) .... 7 V
Input voltage (see Note 1) .... 5.5 V
Voltage applied to disabled output (see Note 1) .... 5.5 V
Operating free-air temperature range .... −55°C to 125°C
Storage temperature range .... −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−2	mA
I_{OL}	Low-level output current				12	mA
f_{clock}†	Clock frequency		0		62.5	MHz
t_w	Pulse duration, clock (see Note 2)	High	8			ns
		Low	8			
t_{su}†	Setup time, input or feedback before clock↑		10			ns
t_h†	Hold time, input or feedback after clock↑		0			ns
T_A	Operating free-air temperature		−55	25	125	°C

NOTE 2: These are absolute voltage levels with respect to the ground pin of the device and include all overshoots due to system and/or tester noise. Testing these parameters should not be attempted without suitable equipment.

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−0.8	−1.5	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −2 mA		2.4	3.2		V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA			0.3	0.5	V
I_{OZH}‡		V_{CC} = 5.5 V,	V_O = 2.7 V				100	µA
I_{OZL}‡	O, Q outputs	V_{CC} = 5.5 V,	V_O = 0.4 V				−0.1	mA
	I/O ports						−0.25	
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V				1	mA
I_{IH}	I/O ports	V_{CC} = 5.5 V,	V_I = 2.7 V				100	µA
	All others						25	
I_{IL}‡		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.08	−0.25	mA
I_{OS}§		V_{CC} = 5.5 V,	V_O = 0.5 V		−30	−70	−130	mA
I_{CC}		V_{CC} = 5.5 V,	V_I = GND,	Outputs open		140	200	mA
C_i		f = 1 MHz,	V_I = 2 V			5		pF
C_o		f = 1 MHz,	V_O = 2 V			6		pF
$C_{clk/oe}$		f = 1 MHz,	$V_{CLK/OE}$ = 2 V			6		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ I/O leakage is the worst case of I_{OZL} and I_{IL} or I_{OZH} and I_{IH} respectively.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second. V_O is set at 0.5 V to avoid test problems caused by test equipment ground degradation.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	TYP†	MAX	UNIT
f_{max}‡	without feedback		R1 = 390 Ω, R2 = 750 Ω, See Figure 6	62.5			MHz
	with internal feedback (counter configuration)			62.5			
	with external feedback			52.5			
t_{pd}	I, I/O	O, I/O		2	6	10	ns
t_{pd}	CLK↑	Q		1	4	9	ns
t_{pd}§	CLK↑	Feedback input				5	ns
t_{en}	OE↓	Q		1	4	10	ns
t_{dis}	OE↑	Q		1	4	10	ns
t_{en}	I, I/O	O, I/O		2	6	12	ns
t_{dis}	I, I/O	O, I/O		1	6	10	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ See section for f_{max} specifications. f_{max} with external feedback is not production tested but is calculated from the equation found in the f_{max} section.

§ This parameter applies to TIBPAL16R4' and TIBPAL16R6' only (see Figure 4 for illustration) and is calculated from the measured f_{max} with internal feedback in the counter configuration.

programming information

Texas Instruments programmable logic devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments programmable logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

preload procedure for registered outputs (see Figure 1 and Note 3)

The output registers can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below.

Step 1. With V_{CC} at 5 volts and Pin 1 at V_{IL}, raise Pin 11 to V_{IHH}.
Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.
Step 3. Pulse Pin 1, clocking in preload data.
Step 4. Remove output voltage, then lower Pin 11 to V_{IL}. Preload can be verified by observing the voltage level at the output pin.

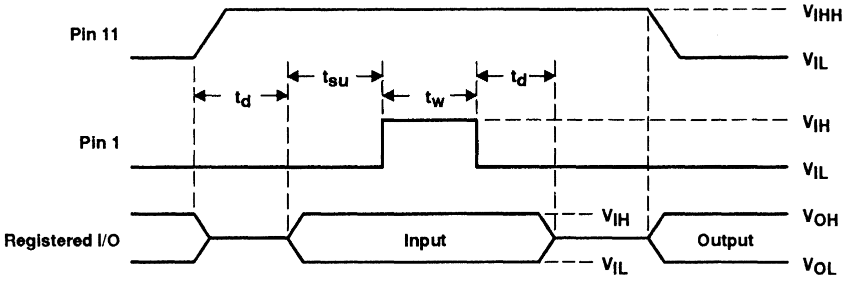
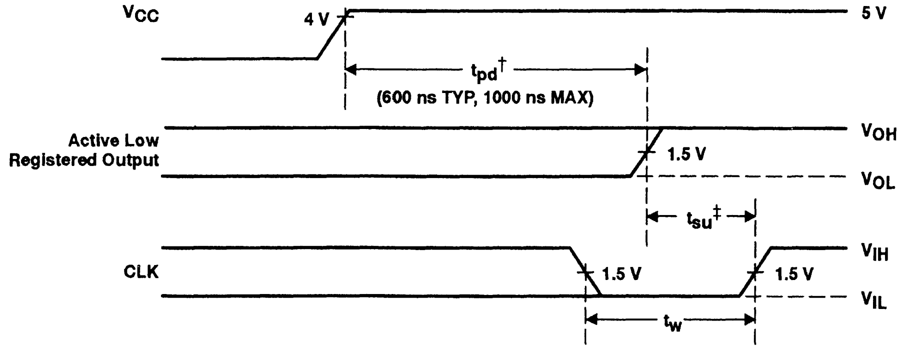


Figure 1. Preload Waveforms

NOTE 3: $t_d = t_{su} = t_h$ = 100 ns to 1000 ns V_{IHH} = 10.25 V to 10.75 v

power-up reset (see Figure 2)

Following power up, all registers are reset to zero. This feature provides extra flexibility to the system designer and is especially valuable in simplifying state-machine initialization. To ensure a valid power-up reset, it is important that the rise of V_{CC} be monotonic. Following power-up reset, a low-to-high clock transition must not occur until all applicable input and feedback setup times are met.



† This is the power-up reset time and applies to registered outputs only. The values shown are from characterization data.
‡ This is the setup time for input or feedback.

Figure 2. Power-Up Reset Waveforms

f_{max} SPECIFICATIONS

f_{max} without feedback, see Figure 3

In this mode, data is presented at the input to the flip-flop and clocked through to the Q output with no feedback. Under this condition, the clock period is limited by the sum of the data setup time and the data hold time ($t_{su} + t_h$). However, the minimum f_{max} is determined by the minimum clock period (t_w high + t_w low).

$$\text{Thus, } f_{max} \text{ without feedback} = \frac{1}{(t_w\text{high} + t_w\text{low})} \text{ or } \frac{1}{(t_{su} + t_h)}.$$

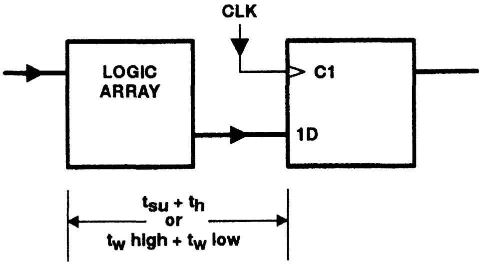


Figure 3. f_{max} Without Feedback

f_{max} with internal feedback, see Figure 4

This configuration is most popular in counters and on-chip state-machine designs. The flip-flop inputs are defined by the device inputs and flip-flop outputs. Under this condition, the period is limited by the internal delay from the flip-flop outputs through the internal feedback and logic array to the inputs of the next flip-flop.

$$\text{Thus, } f_{max} \text{ with internal feedback} = \frac{1}{(t_{su} + t_{pd}\ \text{CLK-to-FB})}.$$

Where tpd CLK-to-FB is the deduced value of the delay from CLK to the input of the logic array.

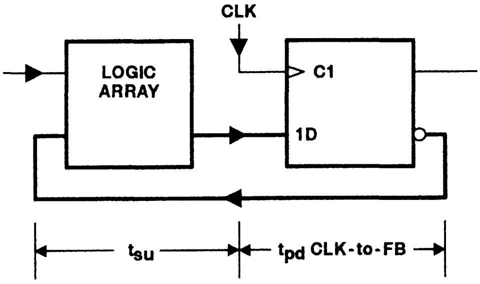


Figure 4. f_{max} With Internal Feedback

f_{max} SPECIFICATIONS

f_{max} with external feedback, see Figure 5

This configuration is a typical state-machine design with feedback signals sent off-chip. This external feedback could go back to the device inputs or to a second device in a multi-chip state machine. The slowest path defining the period is the sum of the clock-to-output time and the input setup time for the external signals (t_{su} + t_{pd} CLK-to-Q).

$$\text{Thus, } f\text{max with external feedback} = \frac{1}{(t_{su} + t_{pd}\ \text{CLK}-\text{to}-\text{Q})}.$$

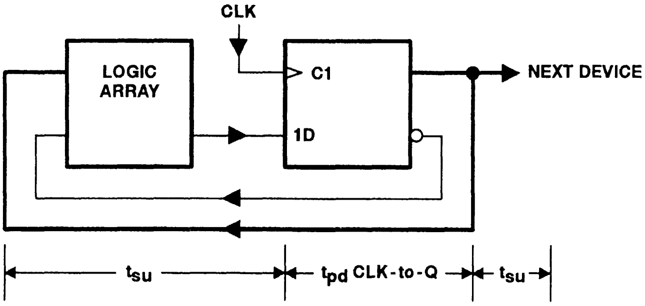
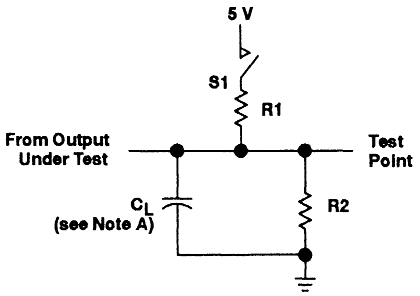
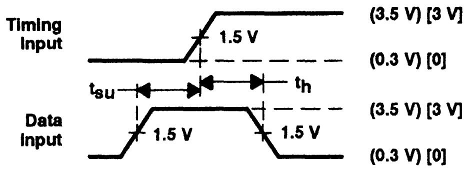


Figure 5. f_{max} With External Feedback

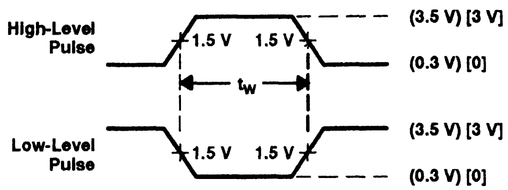
PARAMETER MEASUREMENT INFORMATION



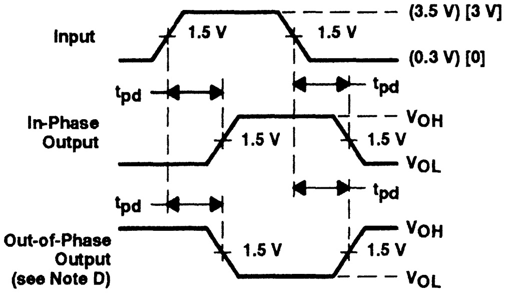
LOAD CIRCUIT FOR
3-STATE OUTPUTS



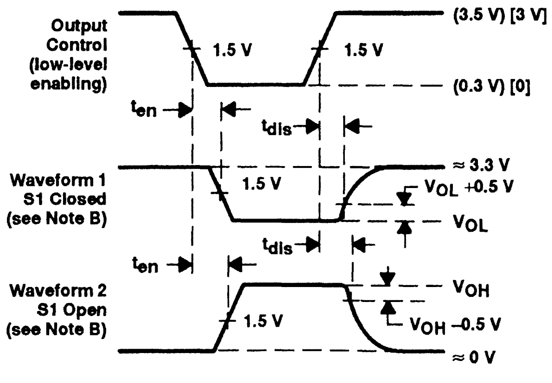
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES:
- A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses have the following characteristics: For C suffix, use the voltage levels indicated in parentheses ( ), PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%; For M suffix, use the voltage levels indicated in brackets [ ], PRR ≤ 10 MHz, t_r and $t_f \leq 2$ ns, duty cycle = 50%
- D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.
- E. Equivalent loads may be used for testing.

Figure 6. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

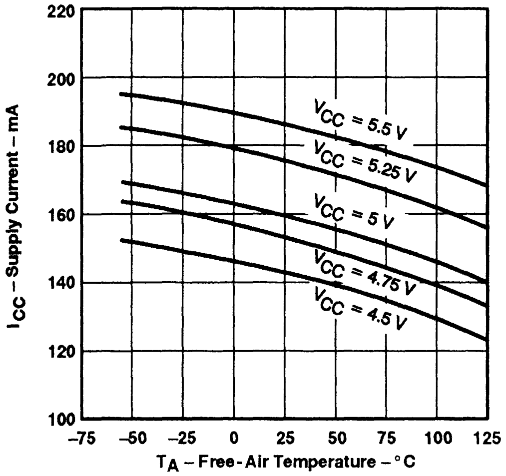


Figure 7

PROPAGATION DELAY TIME
vs
SUPPLY VOLTAGE

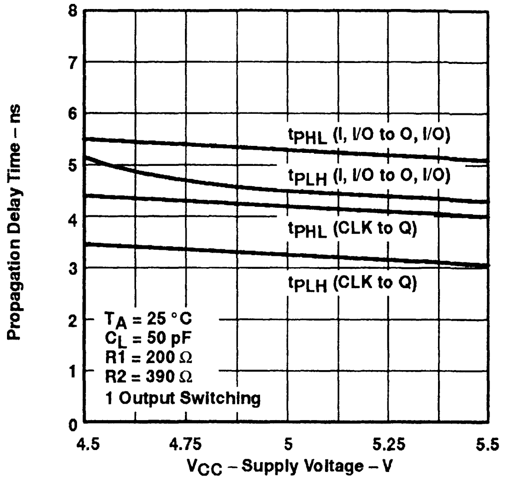


Figure 8

PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

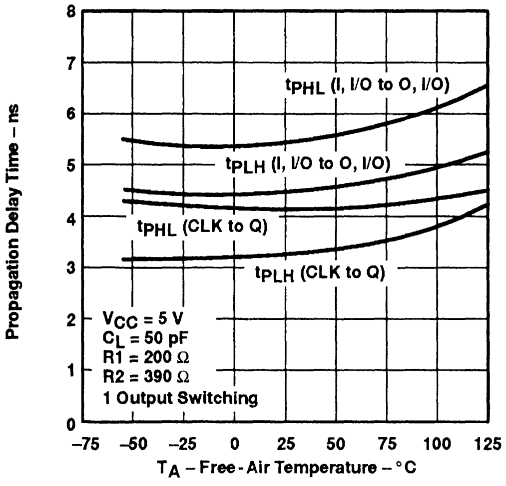


Figure 9

PROPAGATION DELAY TIME
vs
LOAD CAPACITANCE

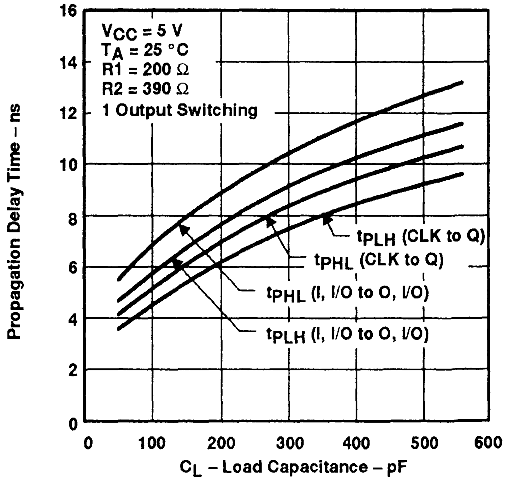


Figure 10

TYPICAL CHARACTERISTICS

POWER DISSIPATION vs FREQUENCY 8-BIT COUNTER MODE

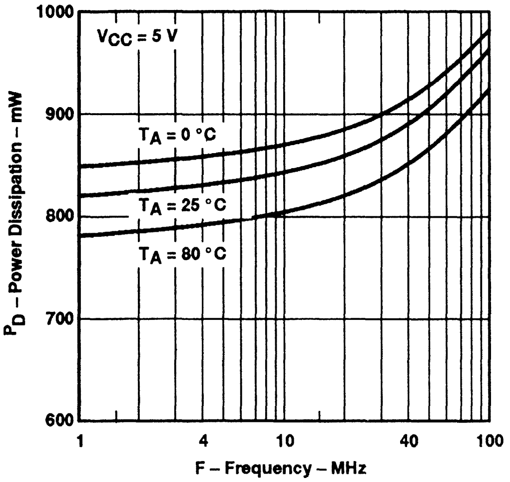


Figure 11

PROPAGATION DELAY TIME† vs NUMBER OF OUTPUTS SWITCHING

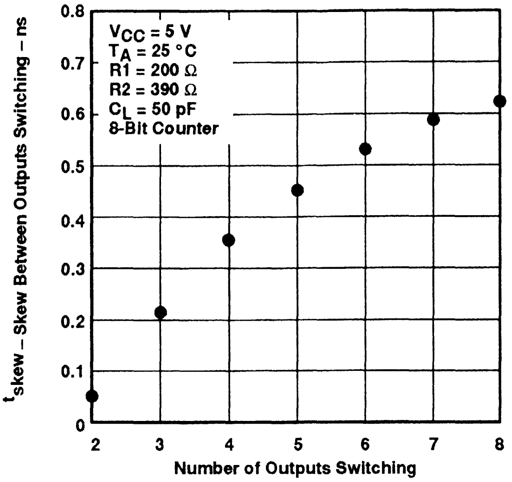


Figure 12

PROPAGATION DELAY TIME vs NUMBER OF OUTPUTS SWITCHING

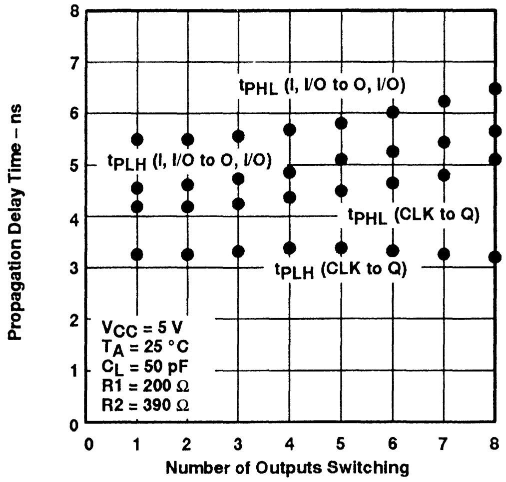


Figure 13

---

† Outputs switching in the same direction (t_{PLH} compared to t_{PLH}/t_{PHL} to t_{PHL})

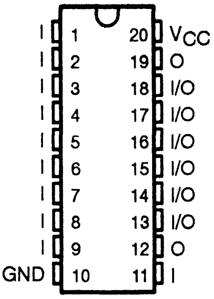
TIBPAL16L8-10C, TIBPAL16R4-10C, TIBPAL16R6-10C, TIBPAL16R8-10C
TIBPAL16L8-12M, TIBPAL16R4-12M, TIBPAL16R6-12M, TIBPAL16R8-12M
HIGH-PERFORMANCE *IMPACT-X*™ *PAL*® CIRCUITS

SRPS017 – D3023, MAY 1987 – REVISED MARCH 1992

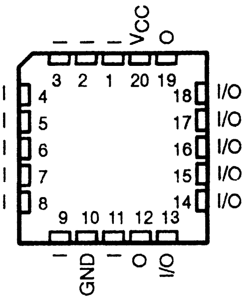
- **High-Performance Operation:**
  f_{max} (w/o feedback)
    TIBPAL16R'-10C Series . . . 62.5 MHz Min
    TIBPAL16R'-12M Series . . . 56 MHz Min
  f_{max} (with feedback)
    TIBPAL16R'-10C Series . . . 55.5 MHz Min
    TIBPAL16R'-12M Series . . . 48 MHz Min
  Propagation Delay
    TIBPAL16L'-10C Series . . . 10 ns Max
    TIBPAL16L'-12M Series . . . 12 ns Max
- **Functionally Equivalent, but Faster than, Existing 20-Pin PLDs**
- **Preload Capability on Output Registers Simplifies Testing**
- **Power-Up Clear on Registered Devices (All Register Outputs are Set Low, but Voltage Levels at the Output Pins Go High)**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Security Fuse Prevents Duplication**
- **Dependable Texas Instruments Quality and Reliability**

DEVICE	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
PAL16L8	10	2	0	6
PAL16R4	8	0	4 (3-state buffers)	4
PAL16R6	8	0	6 (3-state buffers)	2
PAL16R8	8	0	8 (3-state buffers)	0

TIBPAL16L8'
C SUFFIX . . . J OR N PACKAGE
M SUFFIX . . . J PACKAGE
(TOP VIEW)



TIBPAL16L8'
C SUFFIX . . . FN PACKAGE
M SUFFIX . . . FK PACKAGE
(TOP VIEW)



Pin assignments in operating mode

description

These programmable array logic devices feature high speed and functional equivalency when compared with currently available devices. These IMPACT-X™ circuits combine the latest Advanced Low-Power Schottky technology with proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional TTL logic. Their easy programmability allows for quick design of custom functions and typically results in a more compact circuit board. In addition, chip carriers are available for futher reduction in board space.

All of the register outputs are set to a low level during power up. Extra circuitry has been provided to allow loading of each register asynchronously to either a high or low state. This feature simplifies testing because the registers can be set to an initial state prior to executing the test sequence.

The TIBPAL16' C series is characterized from 0°C to 75°C. The TIBPAL16' M series is characterized for operation over the full military temperature range of –55°C to 125°C.

These devices are covered by U.S. Patent 4,410,987.
IMPACT-X is a trademark of Texas Instruments Incorporated.
PAL is a registered trademark of Advanced Micro Devices Inc.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

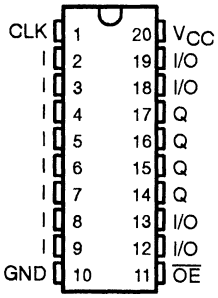
Copyright © 1992, Texas Instruments Incorporated

TEXAS INSTRUMENTS

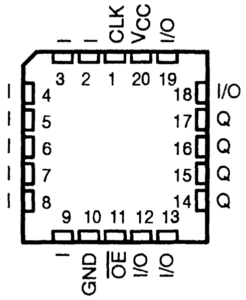
TIBPAL16R4-10C, TIBPAL16R6-10C, TIBPAL16R8-10C
TIBPAL16R4-12M, TIBPAL16R6-12M, TIBPAL16R8-12M
HIGH-PERFORMANCE *IMPACT-X*™ *PAL*® CIRCUITS

SRPS017 – D3023, MAY 1987 – REVISED MARCH 1992

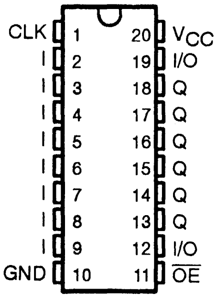
TIBPAL16R4'
C SUFFIX . . . J OR N PACKAGE
M SUFFIX . . . J PACKAGE
(TOP VIEW)



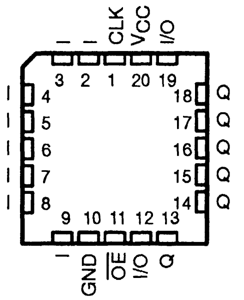
TIBPAL16R4'
C SUFFIX . . . FN PACKAGE
M SUFFIX . . . FK PACKAGE
(TOP VIEW)



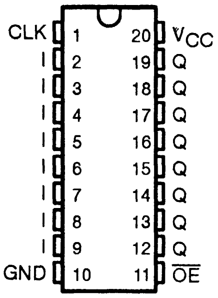
TIBPAL16R6'
C SUFFIX . . . J OR N PACKAGE
M SUFFIX . . . J PACKAGE
(TOP VIEW)



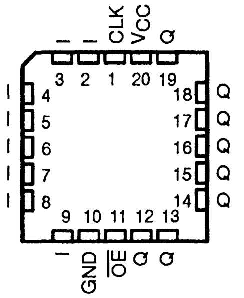
TIBPAL16R6'
C SUFFIX . . . FN PACKAGE
M SUFFIX . . . FK PACKAGE
(TOP VIEW)



TIBPAL16R8'
C SUFFIX . . . J OR N PACKAGE
M SUFFIX . . . J PACKAGE
(TOP VIEW)



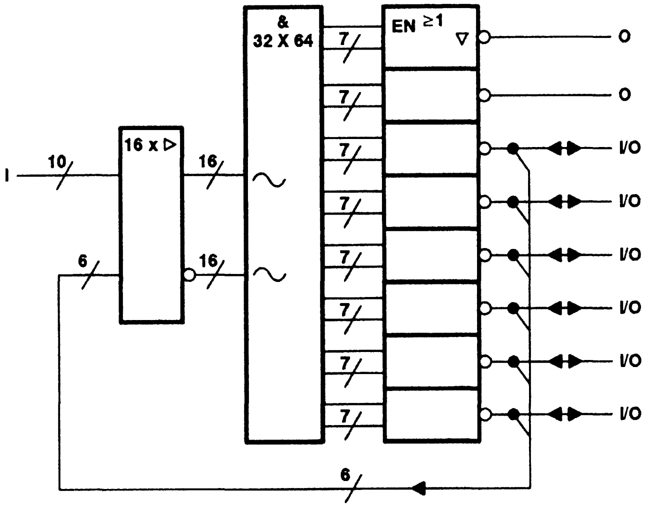
TIBPAL16R8'
C SUFFIX . . . FN PACKAGE
M SUFFIX . . . FK PACKAGE
(TOP VIEW)



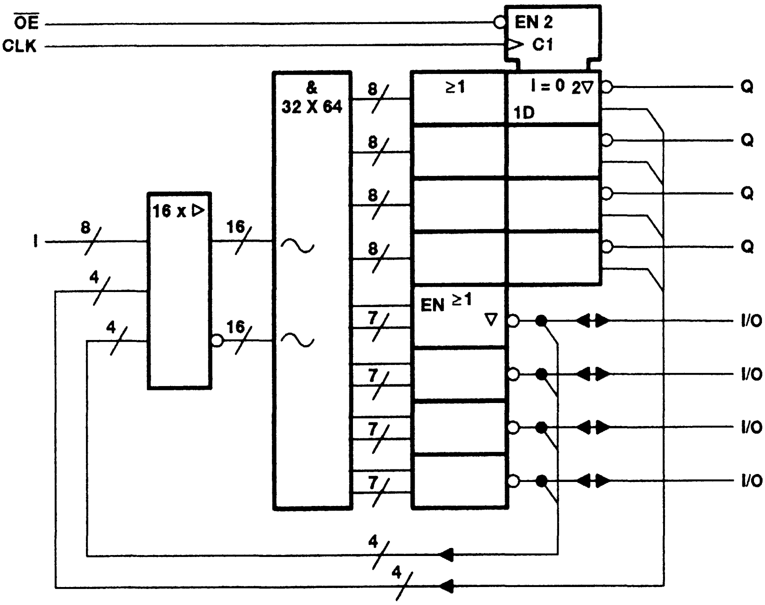
Pin assignments in operating mode

functional block diagrams (positive logic)

TIBPAL16L8'

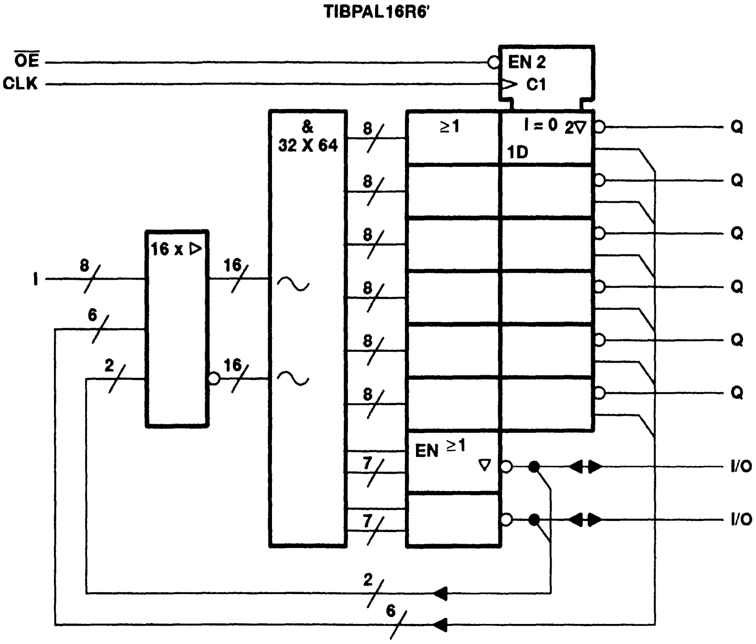


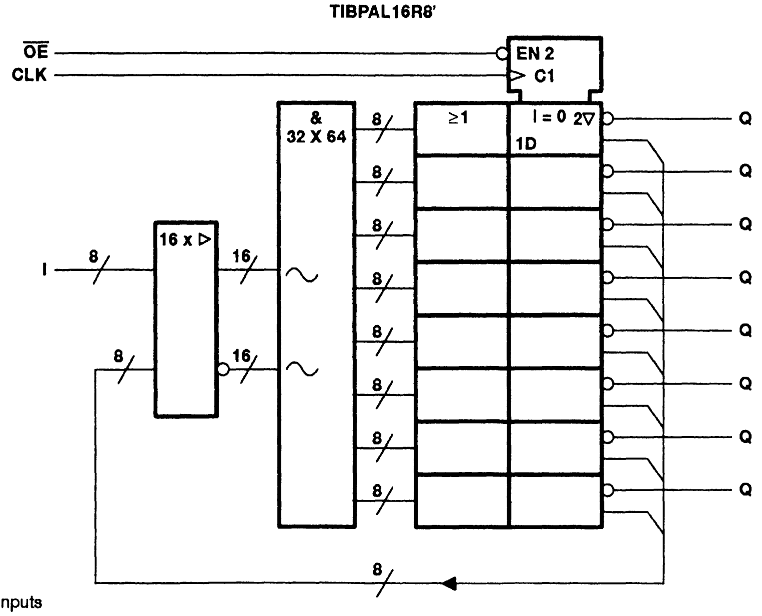
TIBPAL16R4'



∿ denotes fused inputs

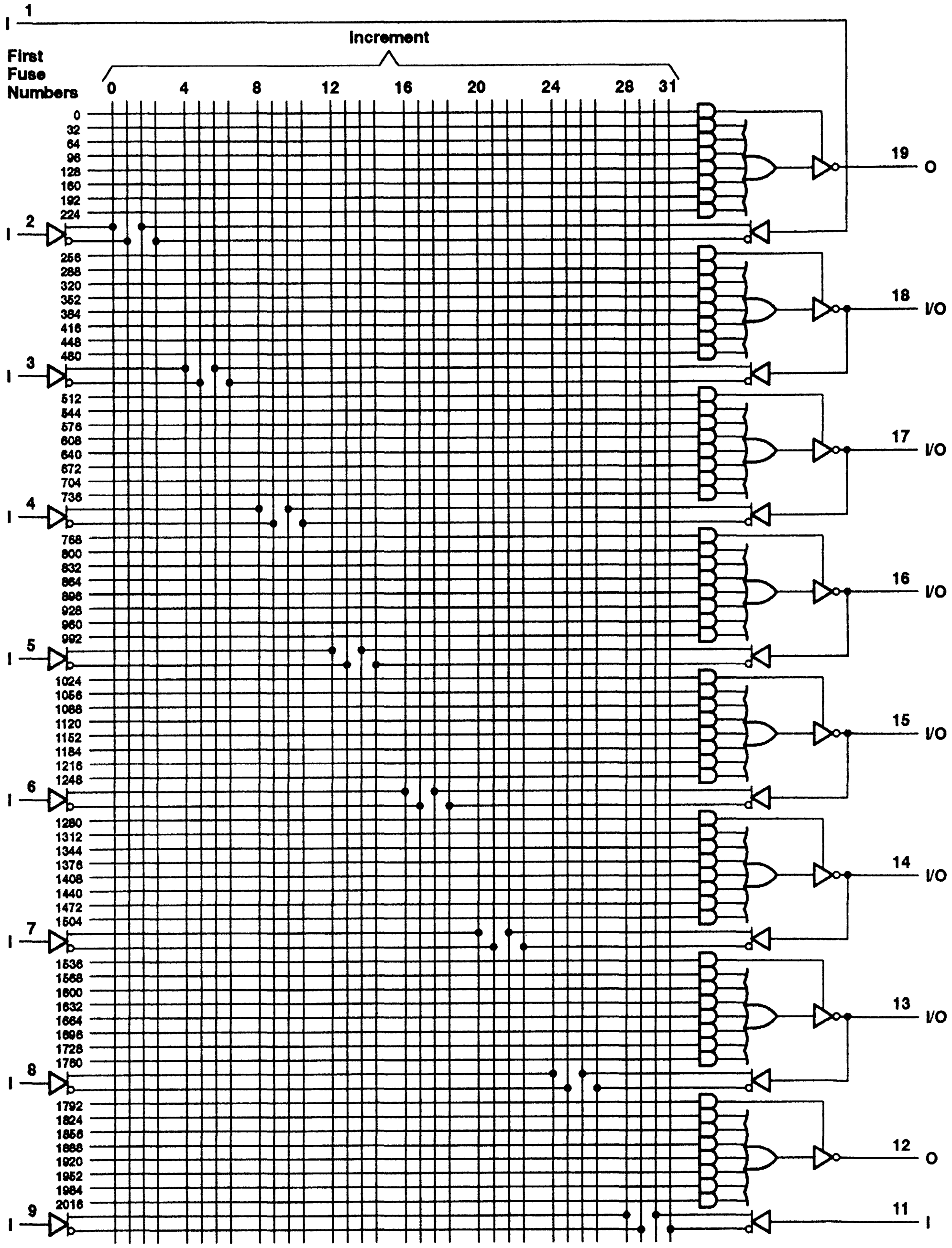
functional block diagrams (positive logic)





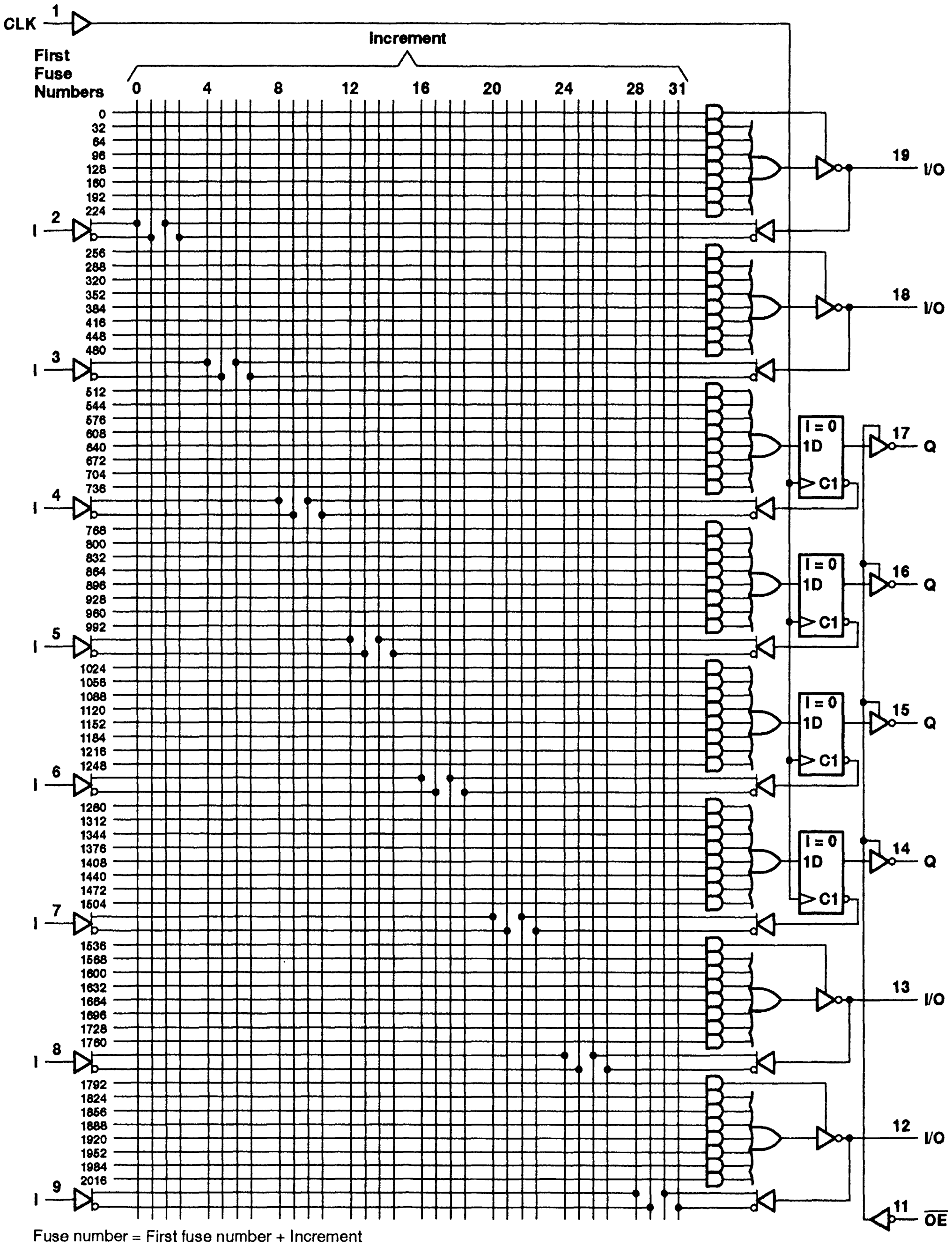
∿ denotes fused inputs

logic diagram (positive logic)



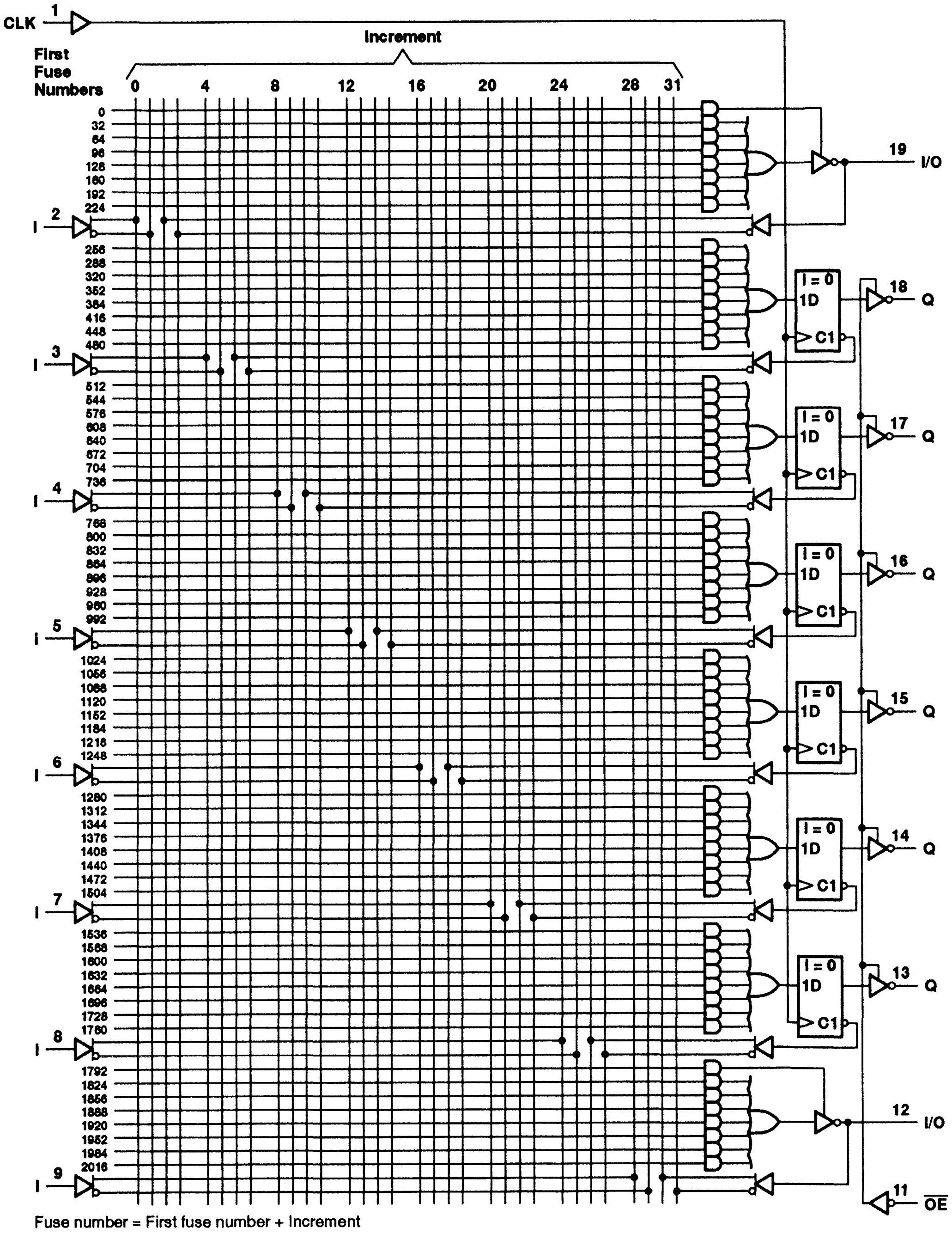
Fuse number = First fuse number + Increment

logic diagram (positive logic)



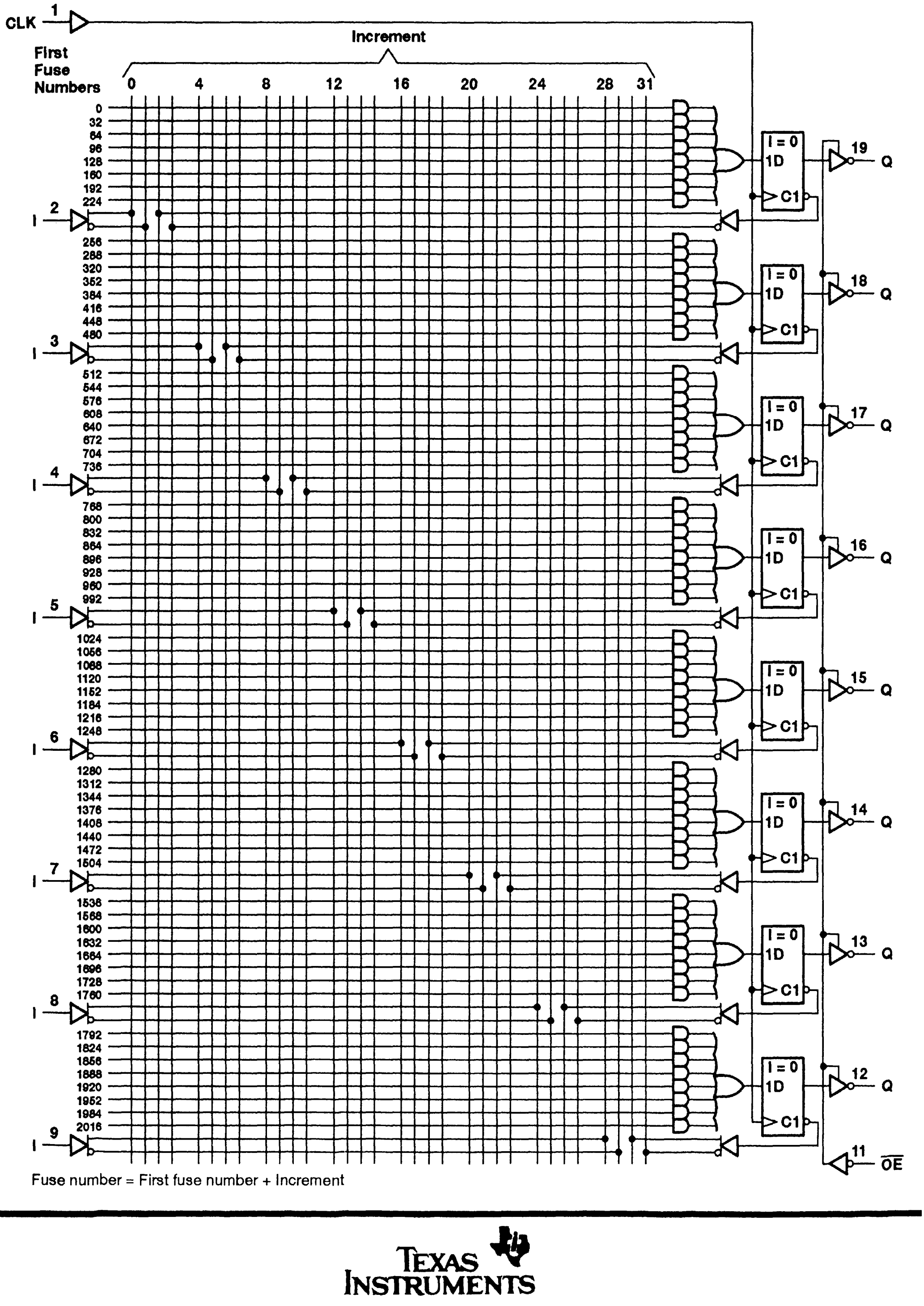
Fuse number = First fuse number + Increment

logic diagram (positive logic)



Fuse number = First fuse number + Increment

logic diagram (positive logic)



Fuse number = First fuse number + Increment

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) .... 7 V
Input voltage (see Note 1) .... 5.5 V
Voltage applied to disabled output (see Note 1) .... 5.5 V
Operating free-air temperature range .... 0°C to 75°C
Storage temperature range .... −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage (see Note 2)		2		5.5	V
V_{IL}	Low-level input voltage (see Note 2)				0.8	V
I_{OH}	High-level output current				−3.2	mA
I_{OL}	Low-level output current				24	mA
f_{clock}	Clock frequency		0		62.5	MHz
t_w	Pulse duration, clock (see Note 2)	High	8			ns
		Low	8			
t_{su}	Setup time, input or feedback before clock↑		10			ns
t_h	Hold time, input or feedback after clock↑		0			ns
T_A	Operating free-air temperature		0	25	75	°C

NOTE 2: These are absolute voltage levels with respect to the ground pin of the device and include all overshoots due to system and/or tester noise. Testing these parameters should not be attempted without suitable equipment.

electrical characteristics over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.75 V,	I_I = −18 mA			−0.8	−1.5	V
V_{OH}	V_{CC} = 4.75 V,	I_{OH} = −3.2 mA		2.4	3.2		V
V_{OL}	V_{CC} = 4.75 V,	I_{OL} = 24 mA			0.3	0.5	V
I_{OZH}‡	V_{CC} = 5.25 V,	V_O = 2.4 V				100	µA
I_{OZL}‡	V_{CC} = 5.25 V,	V_O = 0.4 V				−100	µA
I_I	V_{CC} = 5.25 V,	V_I = 5.5 V				0.2	mA
I_{IH}‡	V_{CC} = 5.25 V,	V_I = 2.4 V				25	µA
I_{IL}‡	V_{CC} = 5.25 V,	V_I = 0.4 V			−0.08	−0.25	mA
I_{OS}§	V_{CC} = 5.25 V,	V_O = 0		−30	−70	−130	mA
I_{CC}	V_{CC} = 5.25 V,	V_I = 0,	Outputs open		140	180	mA
C_i	f = 1 MHz,	V_I = 2 V			5		pF
C_o	f = 1 MHz,	V_O = 2 V			6		pF
$C_{i/o}$	f = 1 MHz,	$V_{I/O}$ = 2 V			7.5		pF
C_{clk}	f = 1 MHz,	V_{CLK} = 2 V			6		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ I/O leakage is the worst case of I_{OZL} and I_{IL} or I_{OZH} and I_{IH} respectively.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	TYP†	MAX	UNIT
f_{max}	With feedback		R1 = 200 Ω, R2 = 390 Ω, See Figure 3	55.5	80		MHz
	Without feedback			62.5	85		
t_{pd}	I, I/O	O, I/O		3	7	10	ns
t_{pd}	CLK↑	Q		2	5	8	ns
t_{en}	OE↓	Q		1	4	10	ns
t_{dis}	OE↑	Q		1	4	10	ns
t_{en}	I, I/O	O, I/O		3	8	10	ns
t_{dis}	I, I/O	O, I/O		3	8	10	ns

† All typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

‡ $f_{max}(\text{with feedback}) = \dfrac{1}{t_{su} + t_{pd}\ (\text{CLK to Q})}$, $f_{max}(\text{without feedback}) = \dfrac{1}{t_w\ \text{high} + t_w\ \text{low}}$

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (see Note 1)	5.5 V
Voltage applied to disabled output (see Note 1)	5.5 V
Operating free-air temperature range	–55°C to 125°C
Storage temperature range	–65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				–2	mA
I_{OL}	Low-level output current				12	mA
f_{clock}†	Clock frequency		0		56	MHz
t_w	Pulse duration, clock (see Note 2)	High	9			ns
		Low	9			
t_{su}†	Setup time, input or feedback before clock↑		11			ns
t_h†	Hold time, input or feedback after clock↑		0			ns
T_A	Operating free-air temperature		–55	25	125	°C

NOTE 2: These are absolute voltage levels with respect to the ground pin of the device and include all overshoots due to system and/or tester noise. Testing these parameters should not be attempted without suitable equipment.

electrical characteristics over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA			–0.8	–1.5	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = –2 mA		2.4	3.2		V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA			0.3	0.5	V
I_{OZH}‡	V_{CC} = 5.5 V,	V_O = 2.4 V				100	µA
I_{OZL}‡	V_{CC} = 5.5 V,	V_O = 0.4 V				–100	µA
I_I	V_{CC} = 5.5 V,	V_I = 5.5 V				0.2	mA
I_{IH}‡	V_{CC} = 5.5 V,	V_I = 2.4 V				25	µA
I_{IL}‡	V_{CC} = 5.5 V,	V_I = 0.4 V			–0.08	–0.25	mA
I_{OS}§	V_{CC} = 5.5 V,	V_O = 0.5 V		–30	–70	–250	mA
I_{CC}	V_{CC} = 5.5 V,	V_I = GND,	Outputs open		140	220	mA
C_i	f = 1 MHz,	V_I = 2 V			5		pF
C_o	f = 1 MHz,	V_O = 2 V			6		pF
$C_{i/o}$	f = 1 MHz,	$V_{I/O}$ = 2 V			7.5		pF
C_{clk}	f = 1 MHz,	V_{CLK} = 2 V			6		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ I/O leakage is the worst case of I_{OZL} and I_{IL} or I_{OZH} and I_{IH} respectively.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second. V_O is set at 0.5 V to avoid test problems caused by test equipment ground degradation.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	TYP†	MAX	UNIT
f_{max}	With feedback		R1 = 390 Ω, R2 = 750 Ω, See Figure 3	48	80		MHz
	Without feedback			56	85		
t_{pd}	I, I/O	O, I/O		3	7	12	ns
t_{pd}	CLK↑	Q		2	5	10	ns
t_{en}	OE↓	Q		1	4	10	ns
t_{dis}	OE↑	Q		1	4	10	ns
t_{en}	I, I/O	O, I/O		3	8	14	ns
t_{dis}	I, I/O	O, I/O		2	8	12	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ $f_{max}(\text{with feedback}) = \dfrac{1}{t_{su} + t_{pd}\ (\text{CLK to Q})}$, $f_{max}(\text{without feedback}) = \dfrac{1}{t_w\ \text{high} + t_w\ \text{low}}$

programming information

Texas Instruments programmable logic devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments programmable logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

preload procedure for registered outputs (see Figure 1 and Note 3)

The output registers can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below.

Step 1. With V_{CC} at 5 volts and Pin 1 at V_{IL}, raise Pin 11 to V_{IHH}.
Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.
Step 3. Pulse Pin 1, clocking in preload data.
Step 4. Remove output voltage, then lower Pin 11 to V_{IL}. Preload can be verified by observing the voltage level at the output pin.

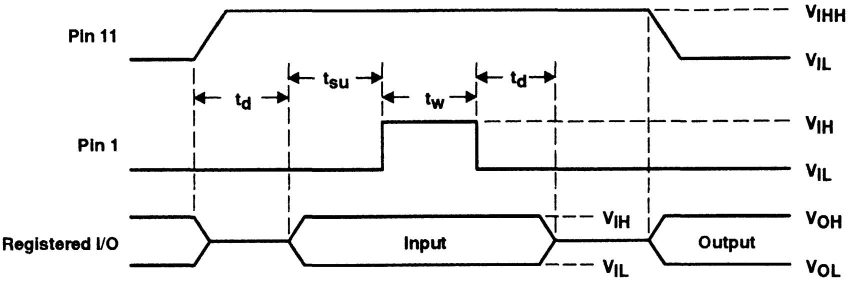
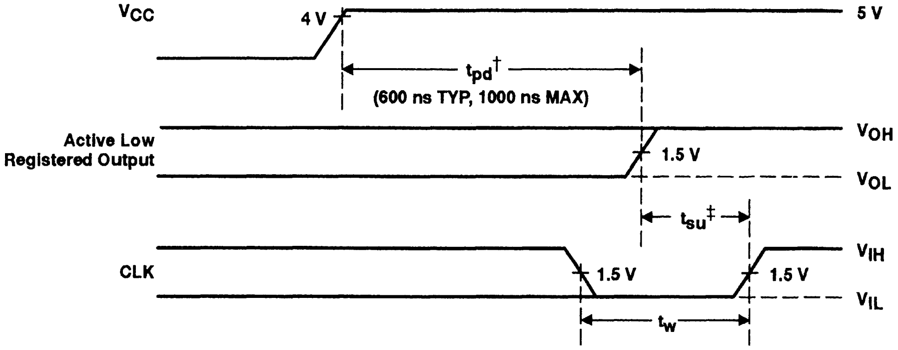


Figure 1. Preload Waveforms

NOTE 3: $t_d = t_{su} = t_h$ = 100 ns to 1000 ns V_{IHH} = 10.25 V to 10.75 v

power-up reset (see Figure 2)

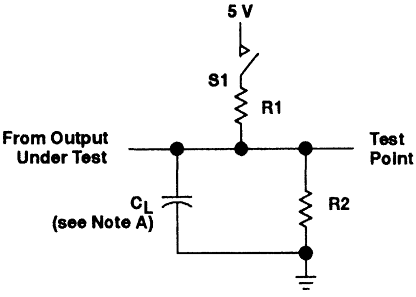
Following power up, all registers are reset to zero. This feature provides extra flexibility to the system designer and is especially valuable in simplifying state-machine initialization. To ensure a valid power-up reset, it is important that the rise of V_{CC} be monotonic. Following power-up reset, a low-to-high clock transition must not occur until all applicable input and feedback setup times are met.



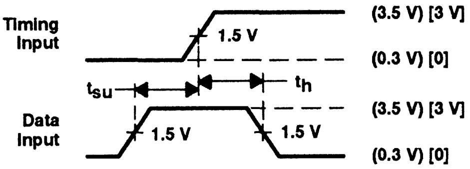
[†] This is the power-up reset time and applies to registered outputs only. The values shown are from characterization data.
[‡] This is the setup time for input or feedback.

Figure 2. Power-Up Reset Waveforms

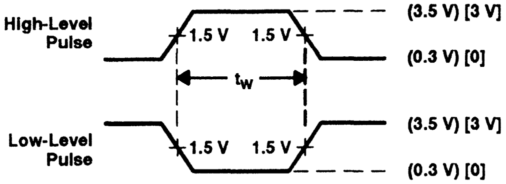
PARAMETER MEASUREMENT INFORMATION



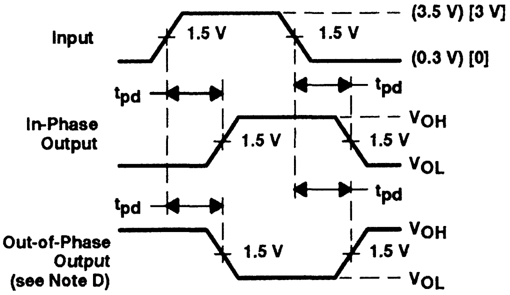
LOAD CIRCUIT FOR
3-STATE OUTPUTS



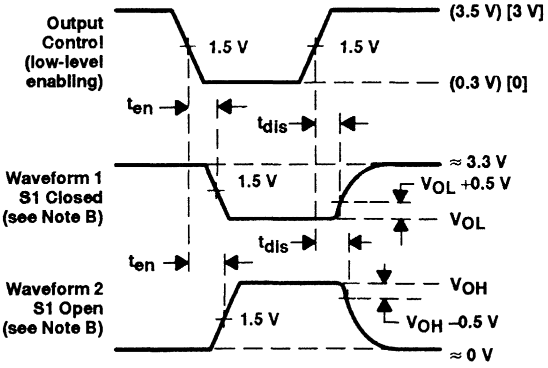
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses have the following characteristics: For C suffix, use the voltage levels indicated in parentheses ( ), PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%; For M suffix, use the voltage levels indicated in brackets [ ], PRR ≤ 10 MHz, t_r and $t_f \le 2$ ns, duty cycle = 50%

D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.

E. Equivalent loads may be used for testing.

Figure 3. Load Circuit and Voltage Waveforms

metastable characteristics of TIBPAL16R4-10C, TIBPAL16R6-10C, and TIBPAL16R8-10C

At some point a system designer is faced with the problem of synchronizing two digital signals operating at two different frequencies. This problem is typically overcome by synchronizing one of the signals to the local clock through use of a flip-flop. However, this solution presents an awkward dilemma since the setup and hold time specifications associated with the flip-flop are sure to be violated. The metastable characteristics of the flip-flop can influence overall system reliability.

Whenever the setup and hold times of a flip-flop are violated, its output response becomes uncertain and is said to be in the metastable state if the output hangs up in the region between V_{IL} and V_{IH}. This metastable condition lasts until the flip-flop falls into one of its two stable states, which takes longer than the specified maximum propagation delay time (CLK to Q max).

From a system engineering standpoint, a designer cannot use the specified data sheet maximum for propagation delay time when using the flip-flop as a data synchronizer – how long to wait after the specified data sheet maximum must be known before using the data in order to guarantee reliable system operation.

The circuit shown in Figure 4 can be used to evaluate MTBF (Mean Time Between Failure) and Δt for a selected flip-flop. Whenever the Q output of the DUT is between 0.8 V and 2 V, the comparators are in opposite states. When the Q output of the DUT is higher than 2 V or lower than 0.8 V, the comparators are at the same logic level. The outputs of the two comparators are sampled a selected time (Δt) after SCLK. The exclusive OR gate detects the occurrence of a failure and increments the failure counter.

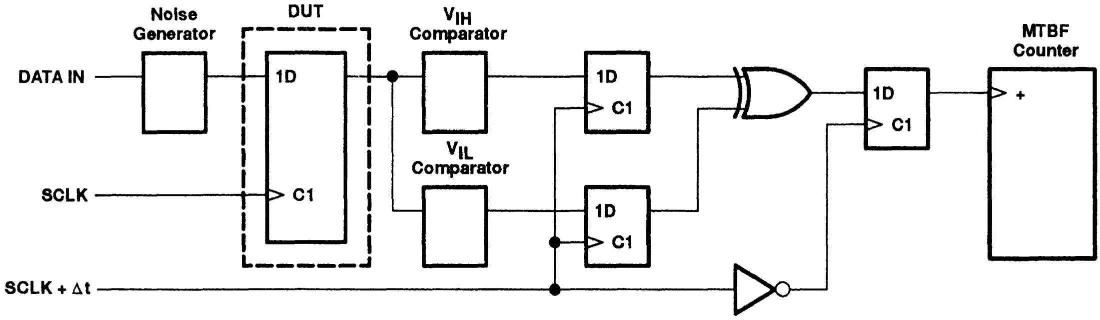
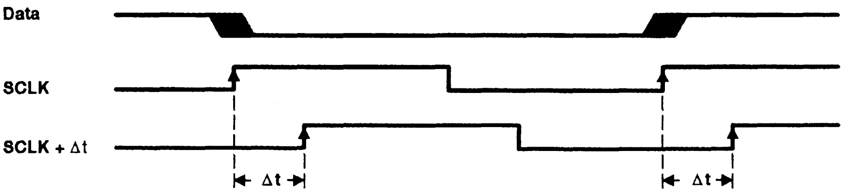


Figure 4. Metastable Evaluation Test Circuit

In order to maximize the possibility of forcing the DUT into a metastable state, the input data signal is applied so that it always violates the setup and hold time. This condition is illustrated in the timing diagram in Figure 5. Any other relationship of SCLK to data will provide less chance for the device to enter into the metastable state.



$$\text{MTBF} = \frac{\text{Time (sec)}}{\text{\# Failures}}$$

$$t_{rec} = \Delta t - \text{CLK to Q (max)}$$

Figure 5. Timing Diagram

By using the described test circuit, MTBF can be determined for several different values of Δt (see Figure 4). Plotting this information on semilog scale demonstrates the metastable characteristics of the selected flip-flop. Figure 6 shows the results for the TIBPAL16'-10C operating at 1 MHz.

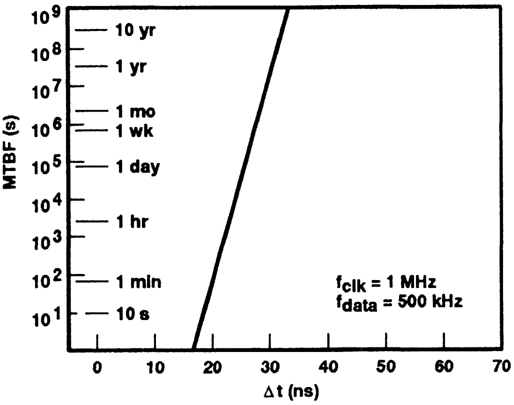


Figure 6. Metastable Characteristics

From the data taken in the above experiment, an equation can be derived for the metastable characteristics at other clock frequencies.

The metastable equation: $\frac{1}{MTBF} = f_{SCLK} \times f_{data} \times C1 \; e^{(-C2 \times \Delta t)}$

The constants C1 and C2 describe the metastable characteristics of the device. From the experimental data, these constants can be solved for: $C1 = 9.15 \times 10^{-7}$ and $C2 = 0.959$

Therefore

$$\frac{1}{MTBF} = f_{SCLK} \times f_{data} \times 9.15 \times 10^{-7} \; e^{(-0.959 \times \Delta t)}$$

definition of variables

DUT (Device Under Test): The DUT is a 10-ns registered PLD programmed with the equation Q : = D.

MTBF (Mean Time Between Failures): The average time (s) between metastable occurrences that cause a violation of the device specifications.

f_{SCLK} (system clock frequency): Actual clock frequency for the DUT.

f_{data} (data frequency): Actual data frequency for a specified input to the DUT.

C1: Calculated constant that defines the magnitude of the curve.

C2: Calculated constant that defines the slope of the curve.

t_{rec} (metastability recovery time): Minimum time required to guarantee recovery from metastability, at a given MTBF failure rate. $t_{rec} = \Delta t - t_{pd}$ (CLK to Q, max)

Δt: The time difference (ns) from when the synchronizing flip-flop is clocked to when its output is sampled.

The test described above has shown the metastable characteristics of the TIBPAL16R4/R6/R8-10C series. For additional information on metastable characteristics of Texas Instruments logic circuits, please refer to TI Applications publication SDAA004, "Metastable Characteristics, Design Considerations for ALS, AS, and LS Circuits."

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

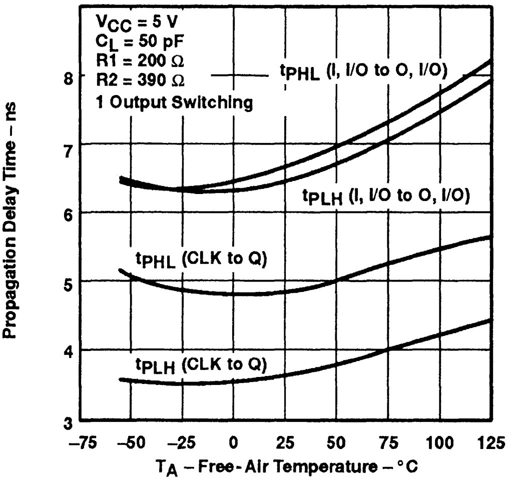


Figure 7

PROPAGATION DELAY TIME
vs
SUPPLY VOLTAGE

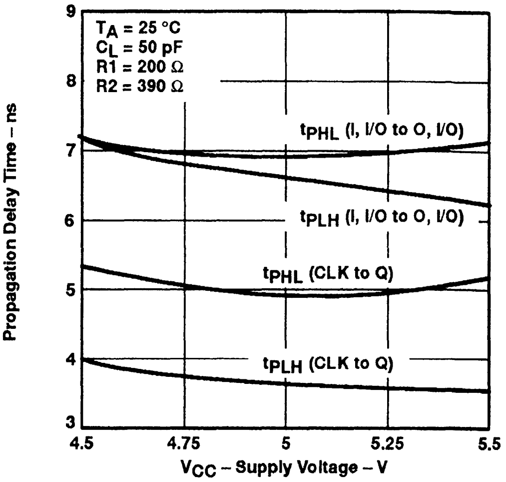


Figure 8

PROPAGATION DELAY TIME
vs
NUMBER OF OUTPUTS SWITCHING

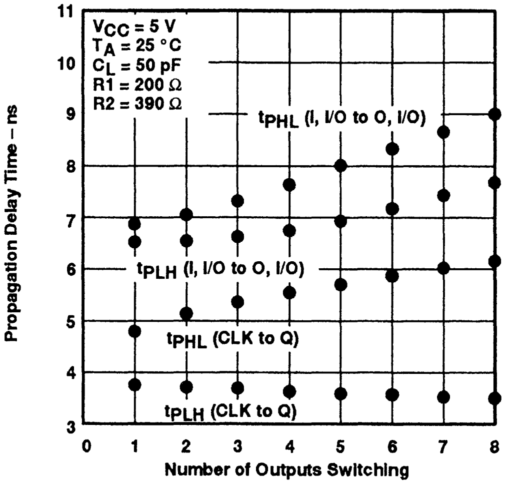


Figure 9

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME vs LOAD CAPACITANCE

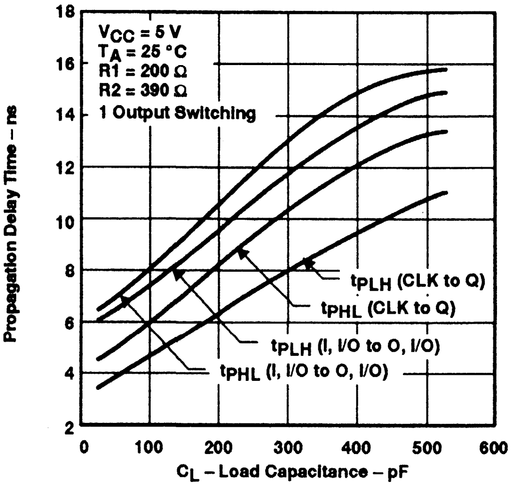


Figure 10

POWER DISSIPATION vs FREQUENCY 8-BIT COUNTER MODE

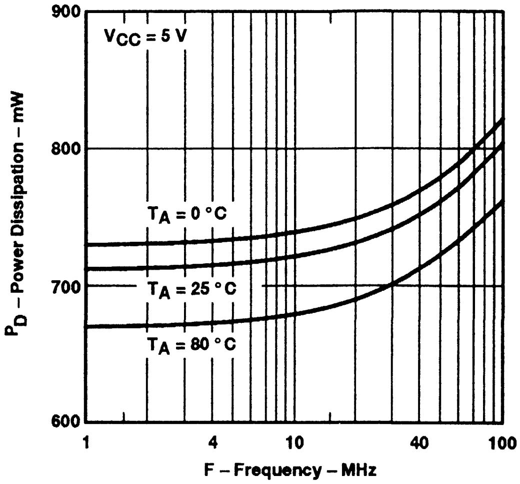


Figure 11

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

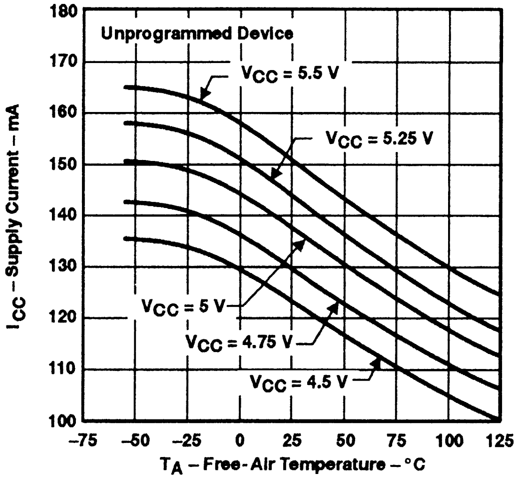


Figure 12

TIBPAL16L8-15M, TIBPAL16R4-15M, TIBPAL16R6-15M, TIBPAL16R8-15M
HIGH-PERFORMANCE *IMPACT*™ *PAL*® CIRCUITS

SRPS018 – D3338, JANUARY 1986 – REVISED MARCH 1992

- **High-Performance Operation:**
  Propagation Delay . . . 15 ns Max
- **Power-Up Clear on Registered Devices (All Register Outputs are Set High, but Voltage Levels at the Output Pins Go Low)**
- **Package Options Include Ceramic DIPs and Ceramic Chip Carriers**
- **Dependable Texas Instruments Quality and Reliability**

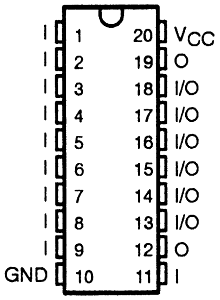
DEVICE	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
PAL16L8	10	2	0	6
PAL16R4	8	0	4 (3-state buffers)	4
PAL16R6	8	0	6 (3-state buffers)	2
PAL16R8	8	0	8 (3-state buffers)	0

description

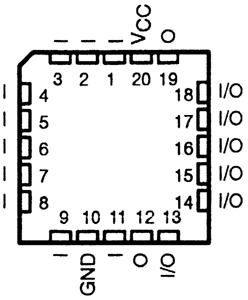
These programmable array logic devices feature high speed and functional equivalency when compared with currently available devices. These IMPACT-X™ circuits combine the latest Advanced Low-Power Schottky technology with proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional TTL logic. Their easy programmability allows for quick design of custom functions and typically results in a more compact circuit board. In addition, chip carriers are available for futher reduction in board space.

The TIBPAL16' M series is characterized for operation over the full military temperature range of –55°C to 125°C.

TIBPAL16L8'
J OR W PACKAGE
(TOP VIEW)



TIBPAL16L8'
FK PACKAGE
(TOP VIEW)



Pin assignments in operating mode

IMPACT is a trademark of Texas Instruments Incorporated.
PAL is a registered trademark of Advanced Micro Devices Inc.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

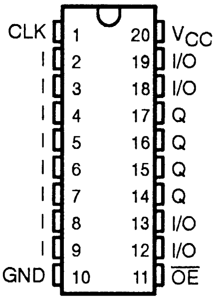
Copyright © 1992, Texas Instruments Incorporated

TEXAS INSTRUMENTS

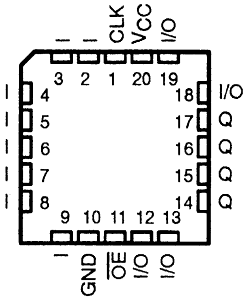
TIBPAL16R4-15M, TIBPAL16R6-15M, TIBPAL16R8-15M
HIGH-PERFORMANCE *IMPACT*™ *PAL*® CIRCUITS

SRPS018 – D3338, JANUARY 1986 – REVISED MARCH 1992

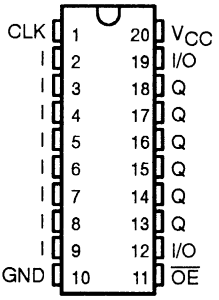
TIBPAL16R4'
J OR W PACKAGE
(TOP VIEW)



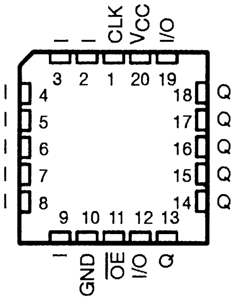
TIBPAL16R4'
FK PACKAGE
(TOP VIEW)



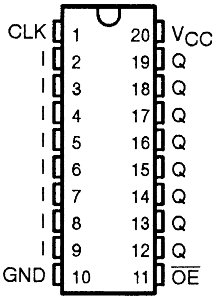
TIBPAL16R6'
J OR W PACKAGE
(TOP VIEW)



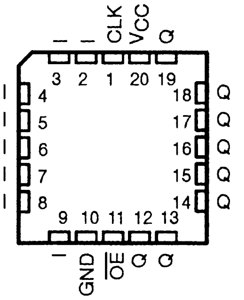
TIBPAL16R6'
FK PACKAGE
(TOP VIEW)



TIBPAL16R8'
J OR W PACKAGE
(TOP VIEW)



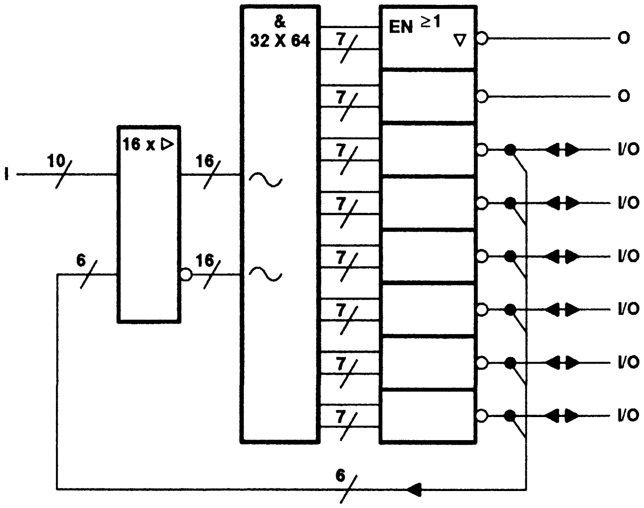
TIBPAL16R8'
FK PACKAGE
(TOP VIEW)



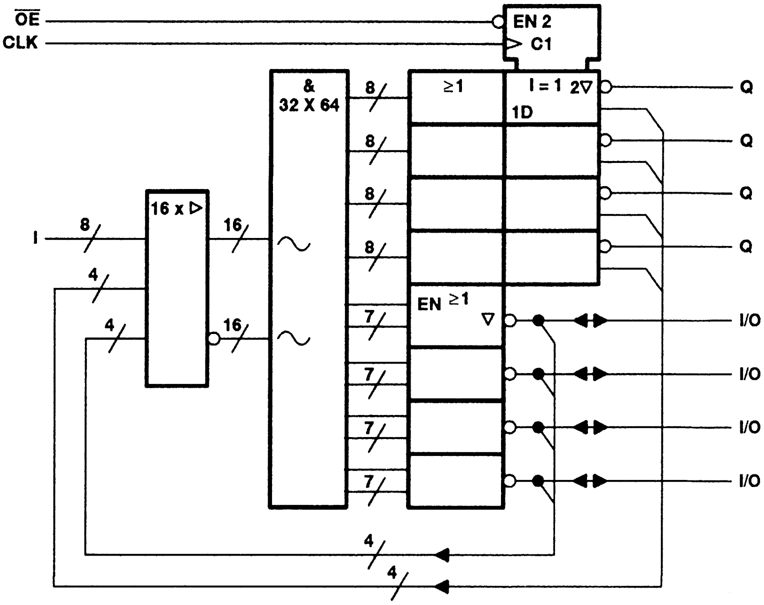
Pin assignments in operating mode

functional block diagrams (positive logic)

TIBPAL16L8'



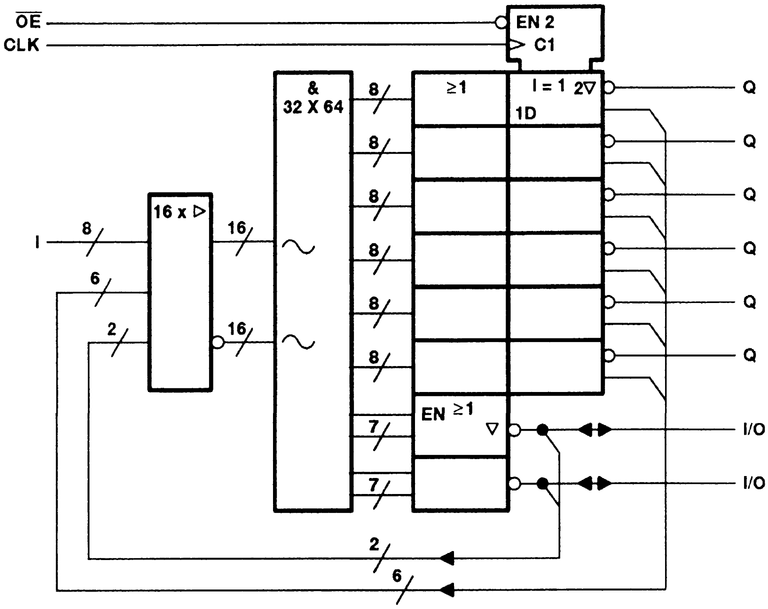
TIBPAL16R4'



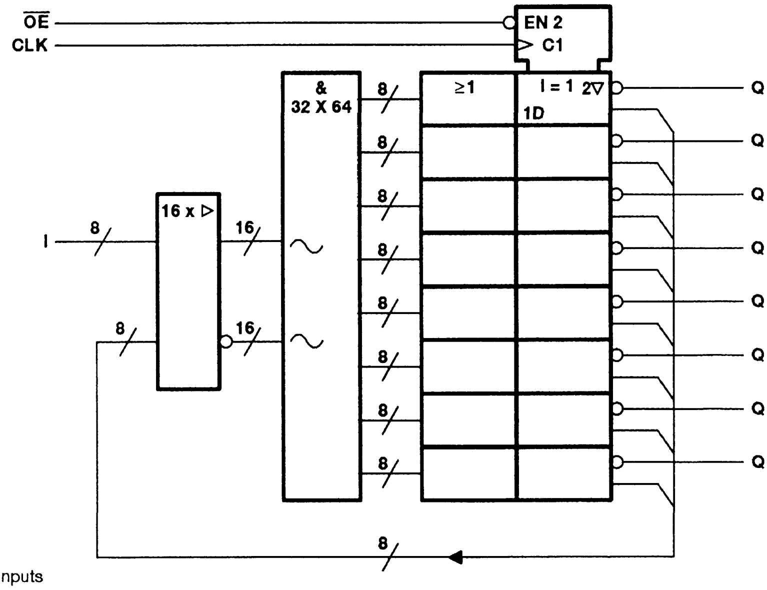
∿ denotes fused inputs

functional block diagrams (positive logic)

TIBPAL16R6'

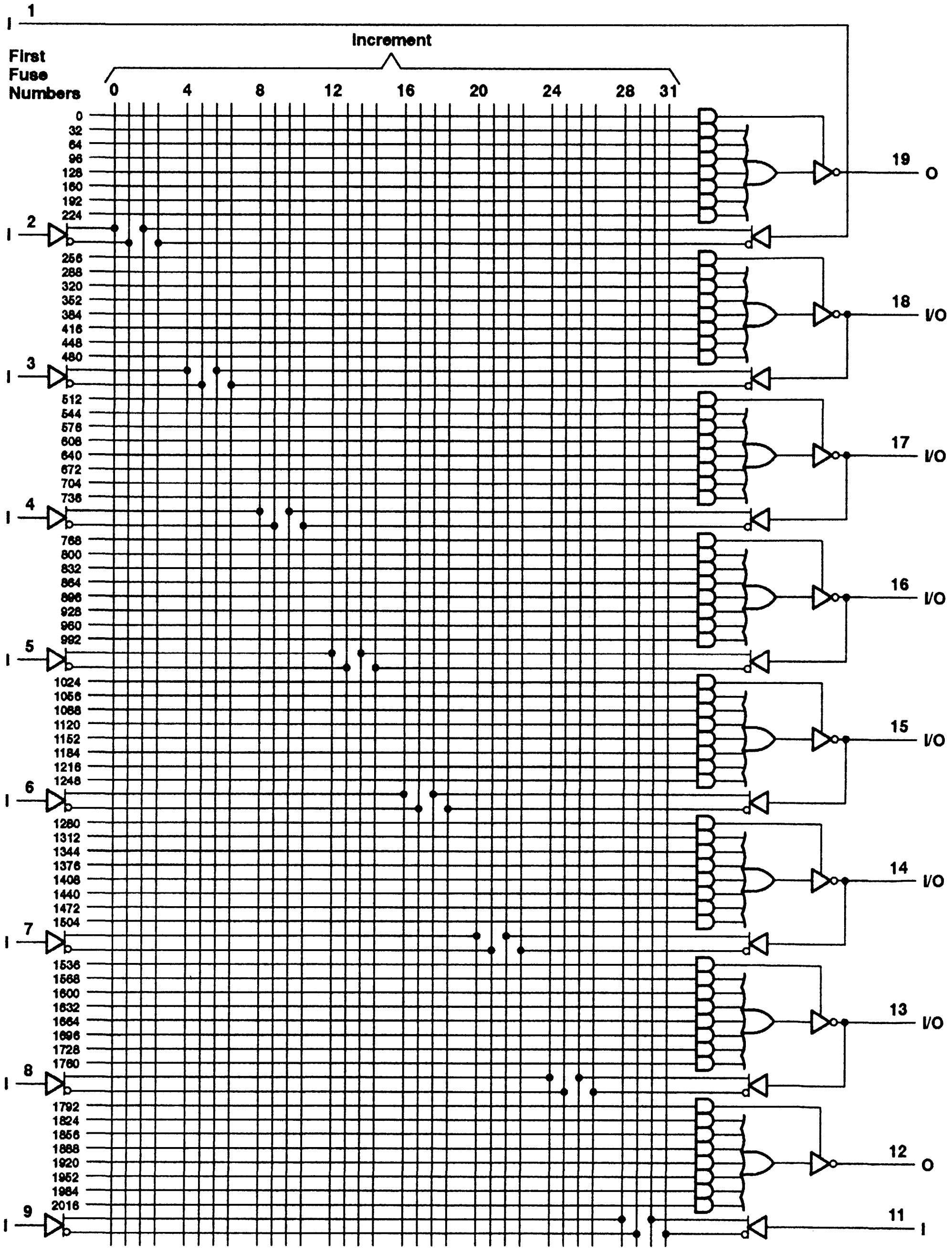


TIBPAL16R8'



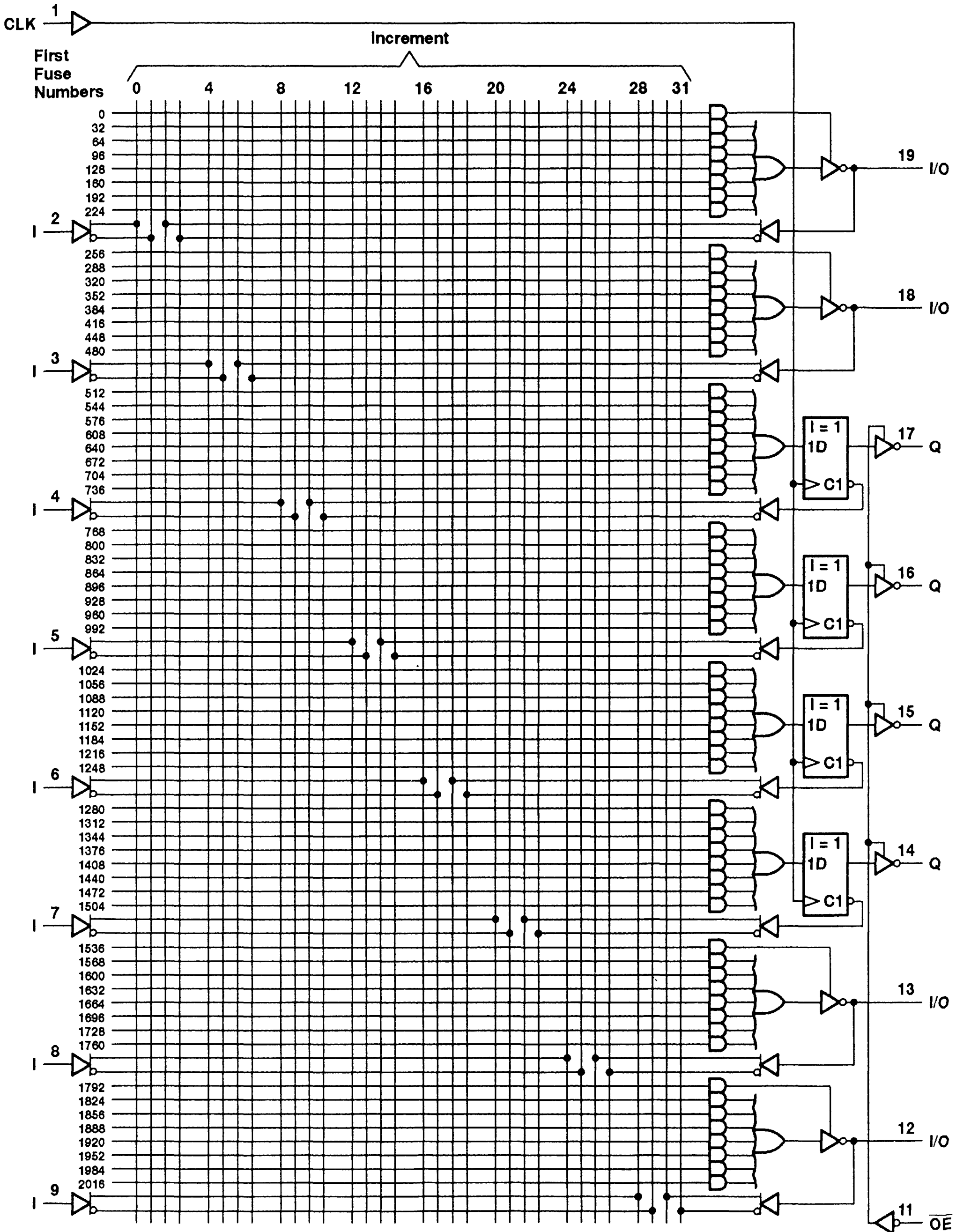
∿ denotes fused inputs

logic diagram (positive logic)



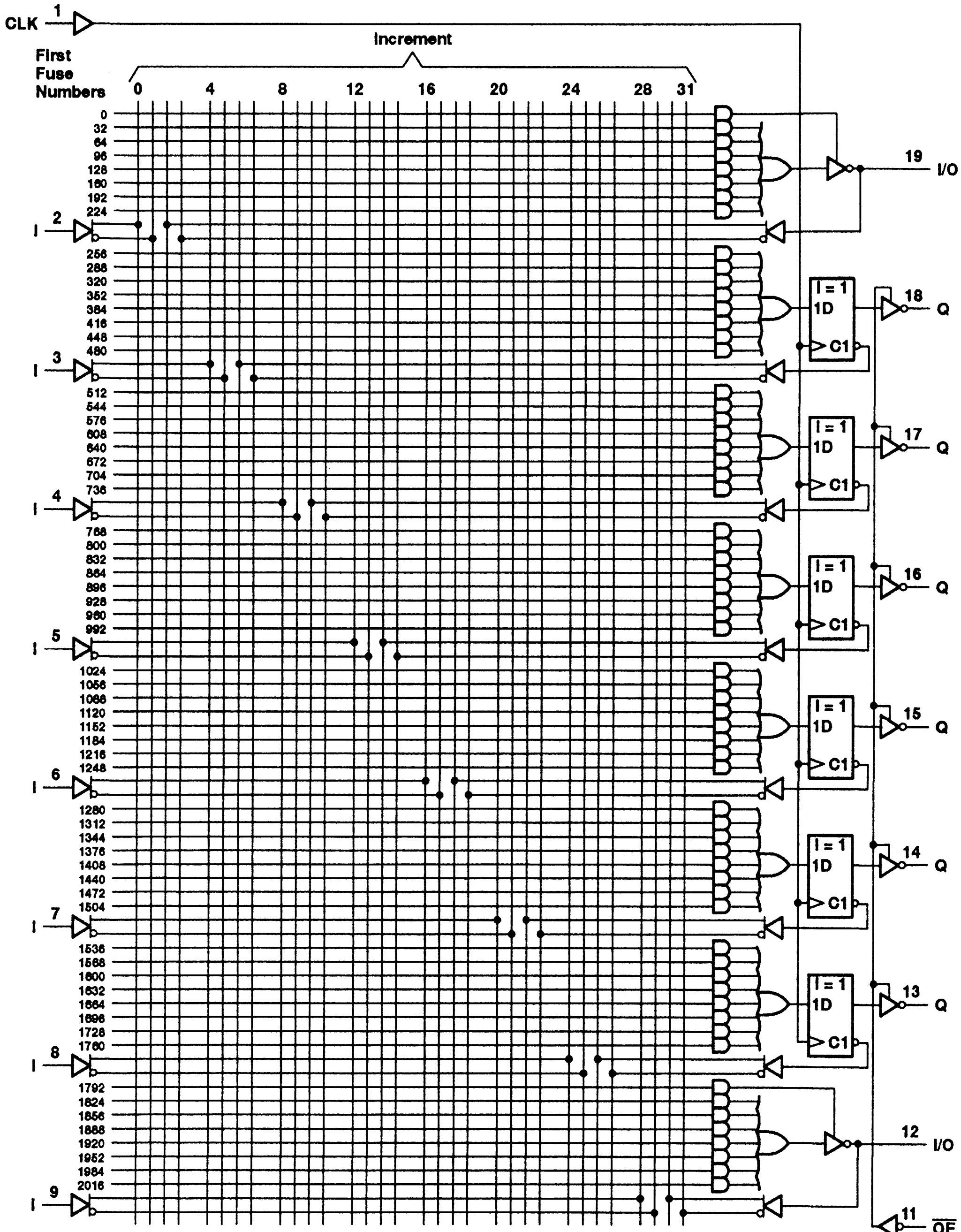
Fuse number = First fuse number + Increment

logic diagram (positive logic)



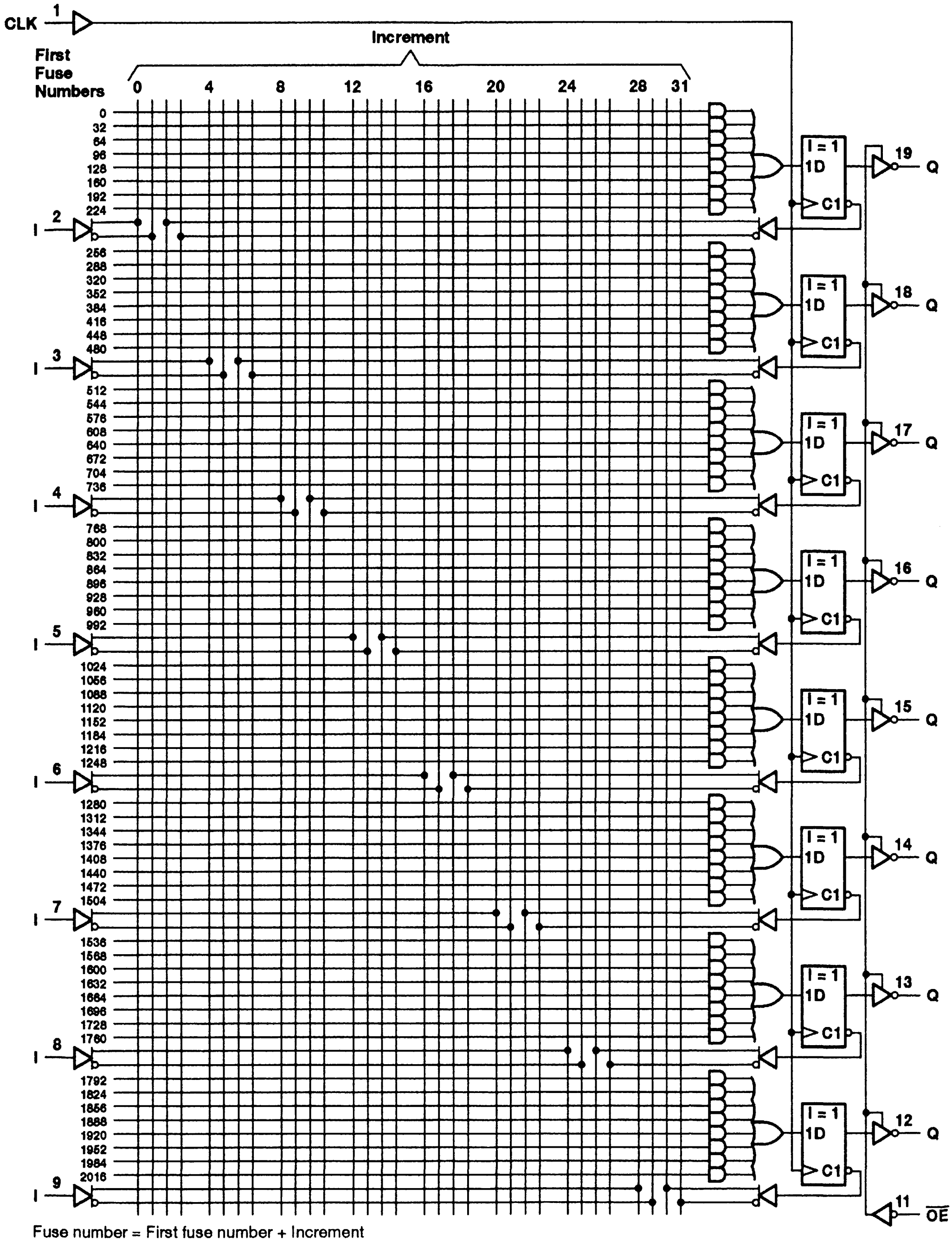
Fuse number = First fuse number + Increment

logic diagram (positive logic)



Fuse number = First fuse number + Increment

logic diagram (positive logic)



Fuse number = First fuse number + Increment

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) .... 7 V
Input voltage (see Note 1) .... 5.5 V
Voltage applied to disabled output (see Note 1) .... 5.5 V
Operating free-air temperature range .... –55°C to 125°C
Storage temperature range .... –65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				–2	mA
I_{OL}	Low-level output current				12	mA
f_{clock}	Clock frequency		0		50	MHz
t_w	Pulse duration, clock (see Note 2)	High	9			ns
		Low	10			
t_{su}	Setup time, input or feedback before clock↑		15			ns
t_h	Hold time, input or feedback after clock↑		0			ns
T_A	Operating free-air temperature		–55	25	125	°C

NOTE 2: The total clock period of clock high and clock low must not exceed clock frequency, f_{clock}. The minimum pulse durations specified are only for clock high or low, but not for both simultaneously.

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS			MIN	TYP[†]	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA				–1.5	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = –2 mA		2.4	3.3		V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA			0.35	0.5	V
I_{OZH}	Outputs	V_{CC} = 5.5 V,	V_O = 2.7 V				20	μA
	I/O ports						100	
I_{OZL}	Outputs	V_{CC} = 5.5 V,	V_O = 0.4 V				–20	μA
	I/O ports						–250	
I_I	Pin 1, 11	V_{CC} = 5.5 V,	V_I = 5.5 V				0.2	mA
	All others						0.1	
I_{IH}	Pin 1, 11	V_{CC} = 5.5 V,	V_I = 2.7 V				50	μA
	I/O ports						100	
	All others						20	
I_{IL}	I/O ports	V_{CC} = 5.5 V,	V_I = 0.4 V				–0.25	mA
	All others						–0.2	
I_{OS}[‡]		V_{CC} = 5.5 V,	V_O = 0.5 V		–30		–250	mA
I_{CC}		V_{CC} = 5.5 V,	V_I = 0,	Outputs open		170	220	mA

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C.
[‡] Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second. Set V_O at 0.5 V to avoid test equipment degradation.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	TYP†	MAX	UNIT
f_{max}‡			R1 = 390 Ω, R2 = 750 Ω, See Figure 1	50			MHz
t_{pd}	I, I/O	O, I/O			8	15	ns
t_{pd}	CLK↑	Q			7	12	ns
t_{en}	OE↓	Q			8	12	ns
t_{dis}	OE↑	Q			7	12	ns
t_{en}	I, I/O	O, I/O			8	15	ns
t_{dis}	I, I/O	O, I/O			8	15	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

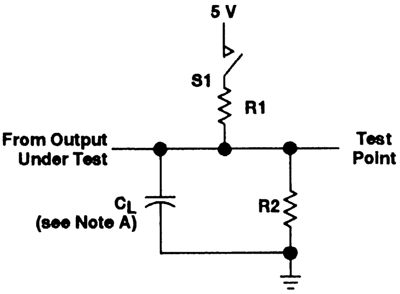
‡ Maximum operating frequency and propagation delay are specified for the basic building block. When using feedback, limits must be calculated accordingly.

programming information

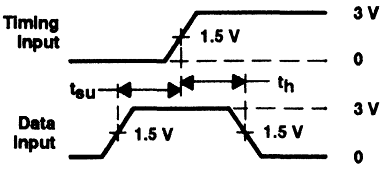
Texas Instruments programmable logic devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments programmable logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

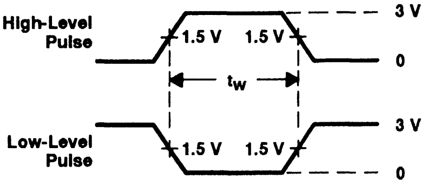
PARAMETER MEASUREMENT INFORMATION



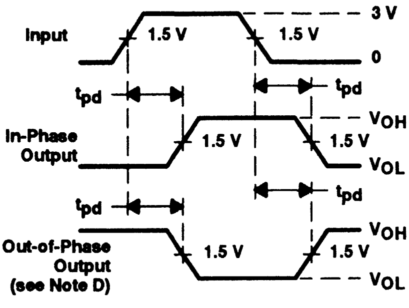
LOAD CIRCUIT FOR
3-STATE OUTPUTS



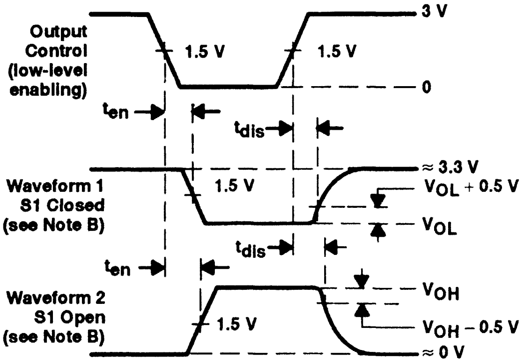
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES:
- A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses have the following characteristics: PRR ≤ 10 MHz, t_r and $t_f \le 2$ ns, duty cycle = 50%
- D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.
- E. Equivalent loads may be used for testing.

Figure 1. Load Circuit and Voltage Waveforms

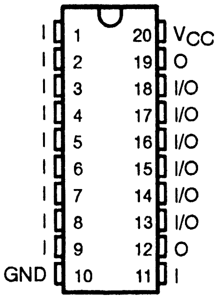
TIBPAL16L8-15C, TIBPAL16R4-15C, TIBPAL16R6-15C, TIBPAL16R8-15C
TIBPAL16L8-20M, TIBPAL16R4-20M, TIBPAL16R6-20M, TIBPAL16R8-20M
HIGH-PERFORMANCE *IMPACT*™ *PAL*® CIRCUITS

SRPS019 – D3340, FEBRUARY 1984 – REVISED MARCH 1992

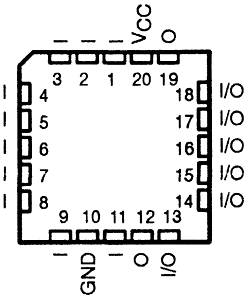
- **High-Performance Operation:**
  Propagation Delay
  C Suffix . . . 15 ns Max
  M Suffix . . . 20 ns Max
- **Functionally Equivalent, but Faster than PAL16L8A, PAL16R4A, PAL16R6A, and PAL16R8A**
- **Power-Up Clear on Registered Devices (All Register Outputs are Set High, but Voltage Levels at the Output Pins Go Low)**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

DEVICE	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
PAL16L8	10	2	0	6
PAL16R4	8	0	4 (3-state buffers)	4
PAL16R6	8	0	6 (3-state buffers)	2
PAL16R8	8	0	8 (3-state buffers)	0

TIBPAL16L8'
C SUFFIX . . . J OR N PACKAGE
M SUFFIX . . . J OR W PACKAGE
(TOP VIEW)



TIBPAL16L8'
C SUFFIX . . . FN PACKAGE
M SUFFIX . . . FK PACKAGE
(TOP VIEW)



description

These programmable array logic devices feature high speed and functional equivalency when compared with currently available devices. These IMPACT™ circuits combine the latest Advanced Low-Power Schottky technology with proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional TTL logic. Their easy programmability allows for quick design of custom functions and typically results in a more compact circuit board. In addition, chip carriers are available for futher reduction in board space.

The TIBPAL16' C series is characterized from 0°C to 75°C. The TIBPAL16' M series is characterized for operation over the full military temperature range of –55°C to 125°C.

These devices are covered by U.S. Patent 4,410,987.
IMPACT is a trademark of Texas Instruments Incorporated.
PAL is a registered trademark of Advanced Micro Devices Inc.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

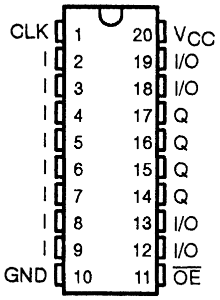
Copyright © 1992, Texas Instruments Incorporated

TIBPAL16R4-15C, TIBPAL16R6-15C, TIBPAL16R8-15C
TIBPAL16R4-20M, TIBPAL16R6-20M, TIBPAL16R8-20M
HIGH-PERFORMANCE *IMPACT*™ *PAL*® CIRCUITS

SRPS019 – D3340, FEBRUARY 1984 – REVISED MARCH 1992

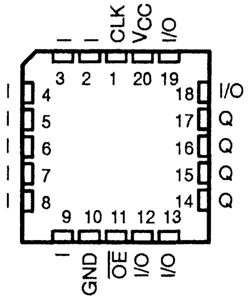
TIBPAL16R4'
C SUFFIX . . . J OR N PACKAGE
M SUFFIX . . . J OR W PACKAGE

(TOP VIEW)



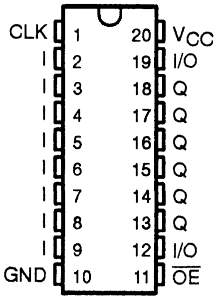
TIBPAL16R4'
C SUFFIX . . . FN PACKAGE
M SUFFIX . . . FK PACKAGE

(TOP VIEW)



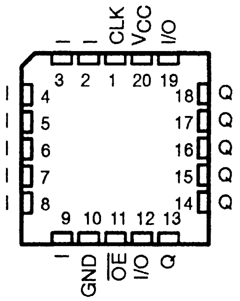
TIBPAL16R6'
C SUFFIX . . . J OR N PACKAGE
M SUFFIX . . . J OR W PACKAGE

(TOP VIEW)



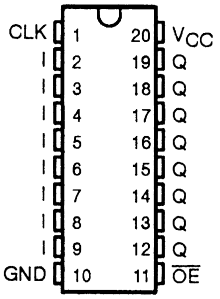
TIBPAL16R6'
C SUFFIX . . . FN PACKAGE
M SUFFIX . . . FK PACKAGE

(TOP VIEW)



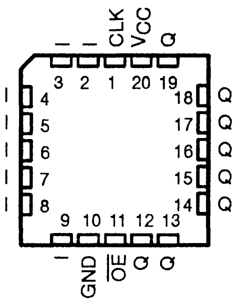
TIBPAL16R8'
C SUFFIX . . . J OR N PACKAGE
M SUFFIX . . . J OR W PACKAGE

(TOP VIEW)



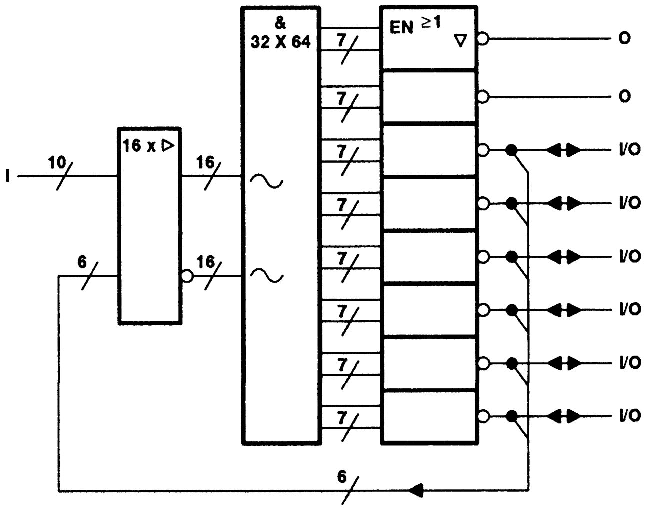
TIBPAL16R8'
C SUFFIX . . . FN PACKAGE
M SUFFIX . . . FK PACKAGE

(TOP VIEW)

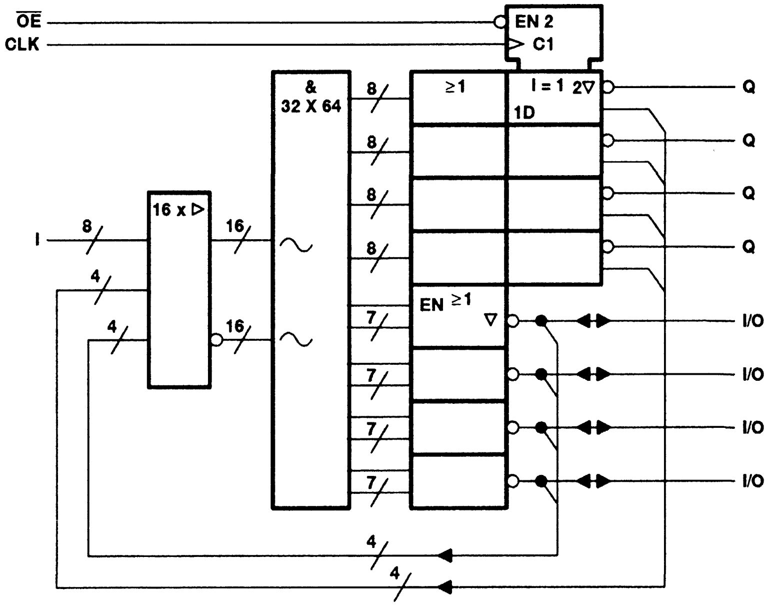


functional block diagrams (positive logic)

TIBPAL16L8'



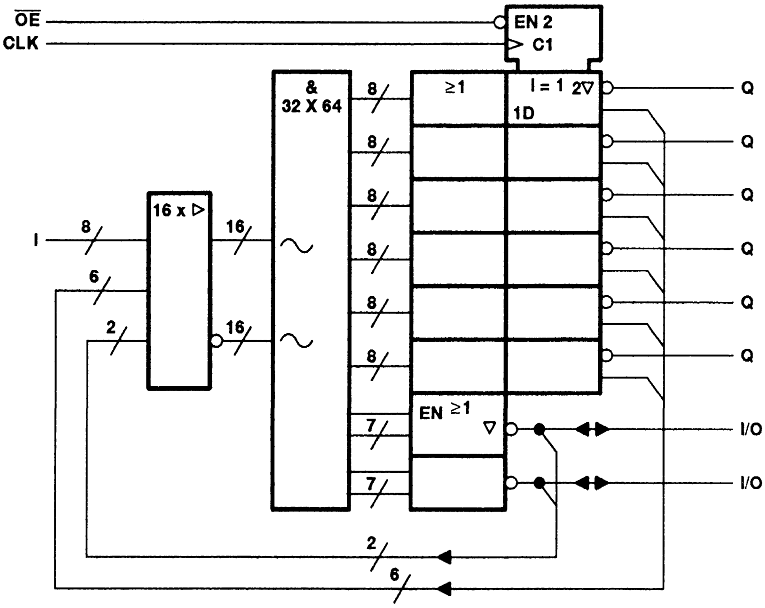
TIBPAL16R4'



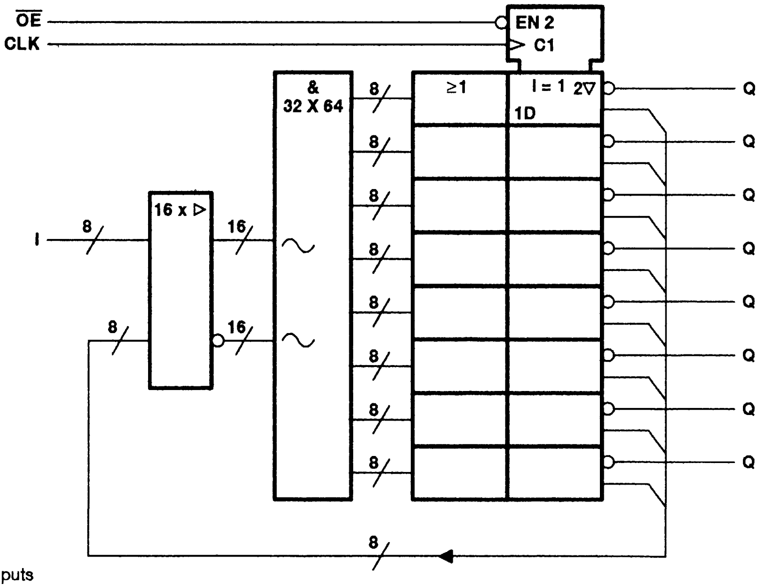
∿ denotes fused inputs

functional block diagrams (positive logic)

TIBPAL16R6'



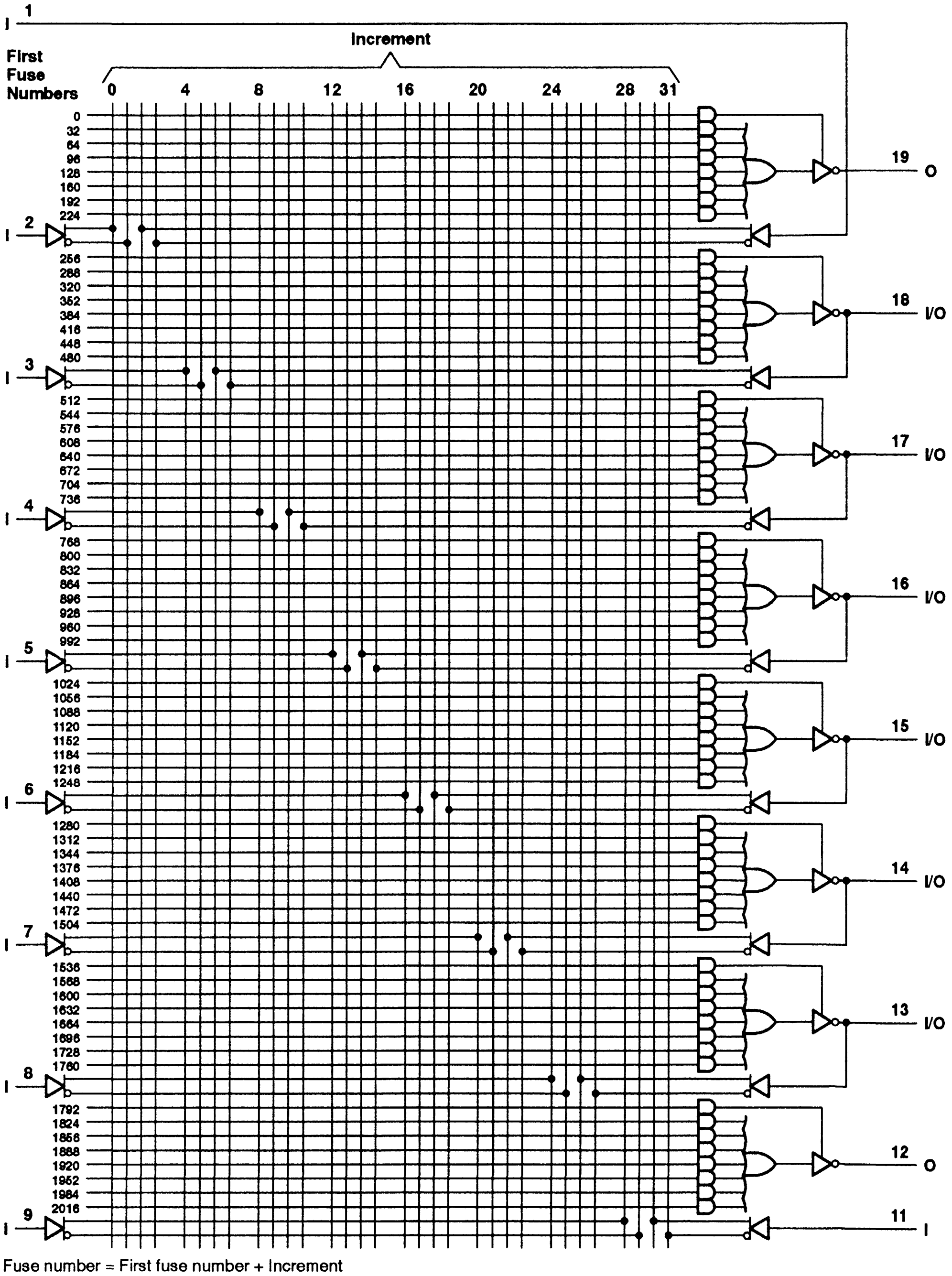
TIBPAL16R8'



∿ denotes fused inputs

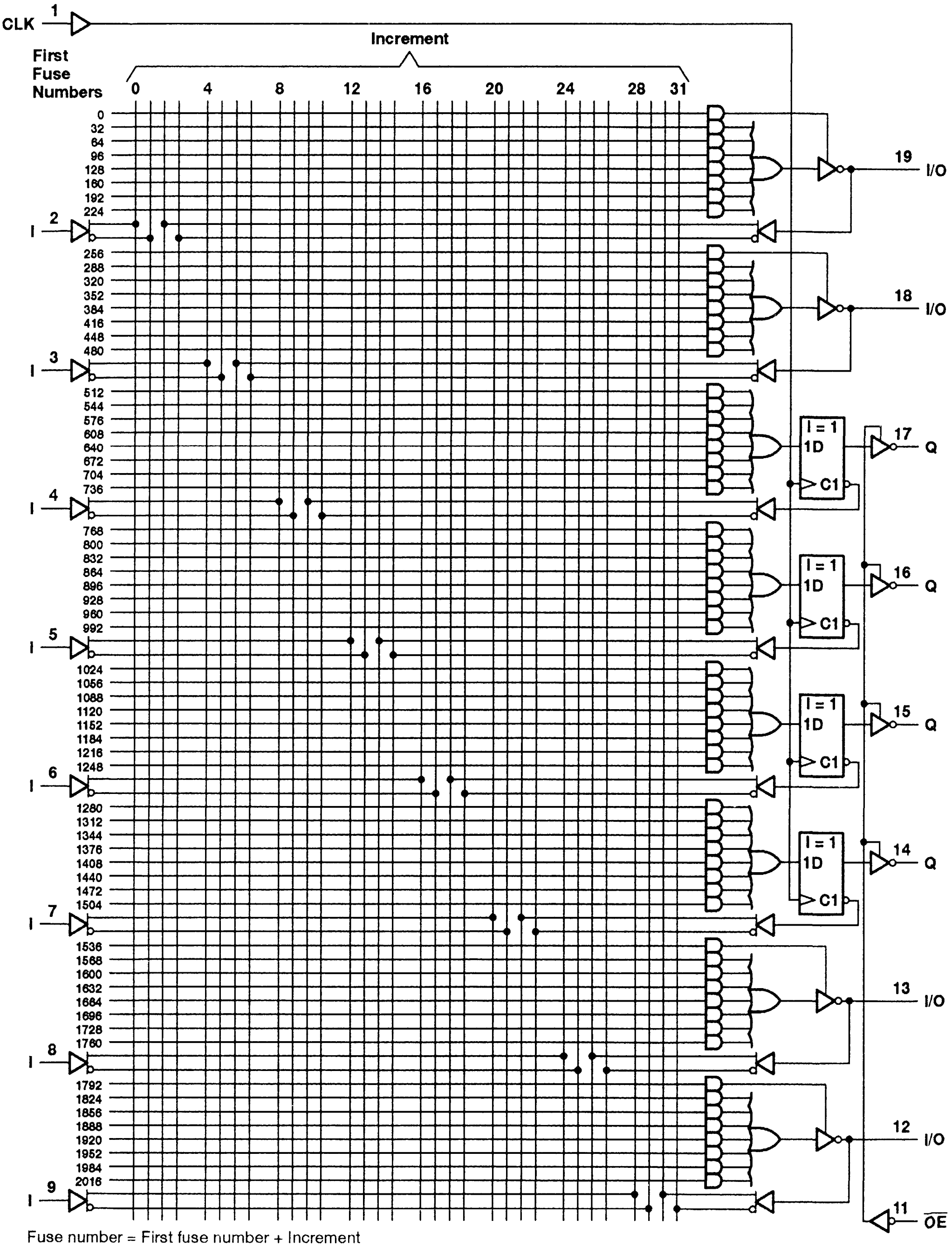
TEXAS INSTRUMENTS
POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

logic diagram (positive logic)



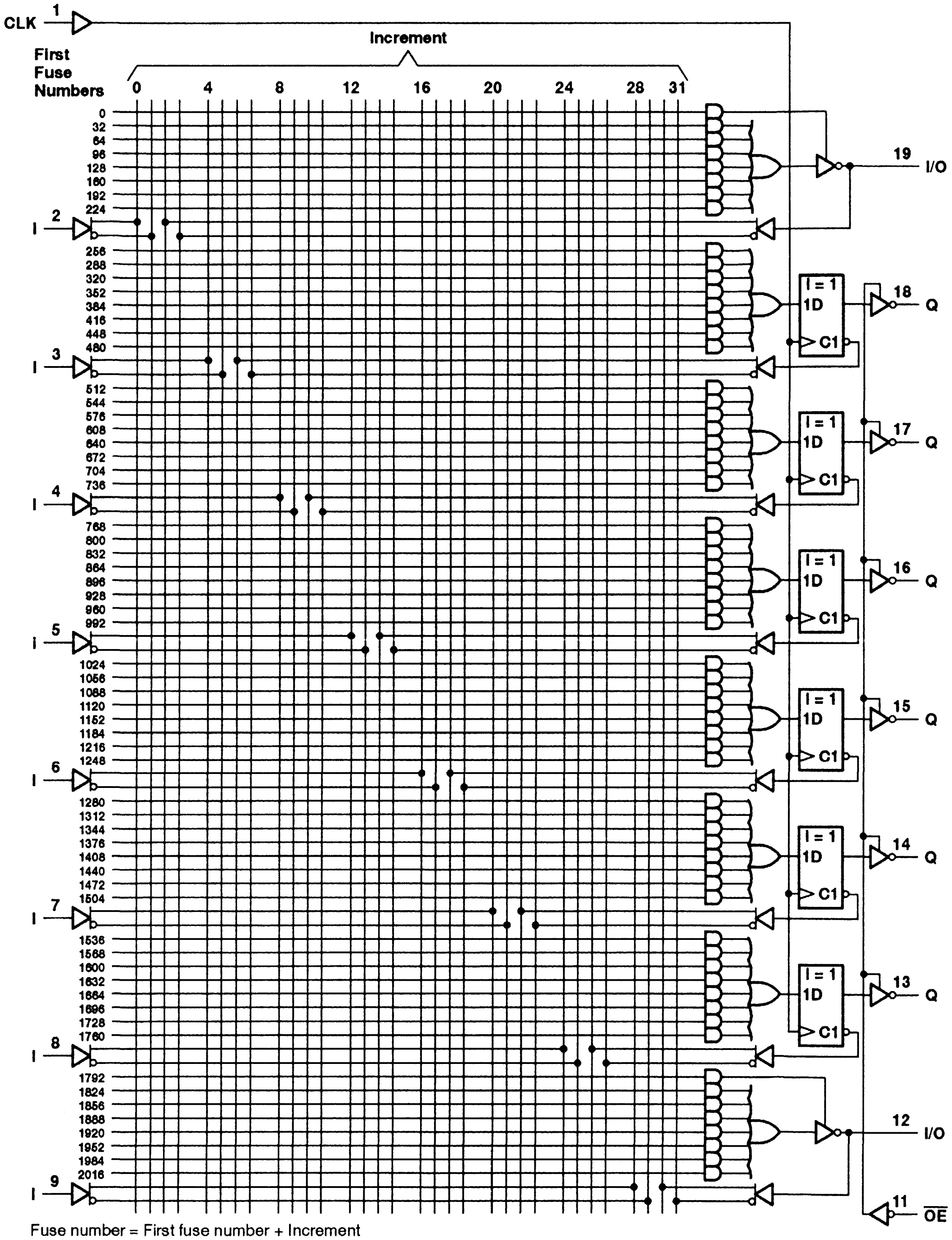
Fuse number = First fuse number + Increment

logic diagram (positive logic)



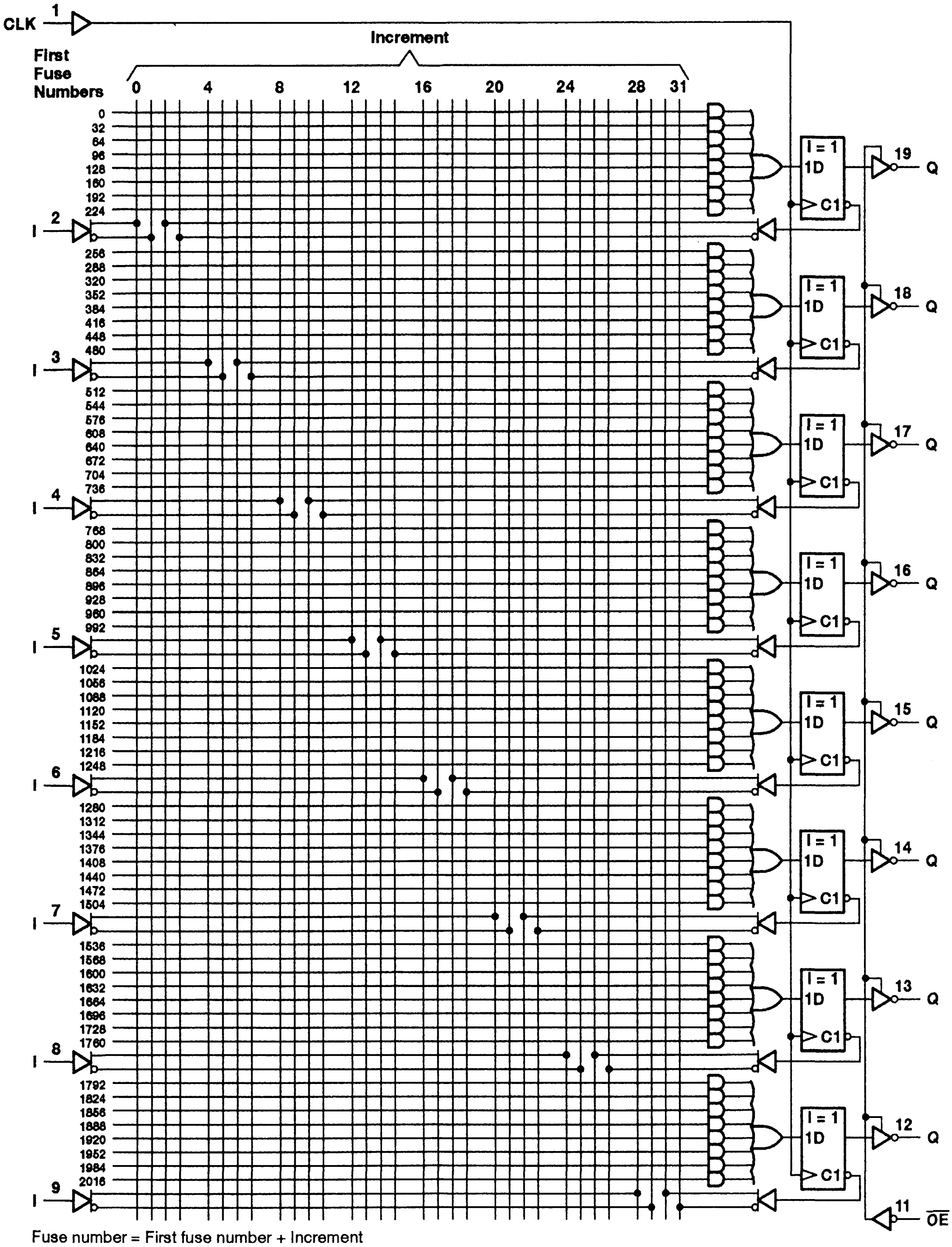
Fuse number = First fuse number + Increment

logic diagram (positive logic)



Fuse number = First fuse number + Increment

logic diagram (positive logic)



Fuse number = First fuse number + Increment

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) .... 7 V
Input voltage (see Note 1) .... 5.5 V
Voltage applied to disabled output (see Note 1) .... 5.5 V
Operating free-air temperature range .... 0°C to 75°C
Storage temperature range .... −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−3.2	mA
I_{OL}	Low-level output current				24	mA
f_{clock}	Clock frequency		0		50	MHz
t_w	Pulse duration, clock (see Note 2)	High	8			ns
		Low	9			
t_{su}	Setup time, input or feedback before clock↑		15			ns
t_h	Hold time, input or feedback after clock↑		0			ns
T_A	Operating free-air temperature		0	25	75	°C

NOTE 2: The total clock period of clock high and clock low must not exceed clock frequency, f_{clock}. The minimum pulse durations specified are only for clock high or low, but not for both simultaneously.

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS	MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.75 V, I_I = −18 mA			−1.5	V
V_{OH}		V_{CC} = 4.75 V, I_{OH} = −3.2 mA	2.4	3.3		V
V_{OL}		V_{CC} = 4.75 V, I_{OL} = 24 mA		0.35	0.5	V
I_{OZH}	Outputs	V_{CC} = 5.25 V, V_O = 2.7 V			20	µA
	I/O ports				100	
I_{OZL}	Outputs	V_{CC} = 5.25 V, V_O = 0.4 V			−20	µA
	I/O ports				−250	
I_I		V_{CC} = 5.25 V, V_I = 5.5 V			0.1	mA
I_{IH}		V_{CC} = 5.25 V, V_I = 2.7 V			20	µA
I_{IL}		V_{CC} = 5.25 V, V_I = 0.4 V			−0.2	mA
I_O‡		V_{CC} = 5.25 V, V_O = 2.25 V	−30		−125	mA
I_{CC}		V_{CC} = 5.25 V, V_I = 0, Outputs open		140	180	mA

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	TYP†	MAX	UNIT
f_{max}			R1 = 500 Ω, R2 = 500 Ω, See Figure 3	50			MHz
t_{pd}	I, I/O	O, I/O			10	15	ns
t_{pd}	CLK↑	Q			8	12	ns
t_{en}	OE↓	Q			8	12	ns
t_{dis}	OE↑	Q			7	10	ns
t_{en}	I, I/O	O, I/O			10	15	ns
t_{dis}	I, I/O	O, I/O			10	15	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The output conditions hace been chosen to produce a current that closely approximates one half of the short-circuit output current, I_{OS}.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (see Note 1)	5.5 V
Voltage applied to disabled output (see Note 1)	5.5 V
Operating free-air temperature range	−55°C to 125°C
Storage temperature range	−65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−2	mA
I_{OL}	Low-level output current				12	mA
f_{clock}	Clock frequency		0		41.6	MHz
t_w	Pulse duration, clock (see Note 2)	High	10			ns
		Low	11			
t_{su}	Setup time, input or feedback before clock↑		20			ns
t_h	Hold time, input or feedback after clock↑		0			ns
T_A	Operating free-air temperature		−55	25	125	°C

NOTE 2: The total clock period of clock high and clock low must not exceed clock frequency, f_{clock}. The minimum pulse durations specified are only for clock high or low, but not for both simultaneously..

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA				−1.5	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −2 mA		2.4	3.2		V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA			0.25	0.4	V
I_{OZH}	Outputs	V_{CC} = 5.5 V,	V_O = 2.7 V				20	μA
	I/O ports						100	
I_{OZL}	Outputs	V_{CC} = 5.5 V,	V_O = 0.4 V				−20	μA
	I/O ports						−250	
I_I	Pin 1, 11	V_{CC} = 5.5 V,	V_I = 5.5 V				0.2	mA
	All others						0.1	
I_{IH}	Pin 1, 11	V_{CC} = 5.5 V,	V_I = 2.7 V				50	μA
	I/O ports						100	
	All others						20	
I_{IL}	I/O ports	V_{CC} = 5.5 V,	V_I = 0.4 V				−0.25	mA
	All others						−0.2	
I_{OS}‡		V_{CC} = 5.5 V,	V_O = 0.5 V		−30		−250	mA
I_{CC}		V_{CC} = 5.5 V,	V_I = 0,	Outputs open		140	190	mA

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	TYP†	MAX	UNIT
f_{max}			R1 = 390 Ω, R2 = 750 Ω, See Figure 4	41.6			MHz
t_{pd}	I, I/O	O, I/O			10	20	ns
t_{pd}	CLK↑	Q			8	15	ns
t_{en}	OE↓	Q			8	15	ns
t_{dis}	OE↑	Q			7	15	ns
t_{en}	I, I/O	O, I/O			10	20	ns
t_{dis}	I, I/O	O, I/O			10	20	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second. Set V_O at 0.5 V to avoid test equipment degradation.

programming information

Texas Instruments programmable logic devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments programmable logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

preload procedure for registered outputs (see Figure 1 and Note 3)

The output registers can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below.

Step 1. With V_{CC} at 5 volts and Pin 1 at V_{IL}, raise Pin 11 to V_{IHH}.
Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.
Step 3. Pulse Pin 1, clocking in preload data.
Step 4. Remove output voltage, then lower Pin 11 to V_{IL}. Preload can be verified by observing the voltage level at the output pin.

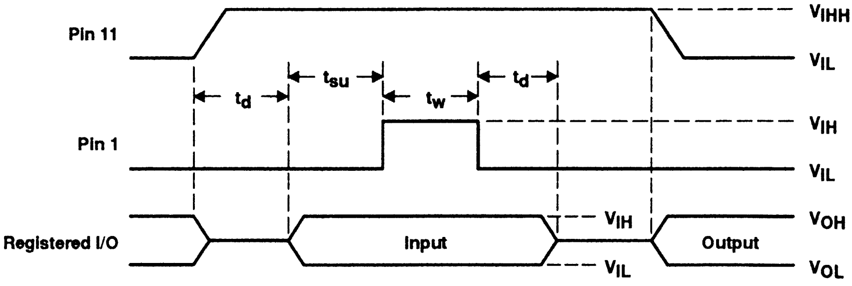
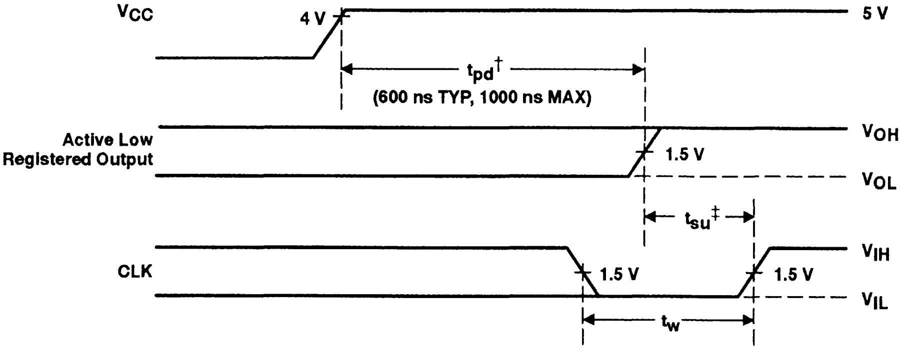


Figure 1. Preload Waveforms

NOTE 3: $t_d = t_{su} = t_h$ = 100 ns to 1000 ns V_{IHH} = 10.25 V to 10.75 v

power-up reset (see Figure 2)

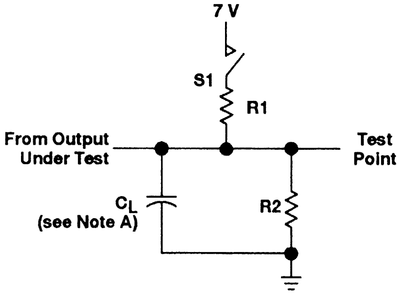
Following power up, all registers are reset to zero. This feature provides extra flexibility to the system designer and is especially valuable in simplifying state-machine initialization. To ensure a valid power-up reset, it is important that the rise of V_{CC} be monotonic. Following power-up reset, a low-to-high clock transition must not occur until all applicable input and feedback setup times are met.



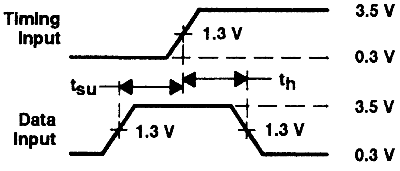
† This is the power-up reset time and applies to registered outputs only. The values shown are from characterization data.
‡ This is the setup time for input or feedback.

Figure 2. Power-Up Reset Waveforms

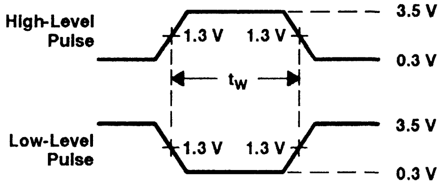
PARAMETER MEASUREMENT INFORMATION



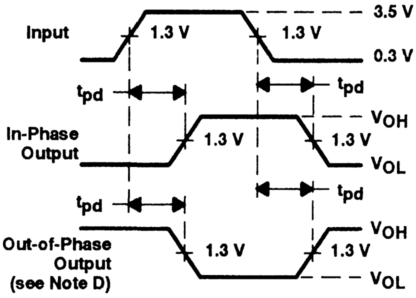
LOAD CIRCUIT FOR
3-STATE OUTPUTS



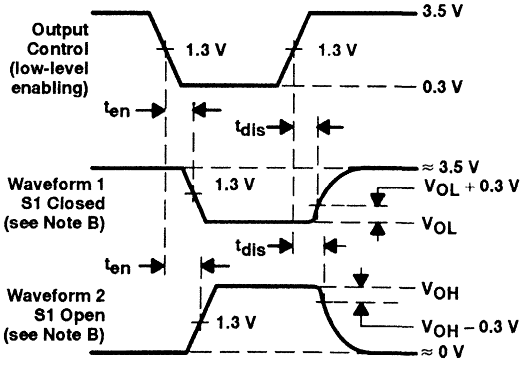
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

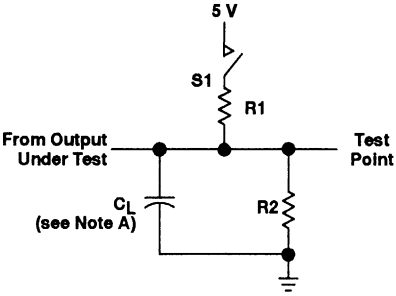


VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

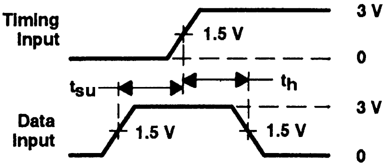
NOTES:
- A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f \leq 2$ ns, duty cycle = 50%
- D. When measuring propagation delay times of 3-state outputs from low to high, switch S1 is closed. When measuring propagation delay times of 3-state outputs from high to low, switch S1 is open.
- E. Equivalent loads may be used for testing.

Figure 3. Load Circuit and Voltage Waveforms

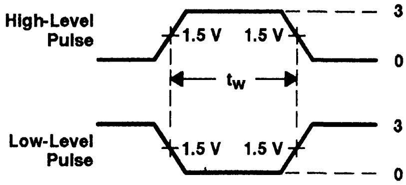
PARAMETER MEASUREMENT INFORMATION



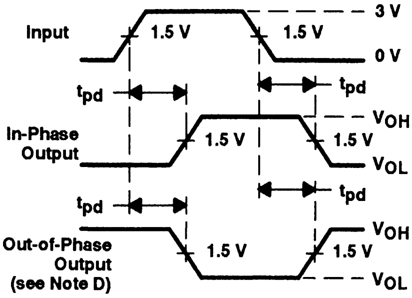
LOAD CIRCUIT FOR 3-STATE OUTPUTS



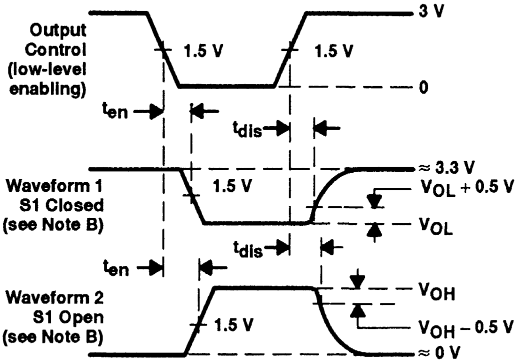
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATIONS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses have the following characteristics: PRR ≤ 10 MHz, t_r and $t_f \le 2$ ns, duty cycle = 50%

D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.

E. Equivalent loads may be used for testing.

Figure 4. Load Circuit and Voltage Waveforms

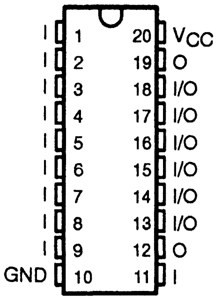
TIBPAL16L8-25C, TIBPAL16R4-25C, TIBPAL16R6-25C, TIBPAL16R8-25C
TIBPAL16L8-30M, TIBPAL16R4-30M, TIBPAL16R6-30M, TIBPAL16R8-30M
LOW-POWER HIGH-PERFORMANCE *IMPACT*™ *PAL*® CIRCUITS

SRPS020 – D3337, FEBRUARY 1984 – REVISED MARCH 1992

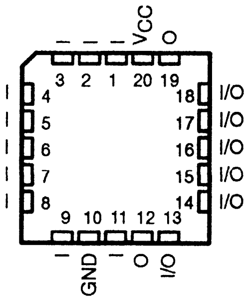
- **High-Performance Operation:**
  Propagation Delay
  C Suffix . . . 25 ns Max
  M Suffix . . . 30 ns Max
- **Functionally Equivalent, but Faster than PAL16L8A, PAL16R4A, PAL16R6A, and PAL16R8A**
- **Power-Up Clear on Registered Devices (All Register Outputs are Set High, but Voltage Levels at the Output Pins Go Low)**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

DEVICE	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
PAL16L8	10	2	0	6
PAL16R4	8	0	4 (3-state buffers)	4
PAL16R6	8	0	6 (3-state buffers)	2
PAL16R8	8	0	8 (3-state buffers)	0

TIBPAL16L8'
C SUFFIX . . . J OR N PACKAGE
M SUFFIX . . . J OR W PACKAGE
(TOP VIEW)



TIBPAL16L8'
C SUFFIX . . . FN PACKAGE
M SUFFIX . . . FK PACKAGE
(TOP VIEW)



description

These programmable array logic devices feature high speed and functional equivalency when compared with currently available devices. These IMPACT™ circuits combine the latest Advanced Low-Power Schottky technology with proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional TTL logic. Their easy programmability allows for quick design of custom functions and typically results in a more compact circuit board. In addition, chip carriers are available for futher reduction in board space.

The TIBPAL16' C series is characterized from 0°C to 75°C. The TIBPAL16' M series is characterized for operation over the full military temperature range of –55°C to 125°C.

These devices are covered by U.S. Patent 4,410,987.
IMPACT is a trademark of Texas Instruments Incorporated.
PAL is a registered trademark of Advanced Micro Devices Inc.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

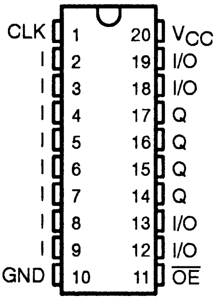
Copyright © 1992, Texas Instruments Incorporated

TIBPAL16R4-25C, TIBPAL16R6-25C, TIBPAL16R8-25C
TIBPAL16R4-30M, TIBPAL16R6-30M, TIBPAL16R8-30M
LOW-POWER HIGH-PERFORMANCE *IMPACT*™ *PAL*® CIRCUITS

SRPS020 – D3337, FEBRUARY 1984 – REVISED MARCH 1992

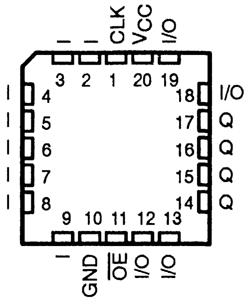
TIBPAL16R4'
C SUFFIX . . . J OR N PACKAGE
M SUFFIX . . . J OR W PACKAGE

(TOP VIEW)



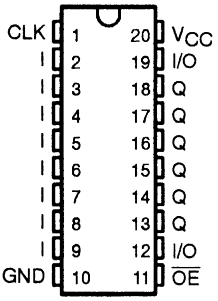
TIBPAL16R4'
C SUFFIX . . . FN PACKAGE
M SUFFIX . . . FK PACKAGE

(TOP VIEW)



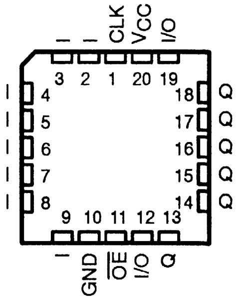
TIBPAL16R6'
C SUFFIX . . . J OR N PACKAGE
M SUFFIX . . . J OR W PACKAGE

(TOP VIEW)



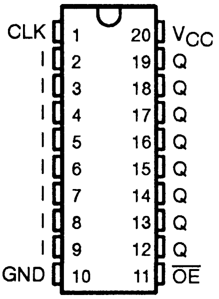
TIBPAL16R6'
C SUFFIX . . . FN PACKAGE
M SUFFIX . . . FK PACKAGE

(TOP VIEW)



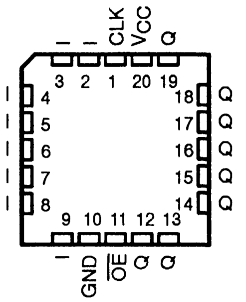
TIBPAL16R8'
C SUFFIX . . . J OR N PACKAGE
M SUFFIX . . . J OR W PACKAGE

(TOP VIEW)



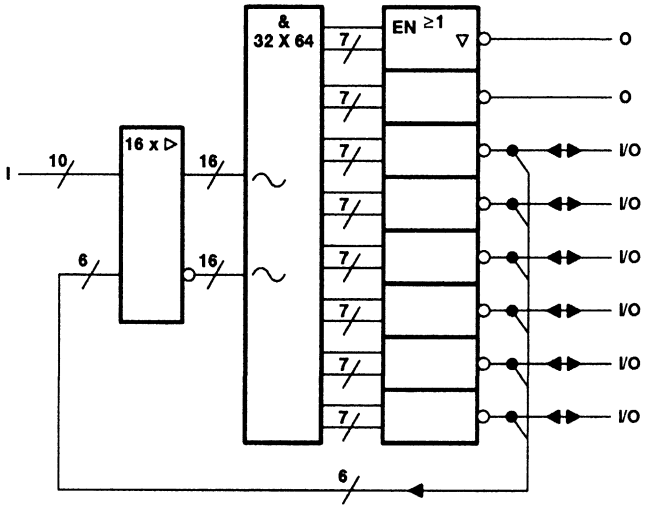
TIBPAL16R8'
C SUFFIX . . . FN PACKAGE
M SUFFIX . . . FK PACKAGE

(TOP VIEW)

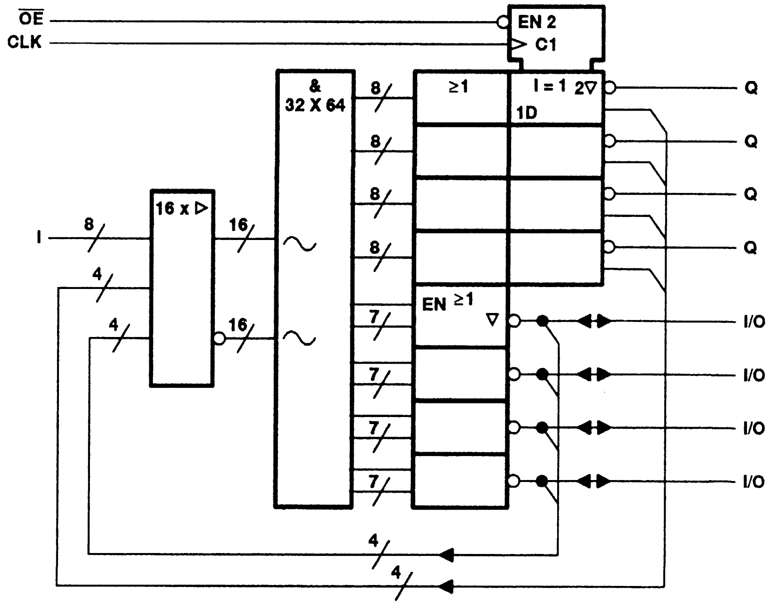


functional block diagrams (positive logic)

TIBPAL16L8'



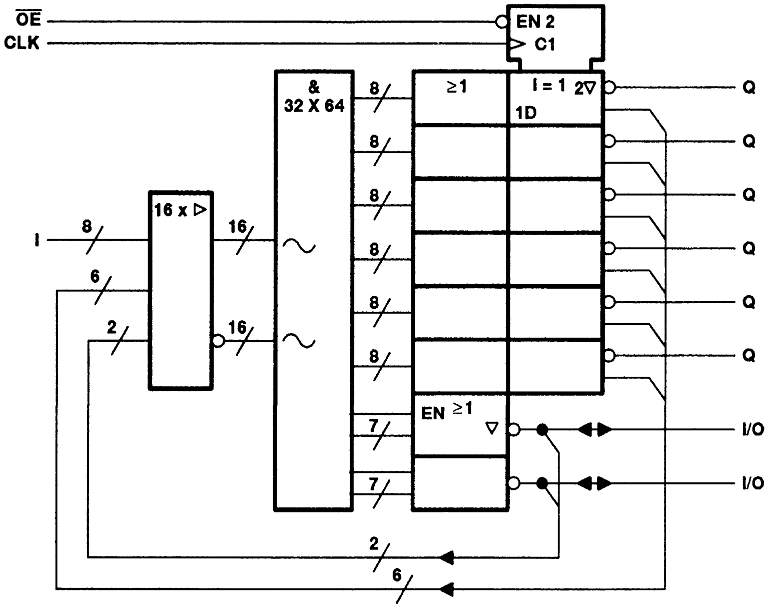
TIBPAL16R4'



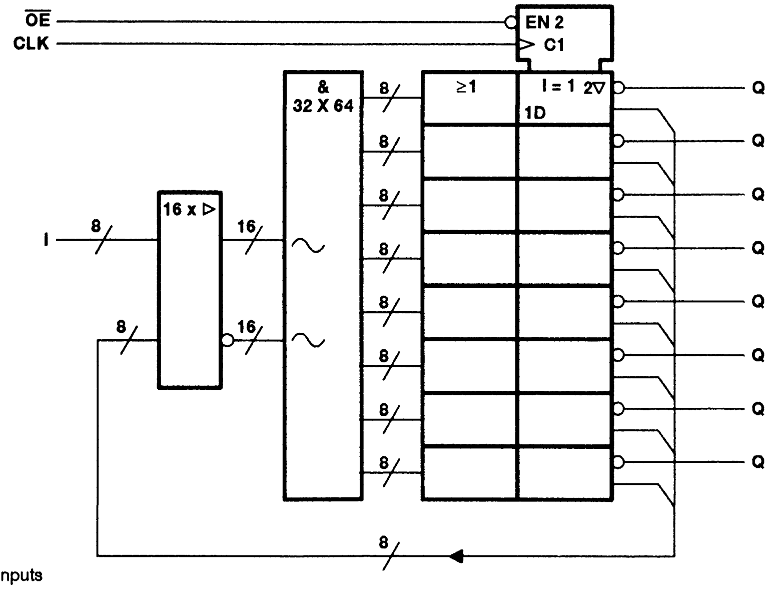
∿ denotes fused inputs

functional block diagrams (positive logic)

TIBPAL16R6'

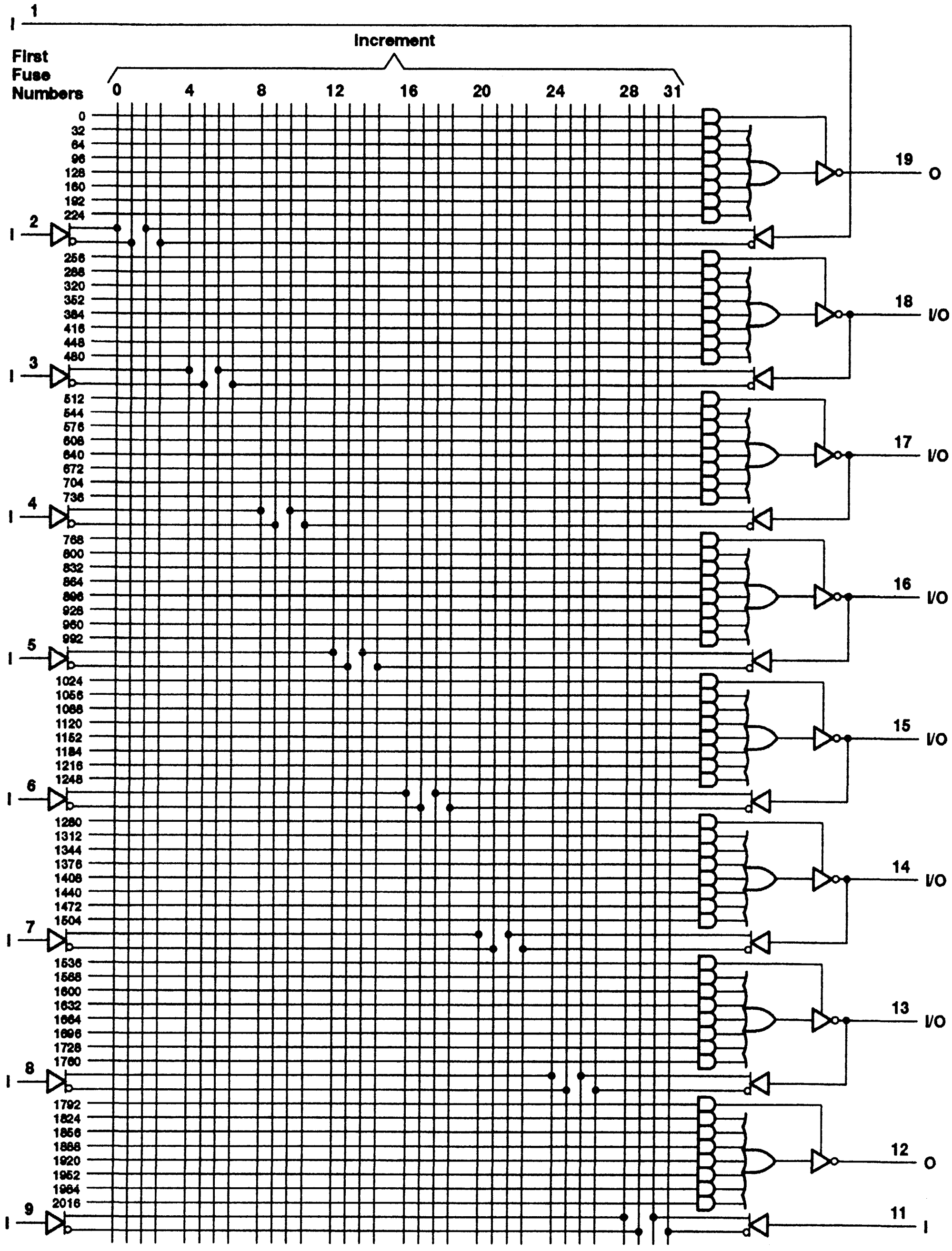


TIBPAL16R8'



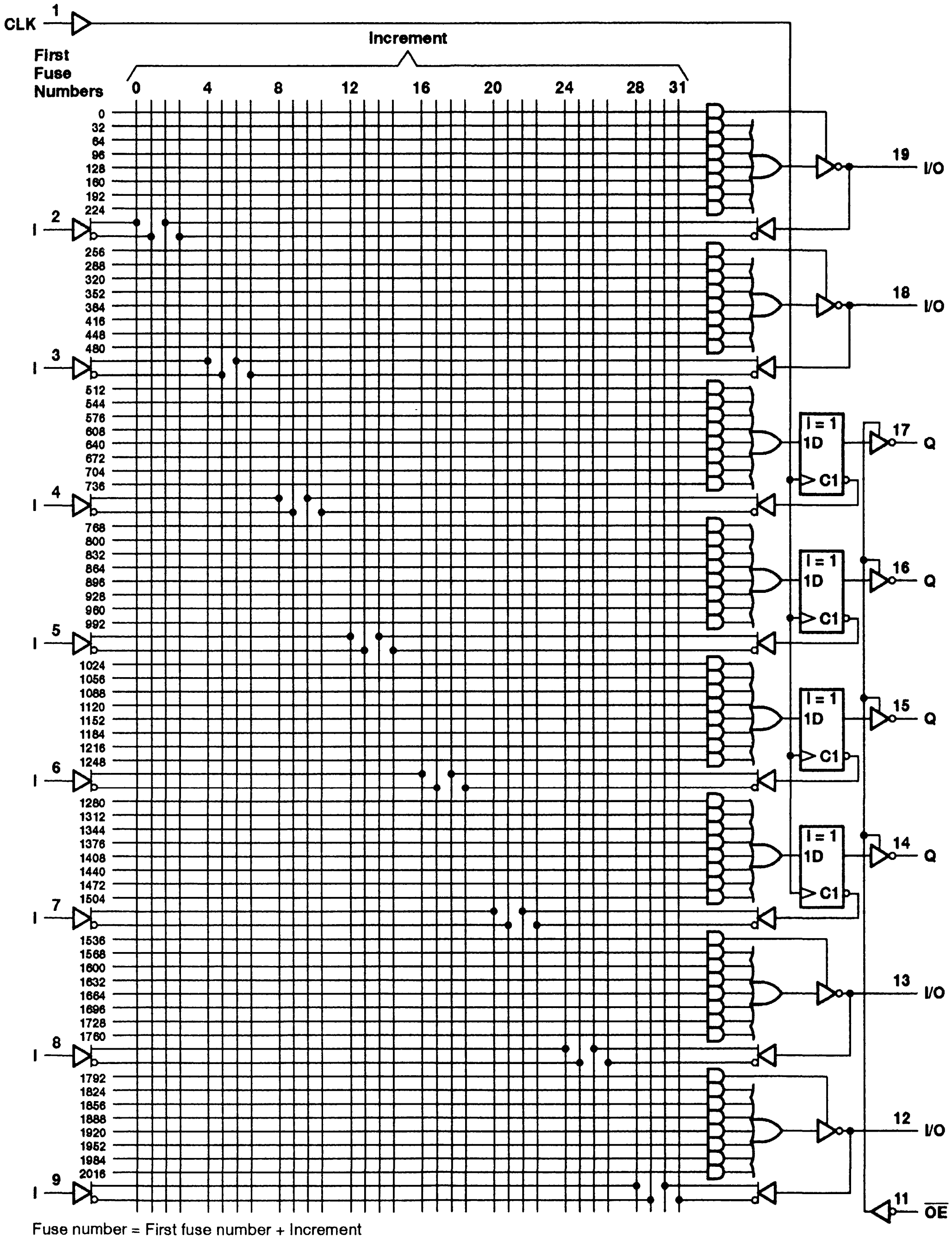
∿ denotes fused inputs

logic diagram (positive logic)



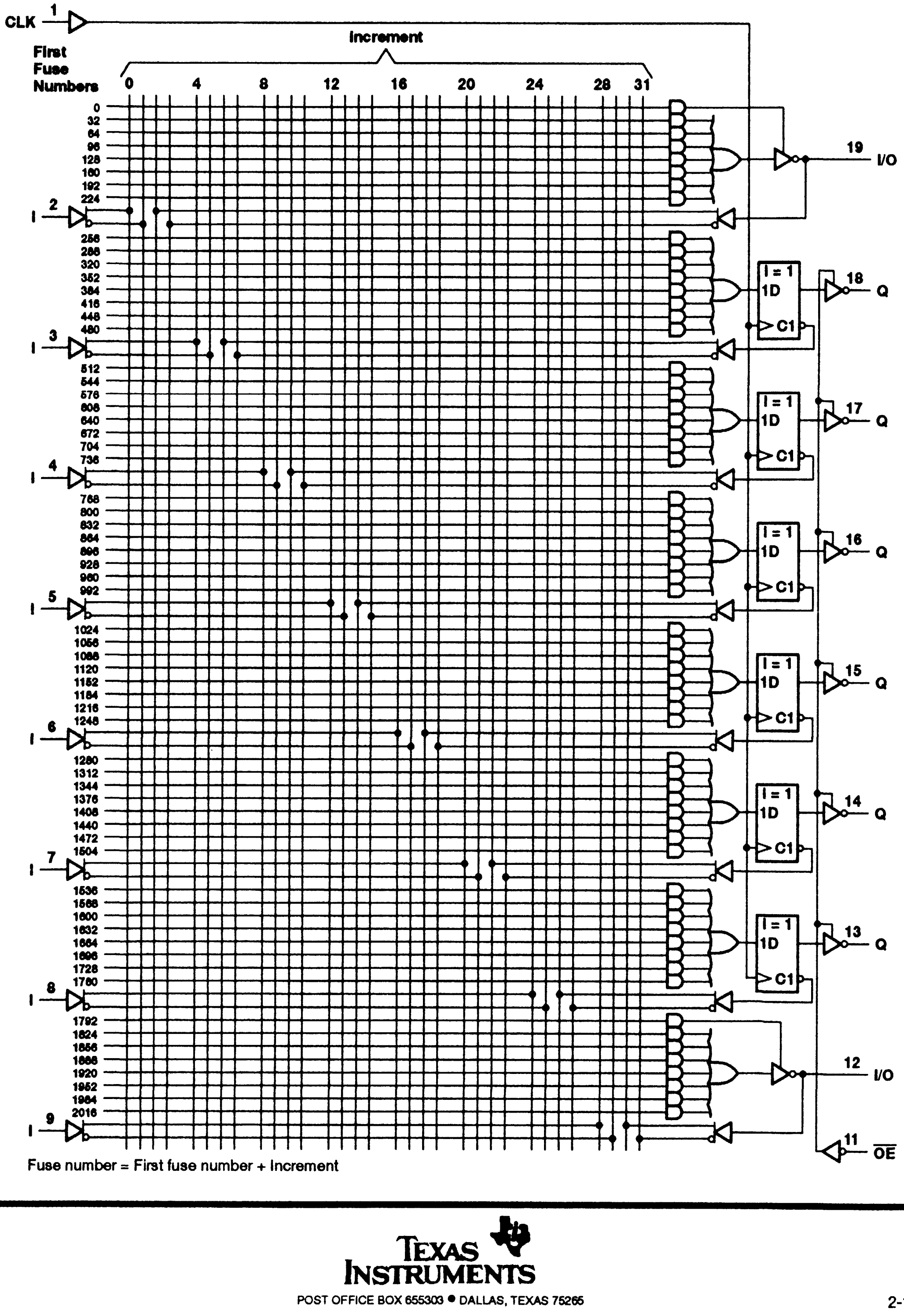
Fuse number = First fuse number + Increment

logic diagram (positive logic)



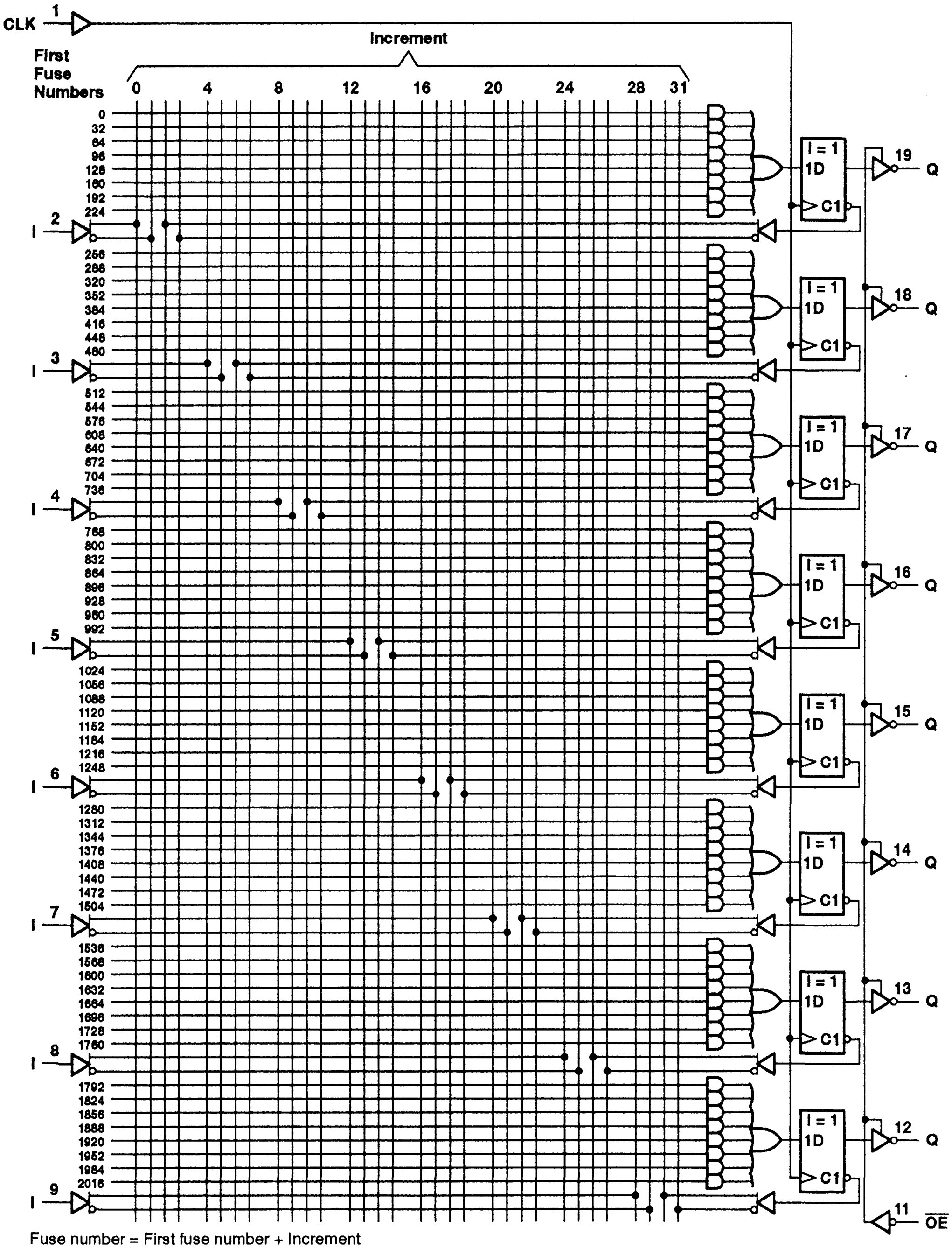
Fuse number = First fuse number + Increment

logic diagram (positive logic)



Fuse number = First fuse number + Increment

logic diagram (positive logic)



Fuse number = First fuse number + Increment

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) .... 7 V
Input voltage (see Note 1) .... 5.5 V
Voltage applied to disabled output (see Note 1) .... 5.5 V
Operating free-air temperature range .... 0°C to 75°C
Storage temperature range .... −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−3.2	mA
I_{OL}	Low-level output current				24	mA
f_{clock}	Clock frequency		0		30	MHz
t_w	Pulse duration, clock (see Note 2)	High	10			ns
		Low	15			
t_{su}	Setup time, input or feedback before clock↑		20			ns
t_h	Hold time, input or feedback after clock↑		0			ns
T_A	Operating free-air temperature		0	25	75	°C

NOTE 2: The total clock period of clock high and clock low must not exceed clock frequency, f_{clock}. The minimum pulse durations specified are only for clock high or low, but not for both simultaneously.

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.75 V,	I_I = −18 mA				−1.5	V
V_{OH}		V_{CC} = 4.75 V,	I_{OH} = −3.2 mA		2.4	3.3		V
V_{OL}		V_{CC} = 4.75 V,	I_{OL} = 24 mA			0.35	0.5	V
I_{OZH}	Outputs	V_{CC} = 5.25 V,	V_O = 2.7 V				20	µA
	I/O ports						100	
I_{OZL}	Outputs	V_{CC} = 5.25 V,	V_O = 0.4 V				−20	µA
	I/O ports						−250	
I_I		V_{CC} = 5.25 V,	V_I = 5.5 V				0.1	mA
I_{IH}		V_{CC} = 5.25 V,	V_I = 2.7 V				20	µA
I_{IL}		V_{CC} = 5.25 V,	V_I = 0.4 V				−0.25	mA
I_O‡		V_{CC} = 5.25 V,	V_O = 2.25 V		−30		−125	mA
I_{CC}		V_{CC} = 5.25 V,	V_I = 0,	Outputs open		75	100	mA

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	TYP†	MAX	UNIT
f_{max}			R1 = 500 Ω, R2 = 500 Ω, See Figure 3	30			MHz
t_{pd}	I, I/O	O, I/O			15	25	ns
t_{pd}	CLK↑	Q			10	15	ns
t_{en}	OE↓	Q			15	20	ns
t_{dis}	OE↑	Q			10	20	ns
t_{en}	I, I/O	O, I/O			14	25	ns
t_{dis}	I, I/O	O, I/O			13	25	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ The output conditions hace been chosen to produce a current that closely approximates one half of the short-circuit output current, I_{OS}.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (see Note 1)	5.5 V
Voltage applied to disabled output (see Note 1)	5.5 V
Operating free-air temperature range	−55°C to 125°C
Storage temperature range	−65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−2	mA
I_{OL}	Low-level output current				12	mA
f_{clock}	Clock frequency		0		25	MHz
t_w	Pulse duration, clock (see Note 2)	High	15			ns
		Low	20			
t_{su}	Setup time, input or feedback before clock↑		25			ns
t_h	Hold time, input or feedback after clock↑		0			ns
T_A	Operating free-air temperature		−55	25	125	°C

NOTE 2: The total clock period of clock high and clock low must not exceed clock frequency, f_{clock}. The minimum pulse durations specified are only for clock high or low, but not for both simultaneously..

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA				–1.5	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = –2 mA		2.4	3.2		V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA			0.25	0.4	V
I_{OZH}	Outputs	V_{CC} = 5.5 V,	V_O = 2.7 V				20	µA
	I/O ports						100	
I_{OZL}	Outputs	V_{CC} = 5.5 V,	V_O = 0.4 V				–20	µA
	I/O ports						–250	
I_I	Pin 1, 11	V_{CC} = 5.5 V,	V_I = 5.5 V				0.2	mA
	All others						0.1	
I_{IH}	Pin 1, 11	V_{CC} = 5.5 V,	V_I = 2.7 V				50	µA
	I/O ports						100	
	All others						20	
I_{IL}	I/O ports	V_{CC} = 5.5 V,	V_I = 0.4 V				–0.25	mA
	All others						–0.2	
I_{OS}‡		V_{CC} = 5.5 V,	V_O = 0.5 V		–30		–250	mA
I_{CC}		V_{CC} = 5.5 V,	V_I = 0,	Outputs open		75	105	mA

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	TYP†	MAX	UNIT
f_{max}			R1 = 390 Ω, R2 = 750 Ω, See Figure 4	25			MHz
t_{pd}	I, I/O	O, I/O			15	30	ns
t_{pd}	CLK↑	Q			10	20	ns
t_{en}	OE↓	Q			15	25	ns
t_{dis}	OE↑	Q			10	25	ns
t_{en}	I, I/O	O, I/O			14	30	ns
t_{dis}	I, I/O	O, I/O			13	30	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ Not more than one output should be shorted at a time and the duration of the short circuit should not exceed one second. Set V_O at 0.5 V to avoid test equipment degradation.

programming information

Texas Instruments programmable logic devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments programmable logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

preload procedure for registered outputs (see Figure 1 and Note 3)

The output registers can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below.

Step 1. With V_{CC} at 5 volts and Pin 1 at V_{IL}, raise Pin 11 to V_{IHH}.
Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.
Step 3. Pulse Pin 1, clocking in preload data.
Step 4. Remove output voltage, then lower Pin 11 to V_{IL}. Preload can be verified by observing the voltage level at the output pin.

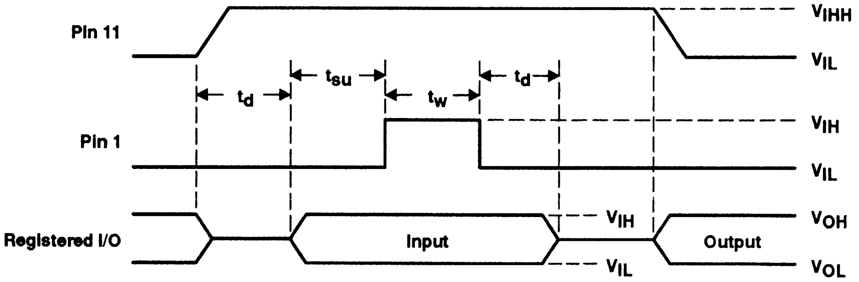
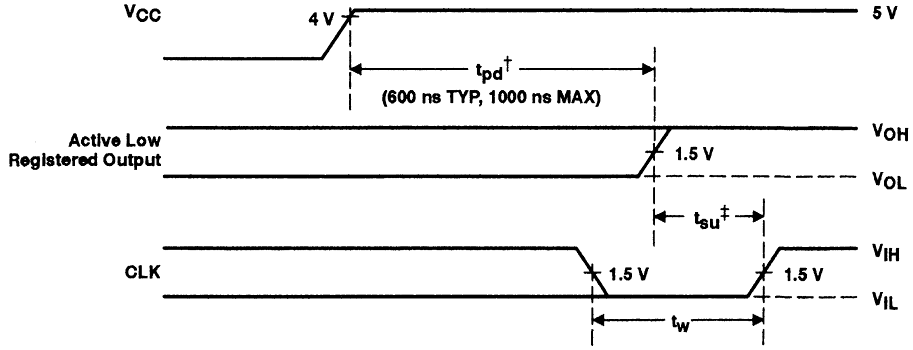


Figure 1. Preload Waveforms

NOTE 3: $t_d = t_{su} = t_h$ = 100 ns to 1000 ns V_{IHH} = 10.25 V to 10.75 v

power-up reset (see Figure 2)

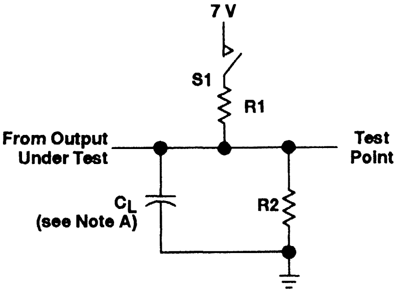
Following power up, all registers are reset to zero. This feature provides extra flexibility to the system designer and is especially valuable in simplifying state-machine initialization. To ensure a valid power-up reset, it is important that the rise of V_{CC} be monotonic. Following power-up reset, a low-to-high clock transition must not occur until all applicable input and feedback setup times are met.



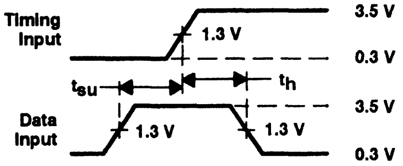
† This is the power-up reset time and applies to registered outputs only. The values shown are from characterization data.
‡ This is the setup time for input or feedback.

Figure 2. Power-Up Reset Waveforms

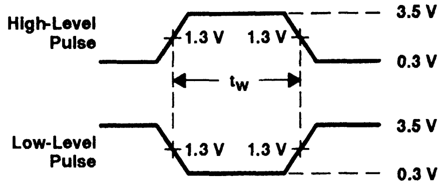
PARAMETER MEASUREMENT INFORMATION



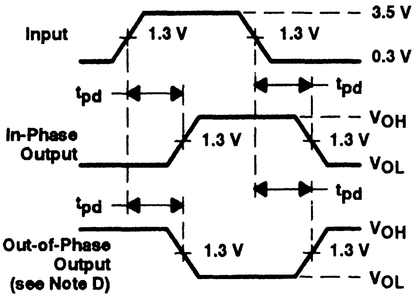
LOAD CIRCUIT FOR 3-STATE OUTPUTS



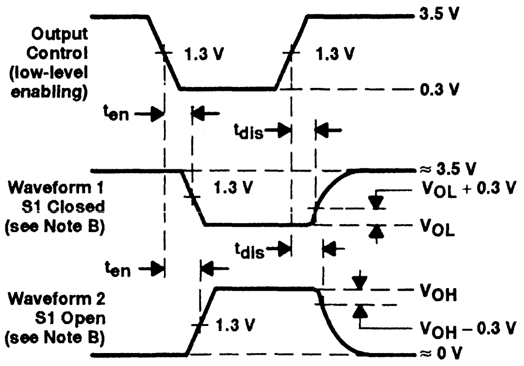
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATIONS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

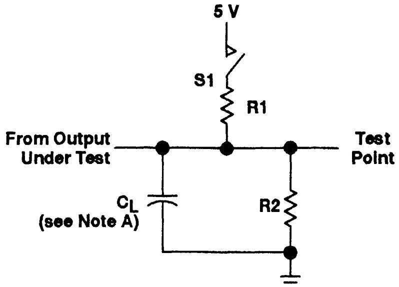
C. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f \leq 2$ ns, duty cycle = 50%

D. When measuring propagation delay times of 3-state outputs from low to high, switch S1 is closed.
When measuring propagation delay times of 3-state outputs from high to low, switch S1 is open.

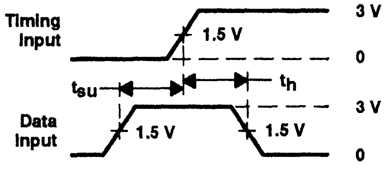
E. Equivalent loads may be used for testing.

Figure 3. Load Circuit and Voltage Waveforms

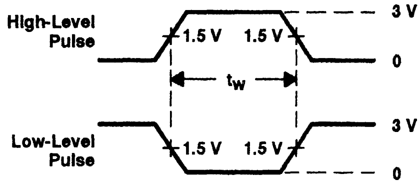
PARAMETER MEASUREMENT INFORMATION



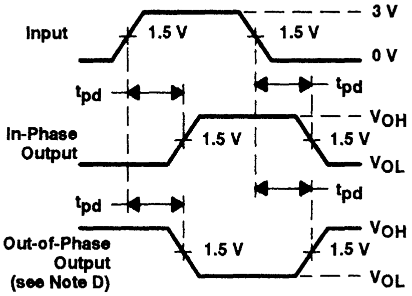
LOAD CIRCUIT FOR
3-STATE OUTPUTS



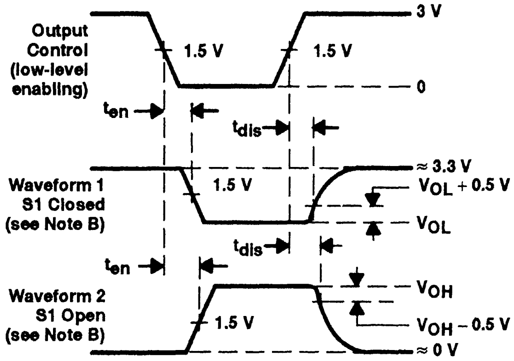
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 10 MHz, t_r and t_f ≤ 2 ns, duty cycle = 50%
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.
E. Equivalent loads may be used for testing.

Figure 4. Load Circuit and Voltage Waveforms

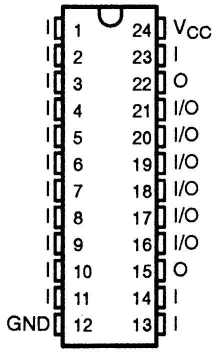
TIBPAL20L8-5C, TIBPAL20R4-5C, TIBPAL20R6-5C, TIBPAL20R8-5C
TIBPAL20L8-7M, TIBPAL20R4-7M, TIBPAL20R6-7M, TIBPAL20R8-7M
HIGH-PERFORMANCE *IMPACT-X*™ *PAL*® CIRCUITS

SRPS010F – D3353, OCTOBER 1989 – REVISED SEPTEMBER 1992

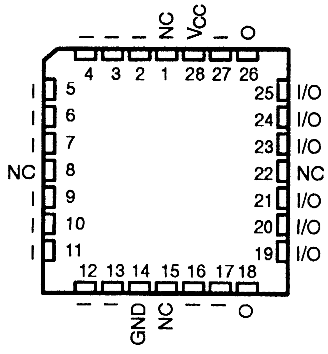
- **High-Performance Operation:**
  f_{max} (no feedback)
    TIBPAL20R' -5C Series . . . 125 MHz Min
    TIBPAL20R' -7M Series . . . 100 MHz Min
  f_{max} (internal feedback)
    TIBPAL20R' -5C Series . . . 125 MHz Min
    TIBPAL20R' -7M Series . . . 100 MHz Min
  f_{max} (external feedback)
    TIBPAL20R' -5C Series . . . 117 MHz Min
    TIBPAL20R' -7M Series . . . 74 MHz Min
  Propagation Delay
    TIBPAL20L8-5C Series . . . 5 ns Max
    TIBPAL20L8-7M Series . . . 7 ns Max
    TIBPAL20R' -5C Series
      (CLK-to-Q) . . . 4 ns Max
    TIBPAL20R' -7M Series
      (CLK-to-Q) . . . 6.5 ns Max
- **Functionally Equivalent, but Faster Than, Existing 24-Pin PLDs**
- **Preload Capability on Output Registers Simplifies Testing**
- **Power-Up Clear on Registered Devices (All Register Outputs are Set Low, but Voltage Levels at the Output Pins Go High)**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Security Fuse Prevents Duplication**

DEVICE	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
PAL20L8	14	2	0	6
PAL20R4	12	0	4 (3-state buffers)	4
PAL20R6	12	0	6 (3-state buffers)	2
PAL20R8	12	0	8 (3-state buffers)	0

TIBPAL20L8'
C SUFFIX . . . JT OR NT PACKAGE
M SUFFIX . . . JT PACKAGE
(TOP VIEW)



TIBPAL20L8'
C SUFFIX . . . FN PACKAGE
M SUFFIX . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection
Pin assignments in operating mode

description

These programmable array logic devices feature high speed and functional equivalency when compared with currently available devices. These IMPACT-X™ circuits combine the latest Advanced Low-Power Schottky technology with proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional TTL logic. Their easy programmability allows for quick design of custom functions and typically results in a more compact circuit board.

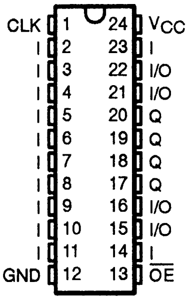
The TIBPAL20' C series is characterized from 0°C to 75°C. The TIBPAL20' M series is characterized for operation over the full military temperature range of –55°C to 125°C.

These devices are covered by U.S. Patent 4,410,987.
IMPACT-X is a trademark of Texas Instruments Incorporated.
PAL is a registered trademark of Advanced Micro Devices Inc.

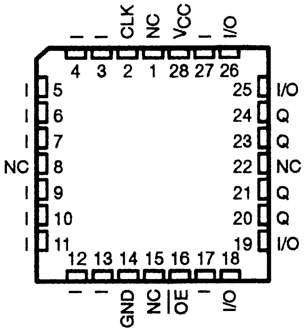
This document contains information on products in more than one phase of development. The status of each device is indicated on the page(s) specifying its electrical characteristics.

Copyright © 1992, Texas Instruments Incorporated

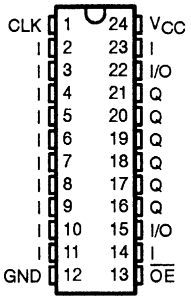
TIBPAL20R4'
C SUFFIX . . . JT OR NT PACKAGE
M SUFFIX . . . JT PACKAGE
(TOP VIEW)



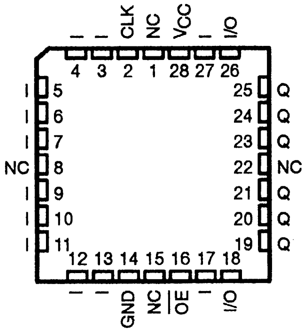
TIBPAL20R4'
C SUFFIX . . . FN PACKAGE
M SUFFIX . . . FK PACKAGE
(TOP VIEW)



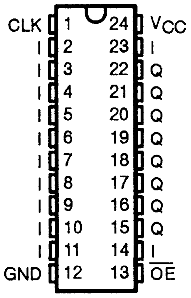
TIBPAL20R6'
C SUFFIX . . . JT OR NT PACKAGE
M SUFFIX . . . JT PACKAGE
(TOP VIEW)



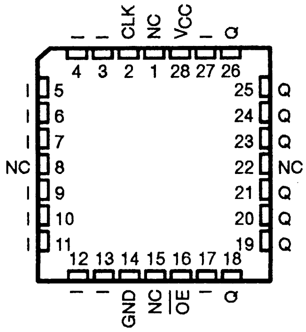
TIBPAL20R6'
C SUFFIX . . . FN PACKAGE
M SUFFIX . . . FK PACKAGE
(TOP VIEW)



TIBPAL20R8'
C SUFFIX . . . JT OR NT PACKAGE
M SUFFIX . . . JT PACKAGE
(TOP VIEW)



TIBPAL20R8'
C SUFFIX . . . FN PACKAGE
M SUFFIX . . . FK PACKAGE
(TOP VIEW)

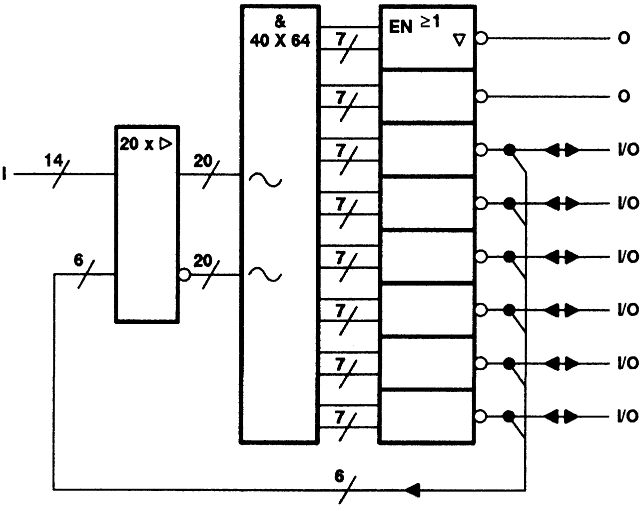


Pin assignments in operating mode

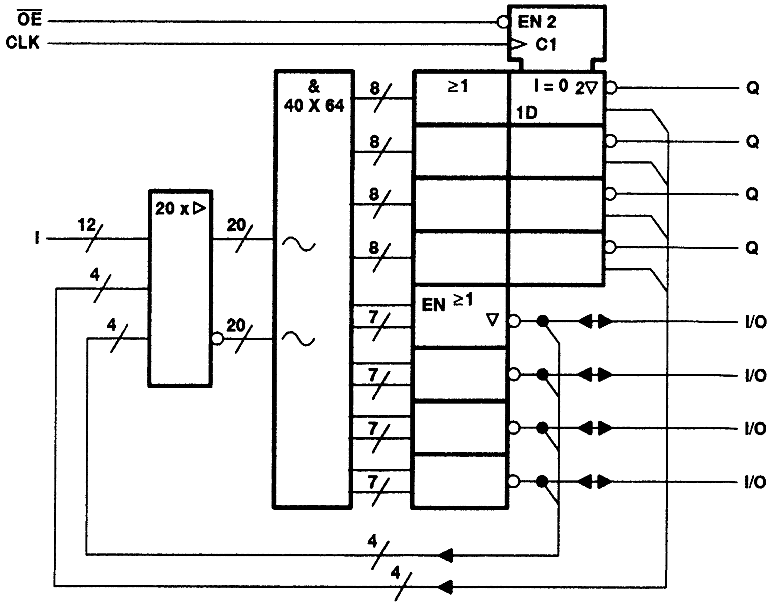
NC – No internal connection

functional block diagrams (positive logic)

TIBPAL20L8'



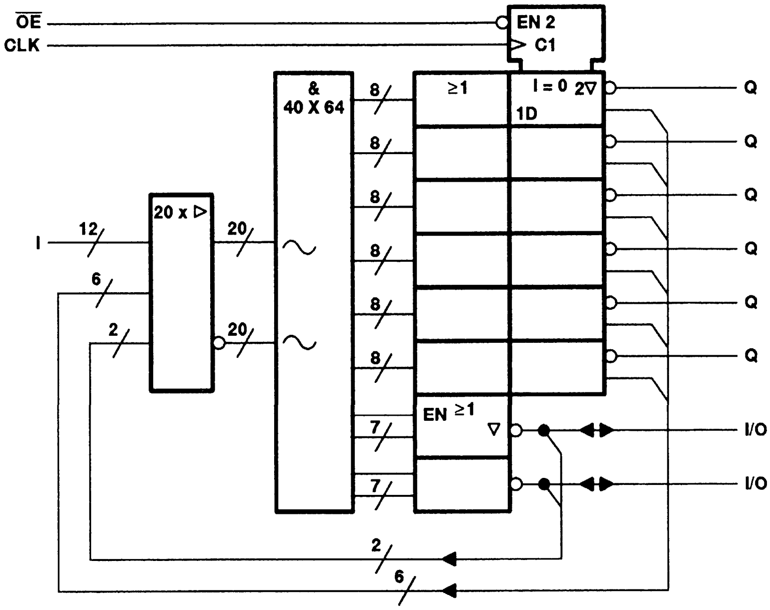
TIBPAL20R4'



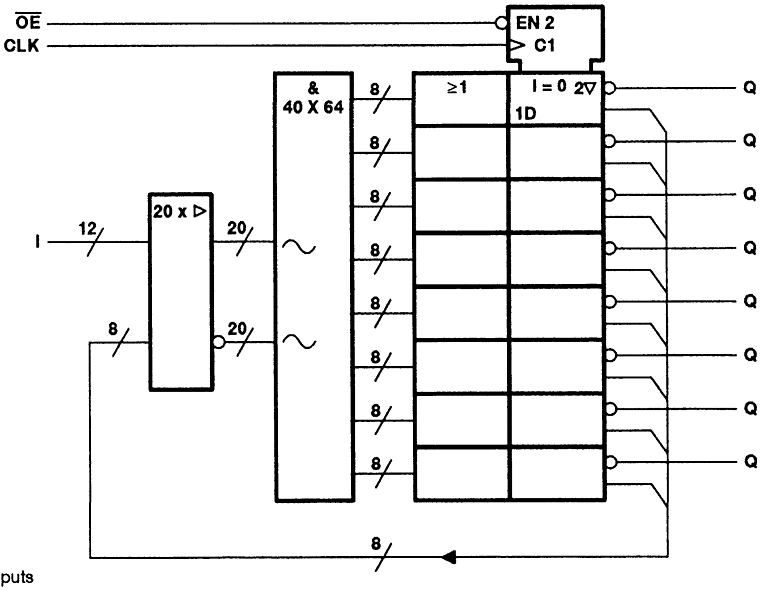
∿ denotes fused inputs

functional block diagrams (positive logic)

TIBPAL20R6'

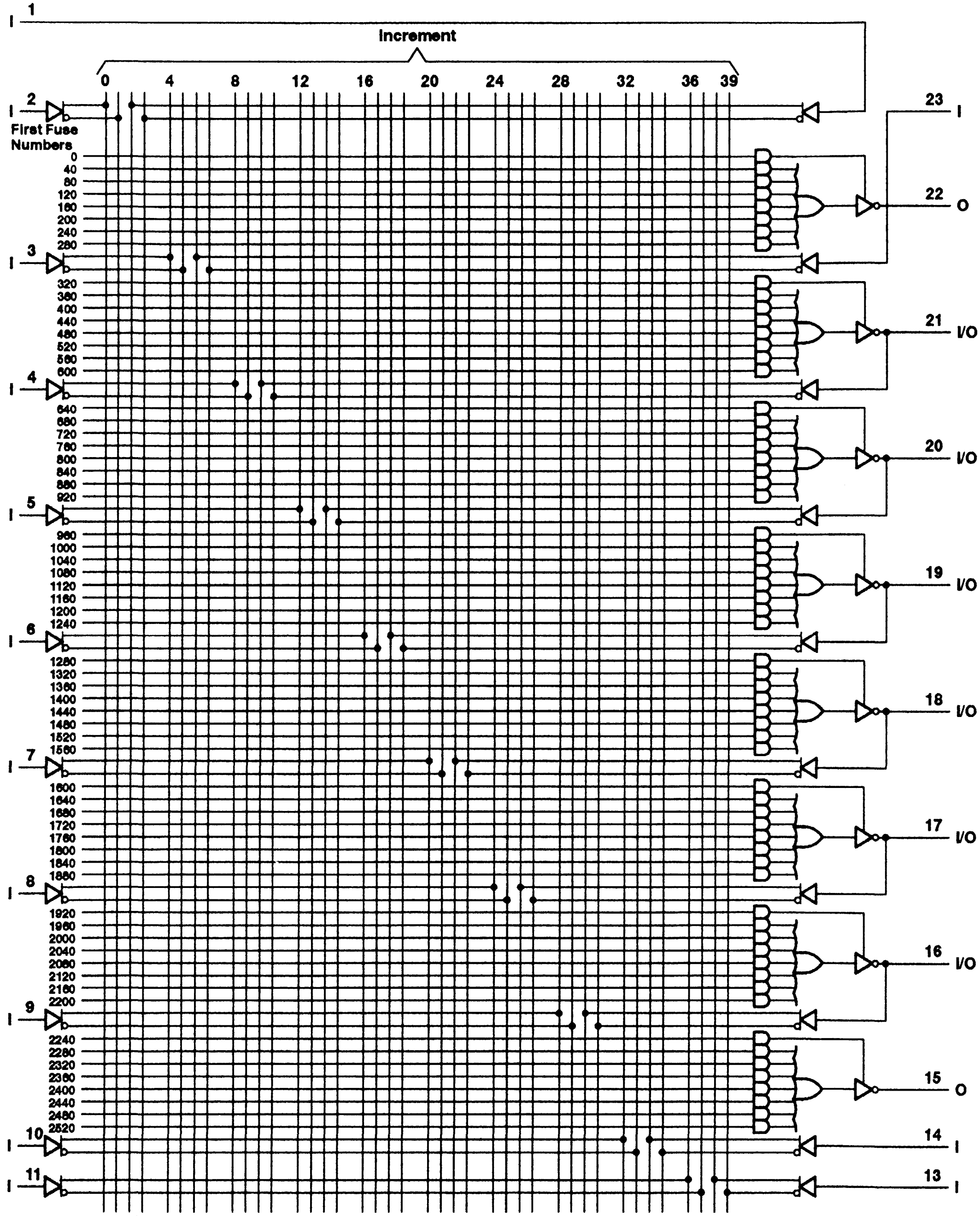


TIBPAL20R8'



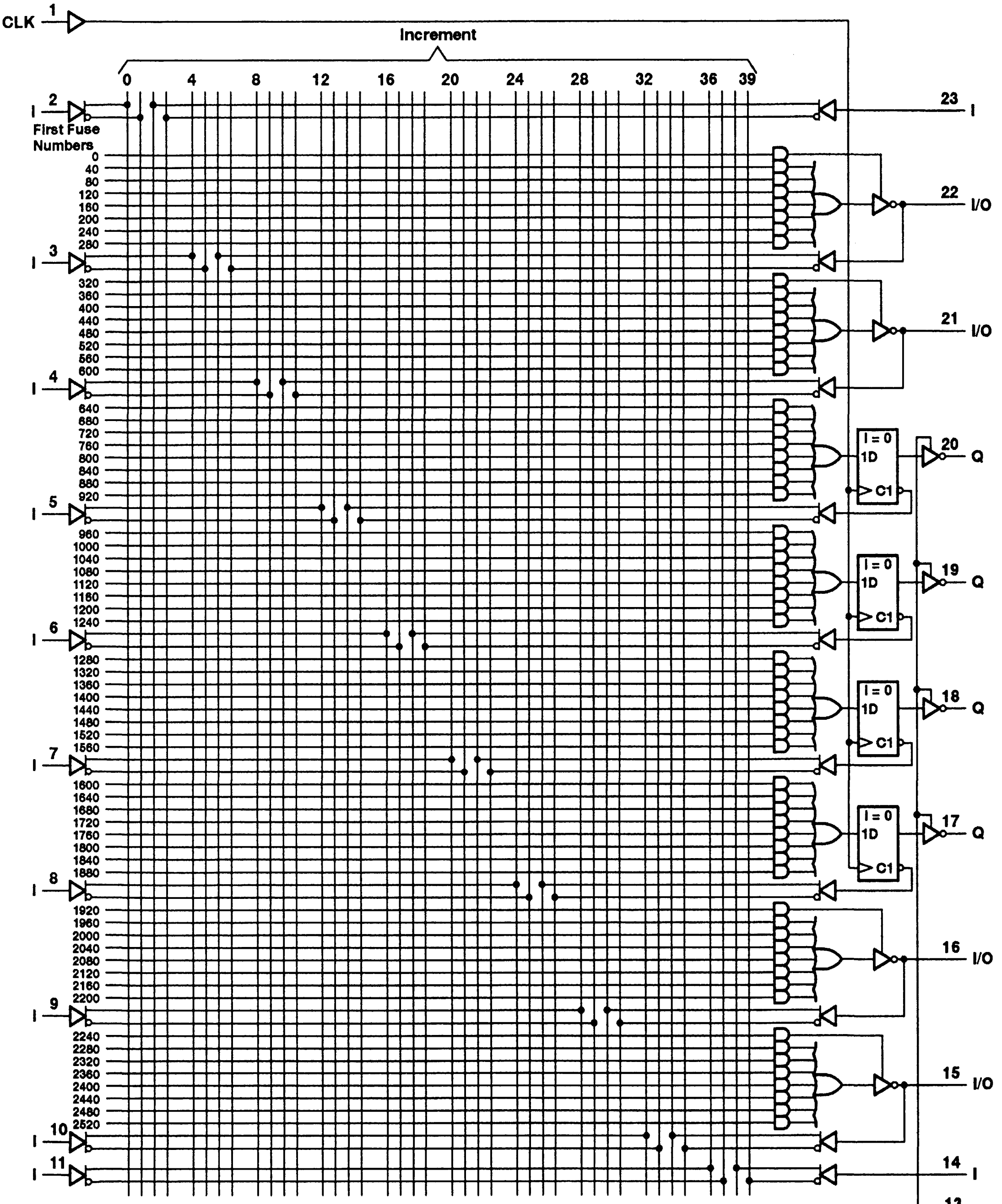
∿ denotes fused inputs

logic diagram (positive logic)



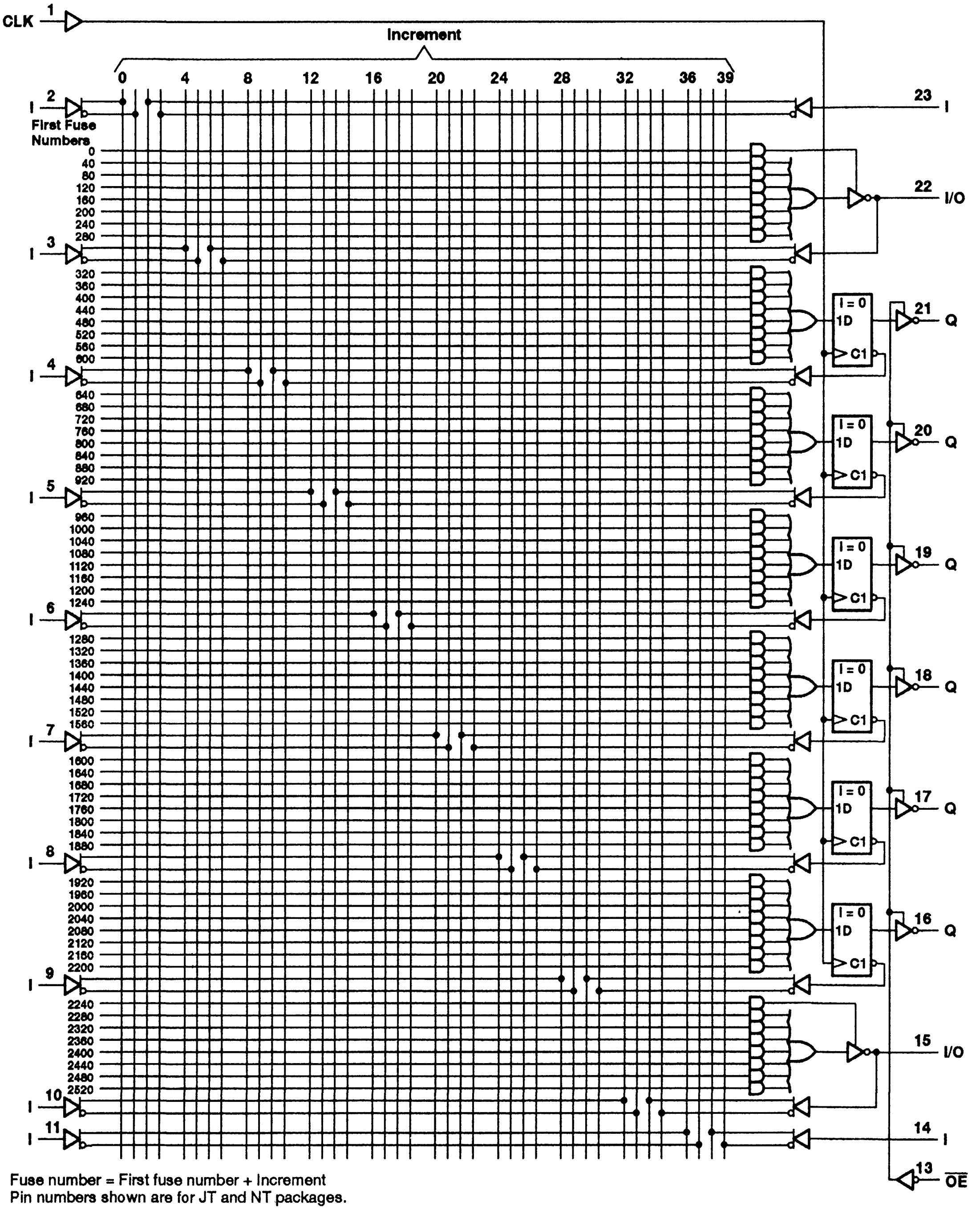
Fuse number = First fuse number + Increment
Pin numbers shown are for JT and NT packages.

logic diagram (positive logic)



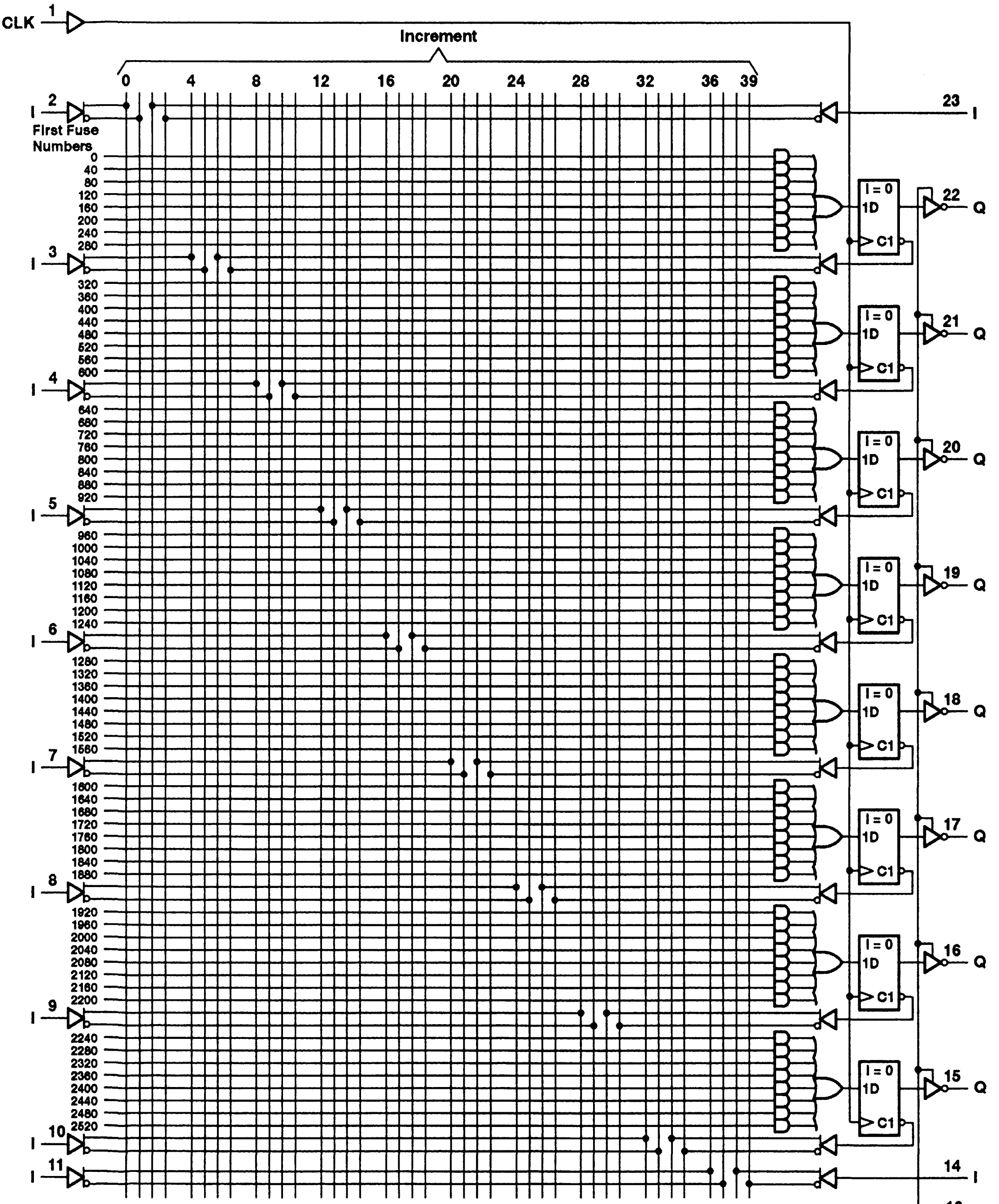
Fuse number = First fuse number + Increment
Pin numbers shown are for JT and NT packages.

logic diagram (positive logic)



Fuse number = First fuse number + Increment
Pin numbers shown are for JT and NT packages.

logic diagram (positive logic)



Fuse number = First fuse number + Increment
Pin numbers shown are for JT and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) .... 7 V
Input voltage (see Note 1) .... 5.5 V
Voltage applied to disabled output (see Note 1) .... 5.5 V
Operating free-air temperature range .... 0°C to 75°C
Storage temperature range .... –65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle or during a preload cycle.

recommended operating conditions

		MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage	4.75	5	5.25	V
V_{IH}	High-level input voltage (see Note 2)	2		5.5	V
V_{IL}	Low-level input voltage (see Note 2)			0.8	V
I_{OH}	High-level output current			–3.2	mA
I_{OL}	Low-level output current			24	mA
T_A	Operating free-air temperature	0	25	75	°C

NOTE 2: These are absolute voltage levels with respect to the ground pin of the device and include all overshoots due to system and/or tester noise. Testing these parameters should not be attempted without suitable equipment.

electrical characteristics over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.75 V,	I_I = –18 mA			–0.8	–1.5	V
V_{OH}	V_{CC} = 4.75 V,	I_{OH} = –3.2 mA		2.4	2.7		V
V_{OL}	V_{CC} = 4.75 V,	I_{OL} = 24 mA			0.3	0.5	V
I_{OZH}‡	V_{CC} = 5.25 V,	V_O = 2.7 V				100	µA
I_{OZL}‡	V_{CC} = 5.25 V,	V_O = 0.4 V				–100	µA
I_I	V_{CC} = 5.25 V,	V_I = 5.5 V				100	µA
I_{IH}‡	V_{CC} = 5.25 V,	V_I = 2.7 V				25	µA
I_{IL}‡	V_{CC} = 5.25 V,	V_I = 0.4 V				–250	µA
I_{OS}§	V_{CC} = 5.25 V,	V_O = 0.5 V		–30	–70	–130	mA
I_{CC}	V_{CC} = 5.25 V,	V_I = 0,	Outputs open			210	mA
C_i	f = 1 MHz,	V_I = 2 V			8.5		pF
C_o	f = 1 MHz,	V_O = 2 V			10		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ I/O leakage is the worst case of I_{OZL} and I_{IL} or I_{OZH} and I_{IH}, respectively.
§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second. V_O is set at 0.5 V to avoid test problems caused by test equipment ground degradation.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		TEST CONDITIONS	TIBPAL20L8-5CFN		TIBPAL20L8-5CJT TIBPAL20L8-5CNT		UNIT
					MIN	MAX	MIN	MAX	
t_{pd}	I, I/O	O, I/O	with up to 4 outputs switching	R1 = 200 Ω, R2 = 200 Ω, See Figure 8	1.5	5	1.5	5	ns
	I, I/O	O, I/O	with more than 4 outputs switching		1.5	5	1.5	5.5	
t_{en}	I, I/O	O, I/O			2	7	2	7	ns
t_{dis}	I, I/O	O, I/O			2	7	2	7	ns

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) .... 7 V
Input voltage (see Note 1) .... 5.5 V
Voltage applied to disabled output (see Note 1) .... 5.5 V
Operating free-air temperature range .... 0°C to 75°C
Storage temperature range .... −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle or during a preload cycle.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage (see Note 2)		2		5.5	V
V_{IL}	Low-level input voltage (see Note 2)				0.8	V
I_{OH}	High-level output current				−3.2	mA
I_{OL}	Low-level output current				24	mA
f_{clock}	Clock frequency		0		125	MHz
t_w	Pulse duration, clock	High	4			ns
		Low	4			
t_{su}	Setup time, input or feedback before clock↑		4.5			ns
t_h	Hold time, input or feedback after clock↑		0			ns
T_A	Operating free-air temperature		0	25	75	°C

NOTE 2: These are absolute voltage levels with respect to the ground pin of the device and include all overshoots due to system and/or tester noise. Testing these parameters should not be attempted without suitable equipment.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.75 V,	I_I = –18 mA			–0.8	–1.5	V
V_{OH}		V_{CC} = 4.75 V,	I_{OH} = –3.2 mA		2.4	2.7		V
V_{OL}		V_{CC} = 4.75 V,	I_{OL} = 24 mA			0.3	0.5	V
I_{OZH}‡		V_{CC} = 5.25 V,	V_O = 2.7 V				100	µA
I_{OZL}‡		V_{CC} = 5.25 V,	V_O = 0.4 V				–100	µA
I_I		V_{CC} = 5.25 V,	V_I = 5.5 V				100	µA
I_{IH}‡		V_{CC} = 5.25 V,	V_I = 2.7 V				25	µA
I_{IL}‡		V_{CC} = 5.25 V,	V_I = 0.4 V				–250	µA
I_{OS}§		V_{CC} = 5.25 V,	V_O = 0.5 V		–30	–70	–130	mA
I_{CC}		V_{CC} = 5.25 V,	V_I = 0,	Outputs open			210	mA
C_i	I	f = 1 MHz,	V_I = 2 V			8.5		pF
	CLK/$\overline{OE}$					7.5		
C_o	I/O	f = 1 MHz,	V_O = 2 V			10		pF
	Q					7		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TIBPAL20R4-5CFN TIBPAL20R6-5CFN			TIBPAL20R4-5CJT TIBPAL20R4-5CNT TIBPAL20R6-5CJT TIBPAL20R6-5CNT			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}¶	without feedback		R1 = 200 Ω, R2 = 200 Ω, See Figure 8	125			125			MHz
	with internal feedback (counter configuration)			125			125			
	with external feedback			117			111			
t_{pd}	CLK↑	Q		1.5		4	1.5		4.5	ns
t_{pd}	CLK↑	Internal feedback				3.5			3.5	ns
t_{pd}	I, I/O	I/O		1.5		5	1.5		5	ns
t_{en}	$\overline{OE}$↓	Q		1.5		6	1.5		6	ns
t_{dis}	$\overline{OE}$↑	Q		1		6.5	1		7	ns
t_{en}	I, I/O	I/O		2		7	2		7	ns
t_{dis}	I, I/O	I/O		2		7	2		7	ns
t_r					1.5			1.5		ns
t_f					1.5			1.5		ns
$t_{sk(o)}$#	Skew between registered outputs				0.5			0.5		ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ I/O leakage is the worst case of I_{OZL} and I_{IL} or I_{OZH} and I_{IH}, respectively.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second. V_O is set at 0.5 V to avoid test problems caused by test equipment ground degradation.

¶ See 'f_{max} Specification' near the end of this data sheet.

\# $t_{sk(o)}$ is the skew time between registered outputs.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) .... 7 V
Input voltage (see Note 1) .... 5.5 V
Voltage applied to disabled output (see Note 1) .... 5.5 V
Operating free-air temperature range .... 0°C to 75°C
Storage temperature range .... –65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle or during a preload cycle.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage (see Note 2)		2		5.5	V
V_{IL}	Low-level input voltage (see Note 2)				0.8	V
I_{OH}	High-level output current				–3.2	mA
I_{OL}	Low-level output current				24	mA
f_{clock}	Clock frequency		0		125	MHz
t_w	Pulse duration, clock	High	4			ns
		Low	4			
t_{su}	Setup time, input or feedback before clock↑		4.5			ns
t_h	Hold time, input or feedback after clock↑		0			ns
T_A	Operating free-air temperature		0	25	75	°C

NOTE 2: These are absolute voltage levels with respect to the ground pin of the device and include all overshoots due to system and/or tester noise. Testing these parameters should not be attempted without suitable equipment.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		TIBPAL20R8-5CFN			TIBPAL20R8-5CJT TIBPAL20R8-5CNT			UNIT
				MIN	TYP[†]	MAX	MIN	TYP[†]	MAX	
V_{IK}		V_{CC} = 4.75 V,	I_I = –18 mA		–0.8	–1.5		–0.8	–1.5	V
V_{OH}		V_{CC} = 4.75 V,	I_{OH} = –3.2 mA	2.4	2.7		2.4	2.7		V
V_{OL}		V_{CC} = 4.75 V,	I_{OL} = 24 mA		0.3	0.5		0.3	0.5	V
I_{OZH}		V_{CC} = 5.25 V,	V_O = 2.7 V			100			100	µA
I_{OZL}		V_{CC} = 5.25 V,	V_O = 0.4 V			–100			–100	µA
I_I		V_{CC} = 5.25 V,	V_I = 5.5 V			100			100	µA
I_{IH}		V_{CC} = 5.25 V,	V_I = 2.7 V			25			25	µA
I_{IL}		V_{CC} = 5.25 V,	V_I = 0.4 V			–250			–250	µA
I_{OS}[‡]		V_{CC} = 5.25 V,	V_O = 0.5 V	–30	–70	–130	–30	–70	–130	mA
I_{CC}		V_{CC} = 5.25 V,	V_I = 0, Outputs open			210			210	mA
C_i	I	f = 1 MHz,	V_I = 2 V		8.5			6.5		pF
	CLK/$\overline{OE}$				7.5			5.5		
C_o		f = 1 MHz,	V_O = 2 V		10			8		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		TEST CONDITIONS	TIBPAL20R8-5CFN			TIBPAL20R8-5CJT TIBPAL20R8-5CNT			UNIT
					MIN	TYP[†]	MAX	MIN	TYP[†]	MAX	
f_{max}[§]	without feedback			R1 = 200 Ω, R2 = 200 Ω, See Figure 8	125			125			MHz
	with internal feedback (counter configuration)				125			125			
	with external feedback				117			111			
t_{pd}	CLK↑	Q	with up to 4 outputs switching		1.5		4	1.5		4	ns
	CLK↑	Q	with more than 4 outputs switching		1.5		4	1.5		4.5	
t_{pd}[¶]	CLK↑	Internal feedback					3.5			3.5	ns
t_{en}	$\overline{OE}$↓	Q			1.5		6	1.5		6	ns
t_{dis}	$\overline{OE}$↑	Q			1		6.5	1		7	ns
t_r						1.5			1.5		ns
t_f						1.5			1.5		ns
$t_{sk(o)}$[#]	Skew between outputs					0.5			0.5		ns

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[‡] Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second. V_O is set at 0.5 V to avoid test problems caused by test equipment ground degradation.

[§] See 'f_{max} Specification' near the end of this data sheet.

[¶] This parameter is calculated from the measured f_{max} with internal feedback in a counter configuration (see Figure 4 for illustration).

[#] $t_{sk(o)}$ is the skew time between registered outputs.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) .... 7 V
Input voltage (see Note 1) .... 5.5 V
Voltage applied to disabled output (see Note 1) .... 5.5 V
Operating free-air temperature range .... –55°C to 125°C
Storage temperature range .... –65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle or during a preload cycle.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage (see Note 2)		2		5.5	V
V_{IL}	Low-level input voltage (see Note 2)				0.8	V
I_{OH}	High-level output current				–2	mA
I_{OL}	Low-level output current				12	mA
f_{clock}†	Clock frequency		0		100	MHz
t_w†	Pulse duration, clock	High	5			ns
		Low	5			
t_{su}†	Setup time, input or feedback before clock↑		7			ns
t_h†	Hold time, input or feedback after clock↑		0			ns
T_A	Operating free-air temperature		–55	25	125	°C

† f_{clock}, t_w, t_{su}, and t_h do not apply to TIBPAL16L8'

NOTE 2: These are absolute voltage levels with respect to the ground pin of the device and include all overshoots due to system and/or tester noise. Testing these parameters should not be attempted without suitable equipment.

PRODUCT PREVIEW

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−0.8	−1.5	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −2 mA		2.4	2.7		V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA			0.25	0.5	V
I_{OZH}	0, Q outputs	V_{CC} = 5.5 V,	V_O = 2.7 V				20	μA
	I/O ports						100	
I_{OZL}	0, Q outputs	V_{CC} = 5.5 V,	V_O = 0.4 V				−20	μA
	I/O ports						−250	
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V				1	mA
I_{IH}	I/O ports	V_{CC} = 5.5 V,	V_I = 2.7 V				100	μA
	All others						25	
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.4 V				−250	μA
I_{OS}‡		V_{CC} = 5.5 V,	V_O = 0.5 V		−30	−70	−130	mA
I_{CC}		V_{CC} = 5.5 V,	V_I = GND,	$\overline{OE}$ = V_{IH}, Outputs open			220	mA
C_i	I	f = 1 MHz,	V_I = 2 V			8.5		pF
	CLK/$\overline{OE}$					7.5		
C_o		f = 1 MHz,	V_O = 2 V			10		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second. V_O is set at 0.5 V to avoid test problems caused by test equipment ground degradation.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	MAX	UNIT
f_{max}§	without feedback		R1 = 390 Ω, R2 = 750 Ω, See Figure 8	100		MHz
	with internal feedback (counter configuration)			100		
	with external feedback			74		
t_{pd}	I, I/O	O, I/O		1	7	ns
t_{pd}	CLK	Q		1	7	ns
t_{en}	OE↓	Q		1	8	ns
t_{dis}	OE↑	Q		1	10	ns
t_{en}	I, I/O	O, I/O		1	9	ns
t_{dis}	I, I/O	O, I/O		1	10	ns

§ See 'f_{max} Specification' near the end of this data sheet. f_{max} does not apply for TIBPAL20L8'. f_{max} with external feedback is not production tested and is calculated from the equation found in the f_{max} specifications section.

PRODUCT PREVIEW

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

programming information

Texas Instruments programmable logic devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments programmable logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

asynchronous preload procedure for registered outputs (see Figure 1 and Note 3)

The output registers can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below.

Step 1. With V_{CC} at 5 volts and Pin 1 at V_{IL}, raise Pin 13 to V_{IHH}.
Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.
Step 3. Lower Pin 13 to 5 V.
Step 4. Remove output voltage, then lower Pin 13 to V_{IL}. Preload can be verified by observing the voltage level at the output pin.

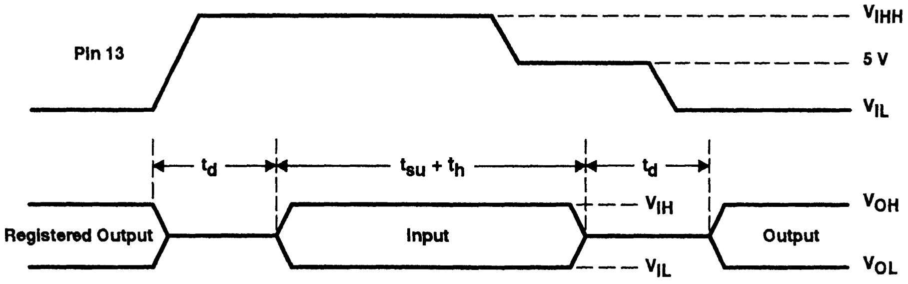
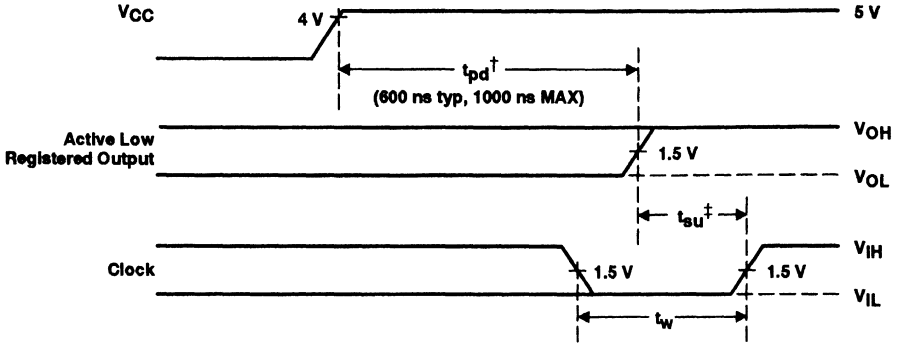


Figure 1. Asynchronous Preload Waveforms

NOTE 3: $t_d = t_{su} = t_h$ = 100 ns to 1000 ns, V_{IHH} = 10.25 V to 10.75 V

power-up reset, see Figure 2

Following power up, all registers are reset to zero. This feature provides extra flexibility to the system designer and is especially valuable in simplifying state-machine initialization. To ensure a valid power-up reset, it is important that the rise of V_{CC} be monotonic. Following power-up reset, a low-to-high clock transition must not occur until all applicable input and feedback setup times are met.



† This is the power-up reset time and applies to registered outputs only. The values shown are from characterization data.
‡ This is the setup time for input or feedback.

Figure 2. Power-Up Reset Waveforms

f_{max} SPECIFICATIONS

f_{max} without feedback, see Figure 3

In this mode, data is presented at the input to the flip-flop and clocked through to the Q output with no feedback. Under this condition, the clock period is limited by the sum of the data setup time and the data hold time ($t_{su} + t_h$). However, the minimum fmax is determined by the minimum clock period (t_w high + t_w low).

$$\text{Thus, fmax without feedback} = \frac{1}{(t_w\text{high} + t_w\text{low})} \text{ or } \frac{1}{(t_{su} + t_h)}.$$

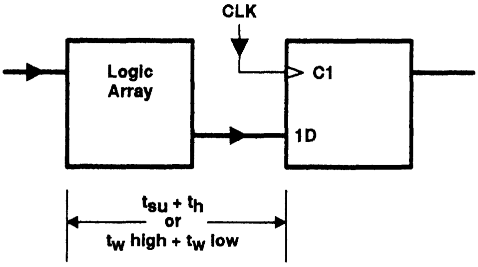


Figure 3. f_{max} Without Feedback

f_{max} with internal feedback, see Figure 4

This configuration is most popular in counters and on-chip state-machine designs. The flip-flop inputs are defined by the device inputs and flip-flop outputs. Under this condition, the period is limited by the internal delay from the flip-flop outputs through the internal feedback and logic array to the inputs of the next flip-flop.

$$\text{Thus, fmax with internal feedback} = \frac{1}{(t_{su} + t_{pd}\ \text{CLK-to-FB})}.$$

Where tpd CLK-to-FB is the deduced value of the delay from CLK to the input of the logic array.

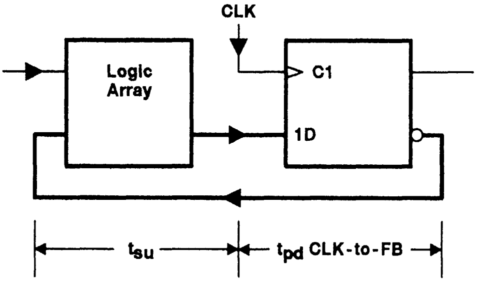


Figure 4. f_{max} With Internal Feedback

f_{max} SPECIFICATIONS

f_{max} with external feedback, see Figure 5

This configuration is a typical state-machine design with feedback signals sent off-chip. This external feedback could go back to the device inputs or to a second device in a multi-chip state machine. The slowest path defining the period is the sum of the clock-to-output time and the input setup time for the external signals (t_{su} + t_{pd} CLK-to-Q).

Thus, f_{max} with external feedback $= \dfrac{1}{(t_{su} + t_{pd}\ \text{CLK}-\text{to}-\text{Q})}$.

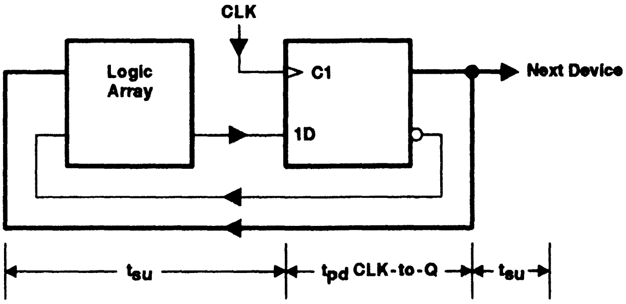


Figure 5. f_{max} With External Feedback

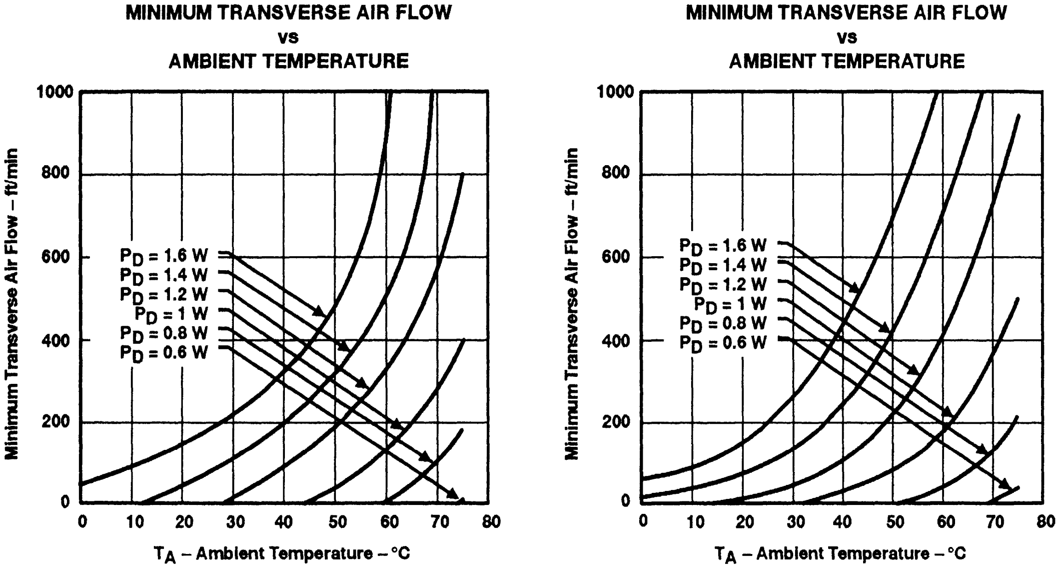
THERMAL INFORMATION

thermal management of the TIBPAL20R8-5C

Thermal management of the TIBPAL20R8-5CNT and TIBPAL20R8-5CFN is necessary when operating at certain conditions of frequency, output loading, and outputs switching simultaneously. The device and system application will determine the appropriate level of management.

Determining the level of thermal management is based on factors such as power dissipation (P_D), ambient temperature (T_A), and transverse airflow (FPM). Figures 6 (a) and 6 (b) show the relationship between ambient temperature and transverse airflow at given power dissipation levels. The required transverse airflow can be determined at a particular ambient temperature and device power dissipation level in order to ensure the device specifications.

Figure 7 illustrates how power dissipation varies as a function of frequency and the number of outputs switching simultaneously. It should be noted that all outputs are fully loaded (C_L = 50 pF). Since the condition of eight fully loaded outputs represents the worst-case condition, each application must be evaluated accordingly.



(a) TIBPAL20-5CNT

(b) TIBPAL20R8-5CFN

Figure 6

THERMAL INFORMATION

POWER DISSIPATION
vs
FREQUENCY

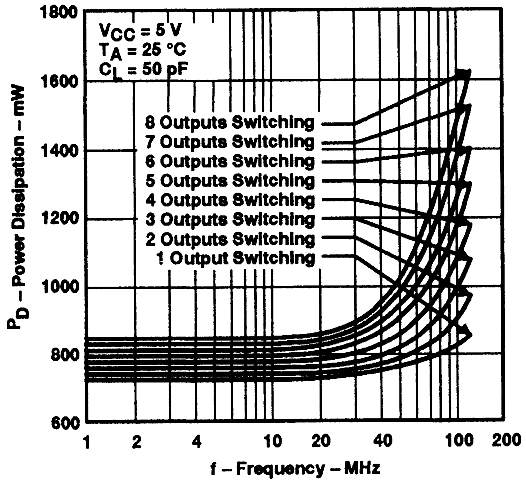
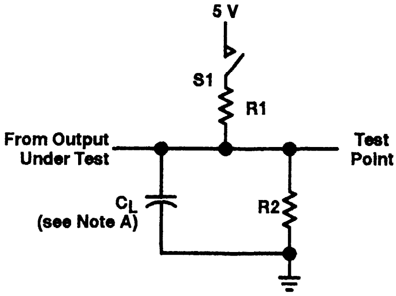
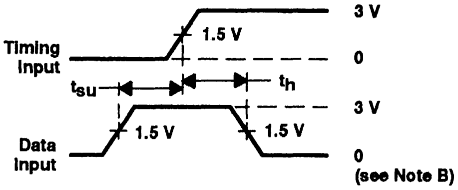


Figure 7

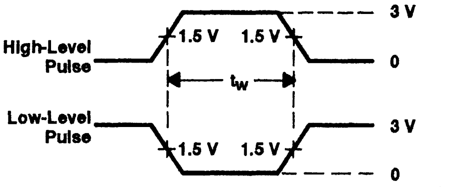
PARAMETER MEASUREMENT INFORMATION



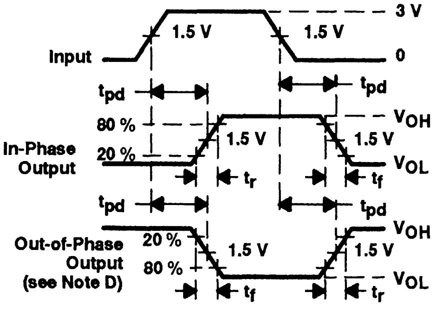
LOAD CIRCUIT FOR 3-STATE OUTPUTS



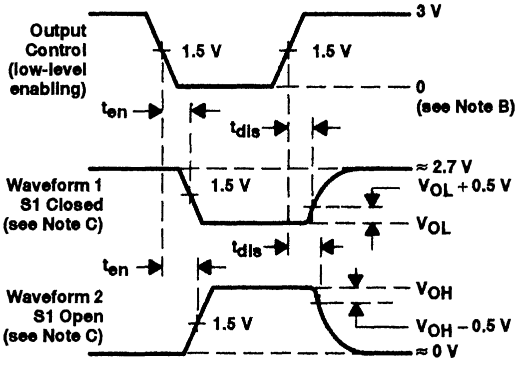
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATIONS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
B. All input pulses have the following characteristics: For C suffix, PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%; For M suffix, PRR ≤ 10 MHz, $t_r = t_f \leq 2$ ns, duty cycle = 50%
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.
E. Equivalent loads may be used for testing.

Figure 8. Load Circuit and Voltage Waveforms

metastable characteristics of TIBPAL20R4-5C, TIBPAL20R6-5C, and TIBPAL20R8-5C

At some point a system designer is faced with the problem of synchronizing two digital signals operating at two different frequencies. This problem is typically overcome by synchronizing one of the signals to the local clock through use of a flip-flop. However, this solution presents an awkward dilemma since the setup and hold time specifications associated with the flip-flop are sure to be violated. The metastable characteristics of the flip-flop can influence overall system reliability.

Whenever the setup and hold times of a flip-flop are violated, its output response becomes uncertain and is said to be in the metastable state if the output hangs up in the region between V_{IL} and V_{IH}. This metastable condition lasts until the flip-flop falls into one of its two stable states, which takes longer than the specified maximum propagation delay time (CLK to Q max).

From a system engineering standpoint, a designer cannot use the specified data sheet maximum for propagation delay time when using the flip-flop as a data synchronizer – how long to wait after the specified data sheet maximum must be known before using the data in order to guarantee reliable system operation.

The circuit shown in Figure 9 can be used to evaluate MTBF (Mean Time Between Failure) and Δt for a selected flip-flop. Whenever the Q output of the DUT is between 0.8 V and 2 V, the comparators are in opposite states. When the Q output of the DUT is higher than 2 V or lower than 0.8 V, the comparators are at the same logic level. The outputs of the two comparators are sampled a selected time (Δt) after SCLK. The exclusive OR gate detects the occurrence of a failure and increments the failure counter.

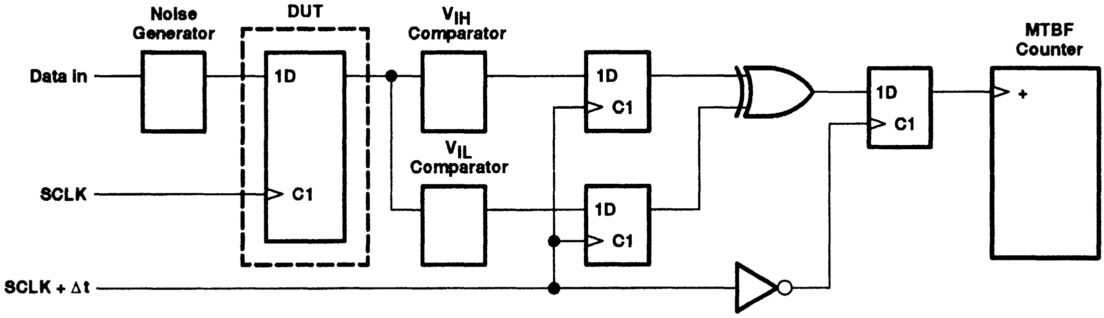
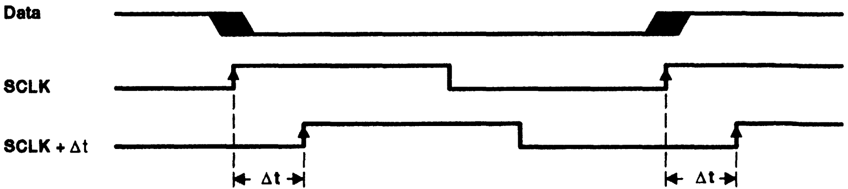


Figure 9. Metastable Evaluation Test Circuit

In order to maximize the possibility of forcing the DUT into a metastable state, the input data signal is applied so that it always violates the setup and hold time. This condition is illustrated in the timing diagram in Figure 10. Any other relationship of SCLK to data will provide less chance for the device to enter into the metastable state.



$$\text{MTBF} = \frac{\text{Time (sec)}}{\text{\# Failures}}$$

$$t_{rec} = \Delta t - \text{CLK to Q (max)}$$

Figure 10. Timing Diagram

By using the described test circuit, MTBF can be determined for several different values of Δt (see Figure 9). Plotting this information on semilog scale demonstrates the metastable characteristics of the selected flip-flop. Figure 11 shows the results for the TIBPAL20'-5C operating at 1 MHz.

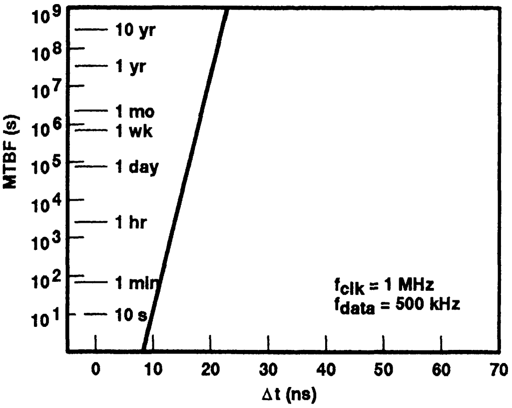


Figure 11. Metastable Characteristics

From the data taken in the above experiment, an equation can be derived for the metastable characteristics at other clock frequencies.

The metastable equation: $\frac{1}{\text{MTBF}} = f_{SCLK} \times f_{data} \times C1 \ e^{(-C2 \times \Delta t)}$

The constants C1 and C2 describe the metastable characteristics of the device. From the experimental data, these constants can be solved for: C1 = 4.37×10^{-3} and C2 = 2.01

Therefore

$$\frac{1}{\text{MTBF}} = f_{SCLK} \times f_{data} \times 4.37 \times 10^{-3} \ e^{(-2.01 \times \Delta t)}$$

definition of variables

DUT (Device Under Test): The DUT is a 5-ns registered PLD programmed with the equation Q : = D.

MTBF (Mean Time Between Failures): The average time (s) between metastable occurrences that cause a violation of the device specifications.

f_{SCLK} (system clock frequency): Actual clock frequency for the DUT.

f_{data} (data frequency): Actual data frequency for a specified input to the DUT.

C1: Calculated constant that defines the magnitude of the curve.

C2: Calculated constant that defines the slope of the curve.

t_{rec} (metastability recovery time): Minimum time required to guarantee recovery from metastability, at a given MTBF failure rate. $t_{rec} = \Delta t - t_{pd}$ (CLK to Q, max)

Δt: The time difference (ns) from when the synchronizing flip-flop is clocked to when its output is sampled.

The test described above has shown the metastable characteristics of the TIBPAL20R4/R6/R8-5C series. For additional information on metastable characteristics of Texas Instruments logic circuits, please refer to TI Applications publication SDAA004, "Metastable Characteristics, Design Considerations for ALS, AS, and LS Circuits."

TYPICAL CHARACTERISTICS

LOW-LEVEL OUTPUT CURRENT vs LOW-LEVEL OUTPUT VOLTAGE

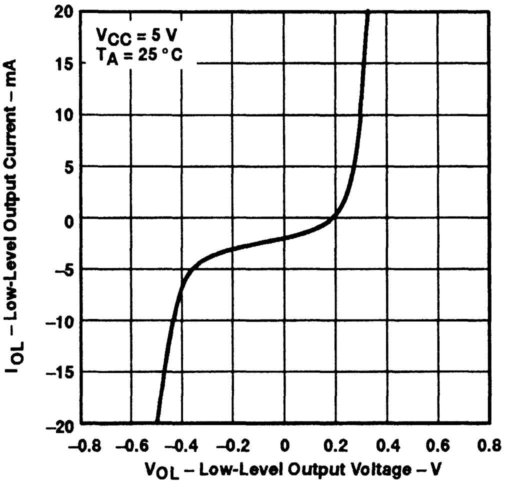


Figure 12

HIGH-LEVEL OUTPUT CURRENT vs HIGH-LEVEL OUTPUT VOLTAGE

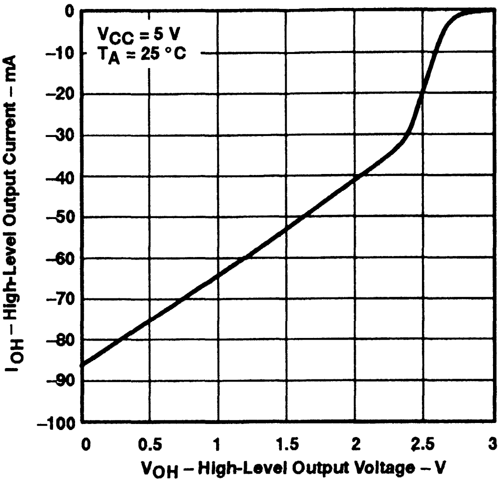


Figure 13

SUPPLY CURRENT vs FREE-AIR TEMPERATURE

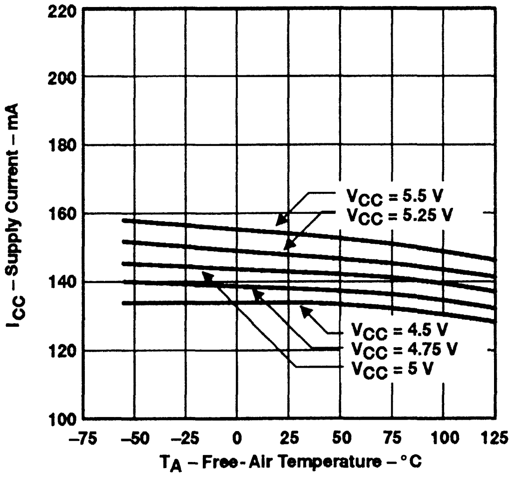


Figure 14

TYPICAL CHARACTERISTICS

POWER DISSIPATION
vs
FREQUENCY
8-BIT COUNTER MODE

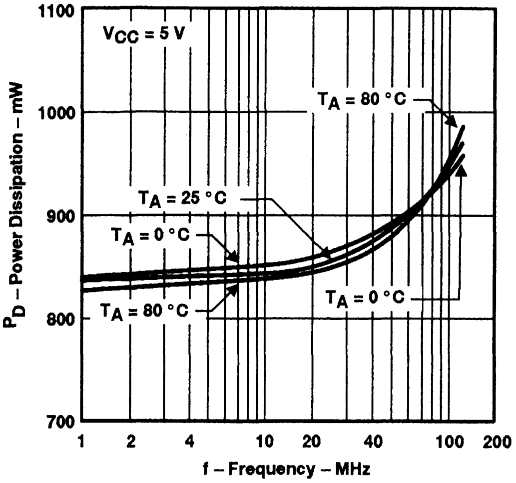


Figure 15

PROPAGATION DELAY TIME
vs
SUPPLY VOLTAGE

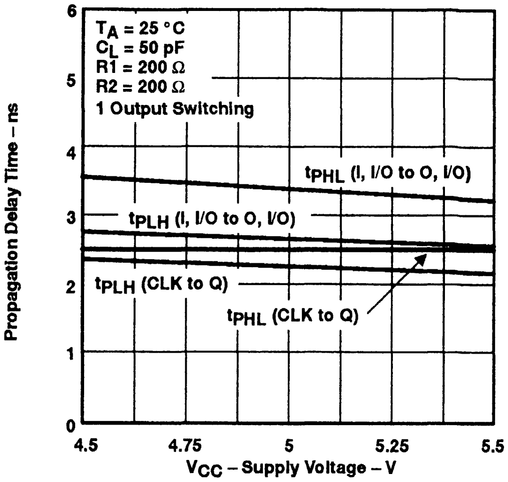


Figure 16

PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

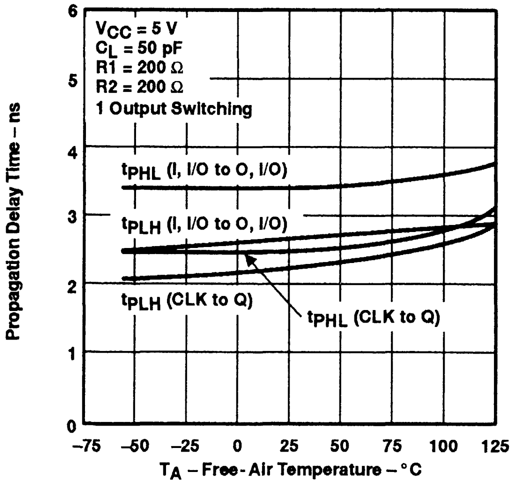


Figure 17

PROPAGATION DELAY TIME
vs
LOAD CAPACITANCE

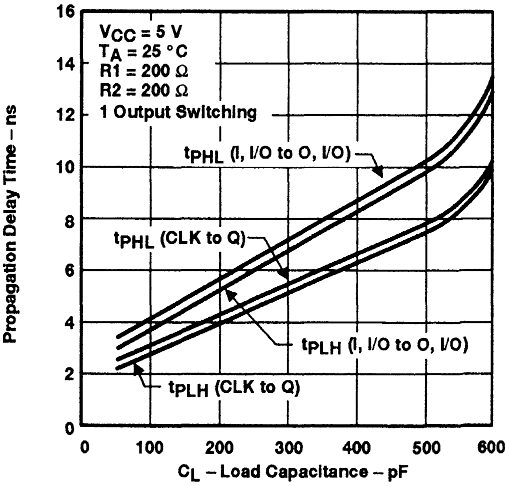
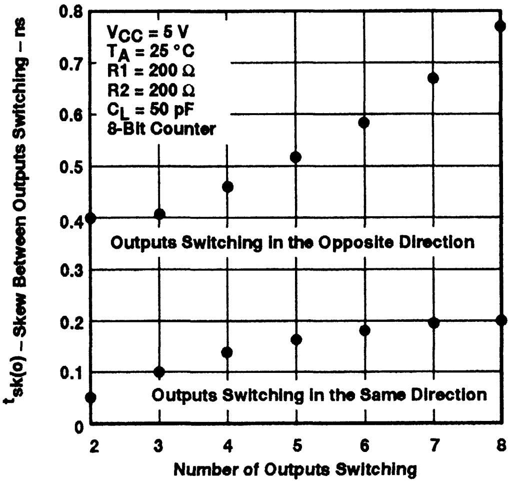


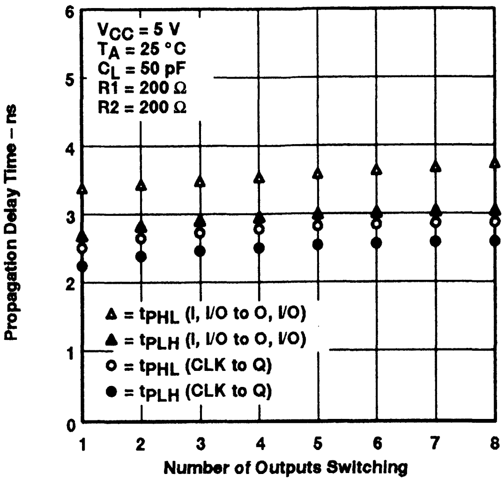
Figure 18

TYPICAL CHARACTERISTICS



SKEW BETWEEN OUTPUTS
vs
NUMBER OF OUTPUTS SWITCHING

Figure 19



PROPAGATION DELAY TIME
vs
NUMBER OF OUTPUTS SWITCHING

Figure 20

TIBPAL20L8-7C, TIBPAL20R4-7C, TIBPAL20R6-7C, TIBPAL20R8-7C
TIBPAL20L8-10M, TIBPAL20R4-10M, TIBPAL20R6-10M, TIBPAL20R8-10M
HIGH-PERFORMANCE *IMPACT-X*™ *PAL*® CIRCUITS

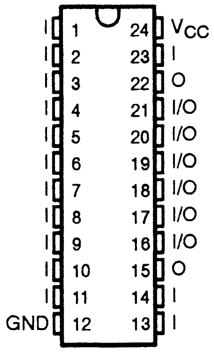
SRPS005C – D3307, OCTOBER 1989 – REVISED MARCH 1992

- **High-Performance Operation:**
  f_{max} (no feedback)
    TIBPAL20R' -7C Series . . . 100 MHz
    TIBPAL20R' -10M Series . . . 62.5 MHz
  f_{max} (internal feedback)
    TIBPAL20R' -7C Series . . . 100 MHz
    TIBPAL20R' -10M Series . . . 62.5 MHz
  f_{max} (external feedback)
    TIBPAL20R' -7C Series . . . 74 MHz
    TIBPAL20R' -10M Series . . . 50 MHz
  Propagation Delay
    TIBPAL20L8-7C Series . . . 7 ns Max
    TIBPAL20L8-10M Series . . . 10 ns Max
- **Functionally Equivalent, but Faster Than Existing 24-Pin PLD Circuits**
- **Preload Capability on Output Registers Simplifies Testing**
- **Power-Up Clear on Registered Devices (All Register Outputs are Set Low, but Voltage Levels at the Output Pins Go High)**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Security Fuse Prevents Duplication**
- **Dependable Texas Instruments Quality and Reliability**

DEVICE	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
PAL20L8	14	2	0	6
PAL20R4	12	0	4 (3-state buffers)	4
PAL20R6	12	0	6 (3-state buffers)	2
PAL20R8	12	0	8 (3-state buffers)	0

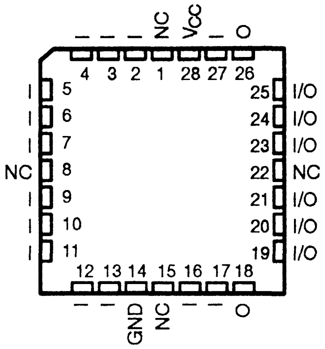
TIBPAL20L8'
C SUFFIX . . . JT OR NT PACKAGE
M SUFFIX . . . JT PACKAGE

(TOP VIEW)



TIBPAL20L8'
C SUFFIX . . . FN PACKAGE
M SUFFIX . . . FK PACKAGE

(TOP VIEW)



NC – No internal connection
Pin assignments in operating mode

description

These programmable array logic devices feature high speed and functional equivalency when compared with currently available devices. These IMPACT-X™ circuits combine the latest Advanced Low-Power Schottky technology with proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional TTL logic. Their easy programmability allows for quick design of custom functions and typically results in a more compact circuit board. In addition, chip carriers are available for futher reduction in board space.

All of the register outputs are set to a low level during power-up. Extra circuitry has been provided to allow loading of each register asynchronously to either a high or low state. This feature simplifies testing because the registers can be set to an initial state prior to executing the test sequence.

The TIBPAL20' C series is characterized from 0°C to 75°C. The TIBPAL20' M series is characterized for operation over the full military temperature range of –55°C to 125°C.

These devices are covered by U.S. Patent 4,410,987.
IMPACT-X is a trademark of Texas Instruments Incorporated.
PAL is a registered trademark of Advanced Micro Devices Inc.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

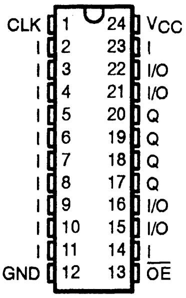
Copyright © 1992, Texas Instruments Incorporated

TEXAS INSTRUMENTS

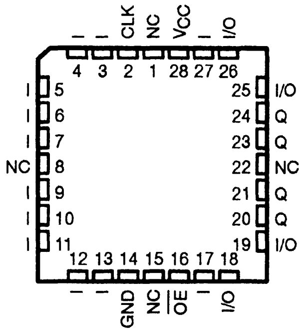
TIBPAL20R4-7C, TIBPAL20R6-7C, TIBPAL20R8-7C
TIBPAL20R4-10M, TIBPAL20R6-10M, TIBPAL20R8-10M
HIGH-PERFORMANCE *IMPACT-X*™ *PAL*® CIRCUITS

SRPS005C – D3307, OCTOBER 1989 – REVISED MARCH 1992

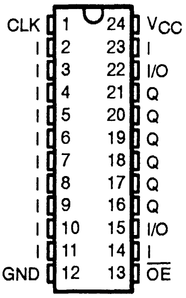
TIBPAL20R4'
C SUFFIX . . . JT OR NT PACKAGE
M SUFFIX . . . JT PACKAGE
(TOP VIEW)



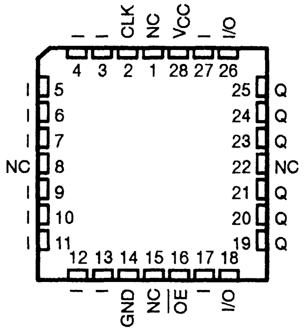
TIBPAL20R4'
C SUFFIX . . . FN PACKAGE
M SUFFIX . . . FK PACKAGE
(TOP VIEW)



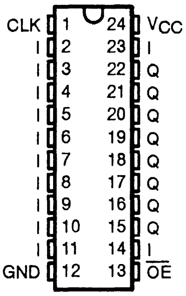
TIBPAL20R6'
C SUFFIX . . . JT OR NT PACKAGE
M SUFFIX . . . JT PACKAGE
(TOP VIEW)



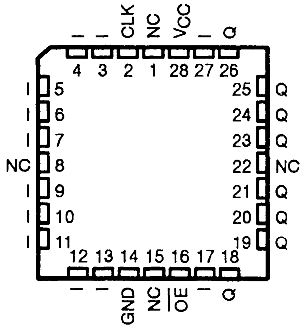
TIBPAL20R6'
C SUFFIX . . . FN PACKAGE
M SUFFIX . . . FK PACKAGE
(TOP VIEW)



TIBPAL20R8'
C SUFFIX . . . JT OR NT PACKAGE
M SUFFIX . . . JT PACKAGE
(TOP VIEW)



TIBPAL20R8'
C SUFFIX . . . FN PACKAGE
M SUFFIX . . . FK PACKAGE
(TOP VIEW)

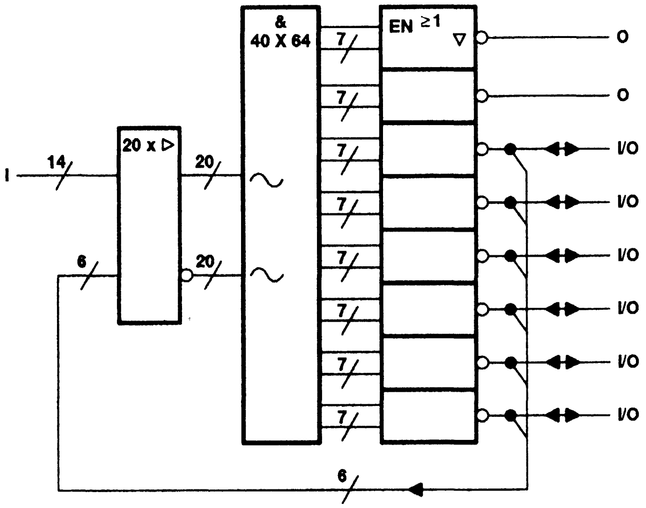


Pin assignments in operating mode

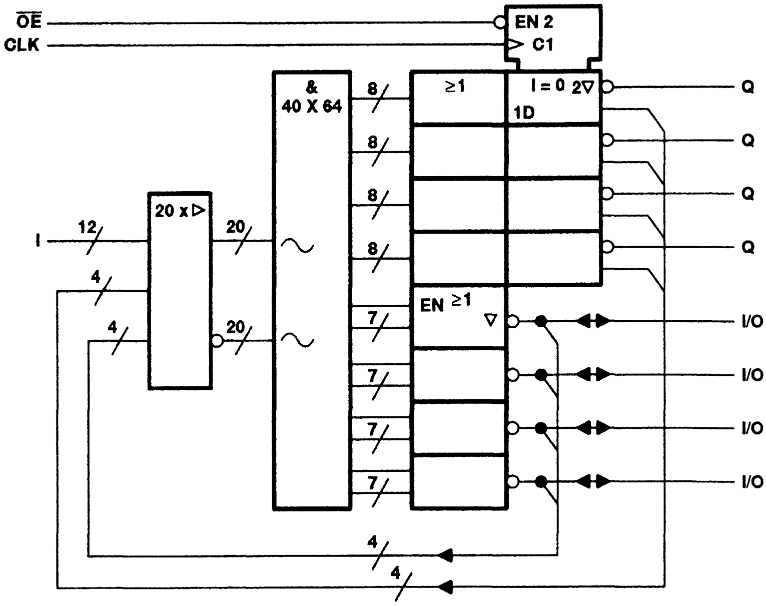
NC — No internal connection

functional block diagrams (positive logic)

TIBPAL20L8'



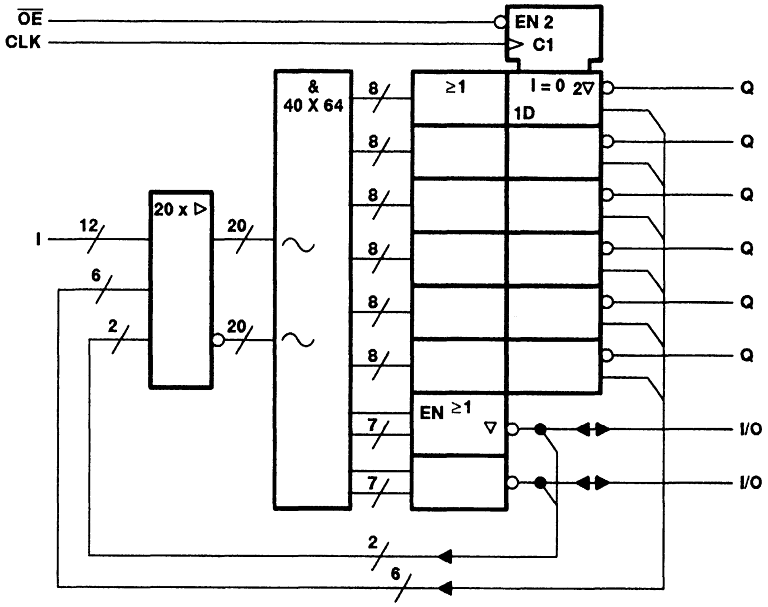
TIBPAL20R4'



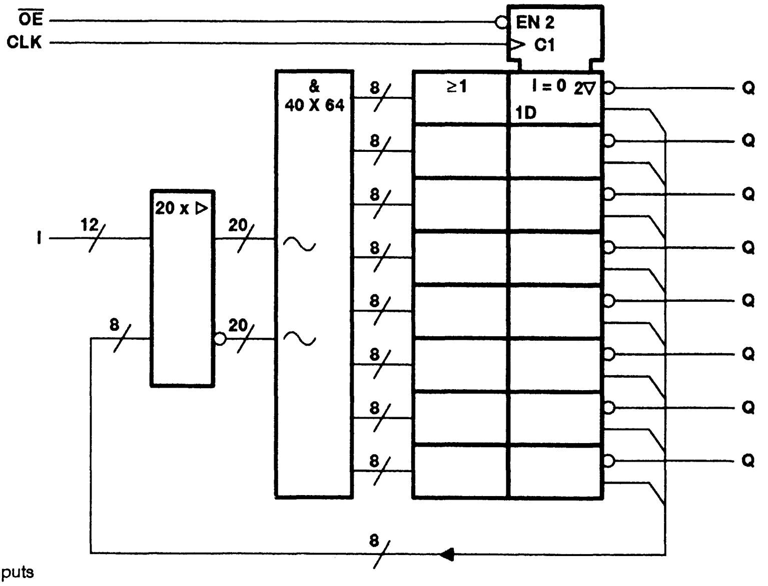
∿ denotes fused inputs

functional block diagrams (positive logic)

TIBPAL20R6'

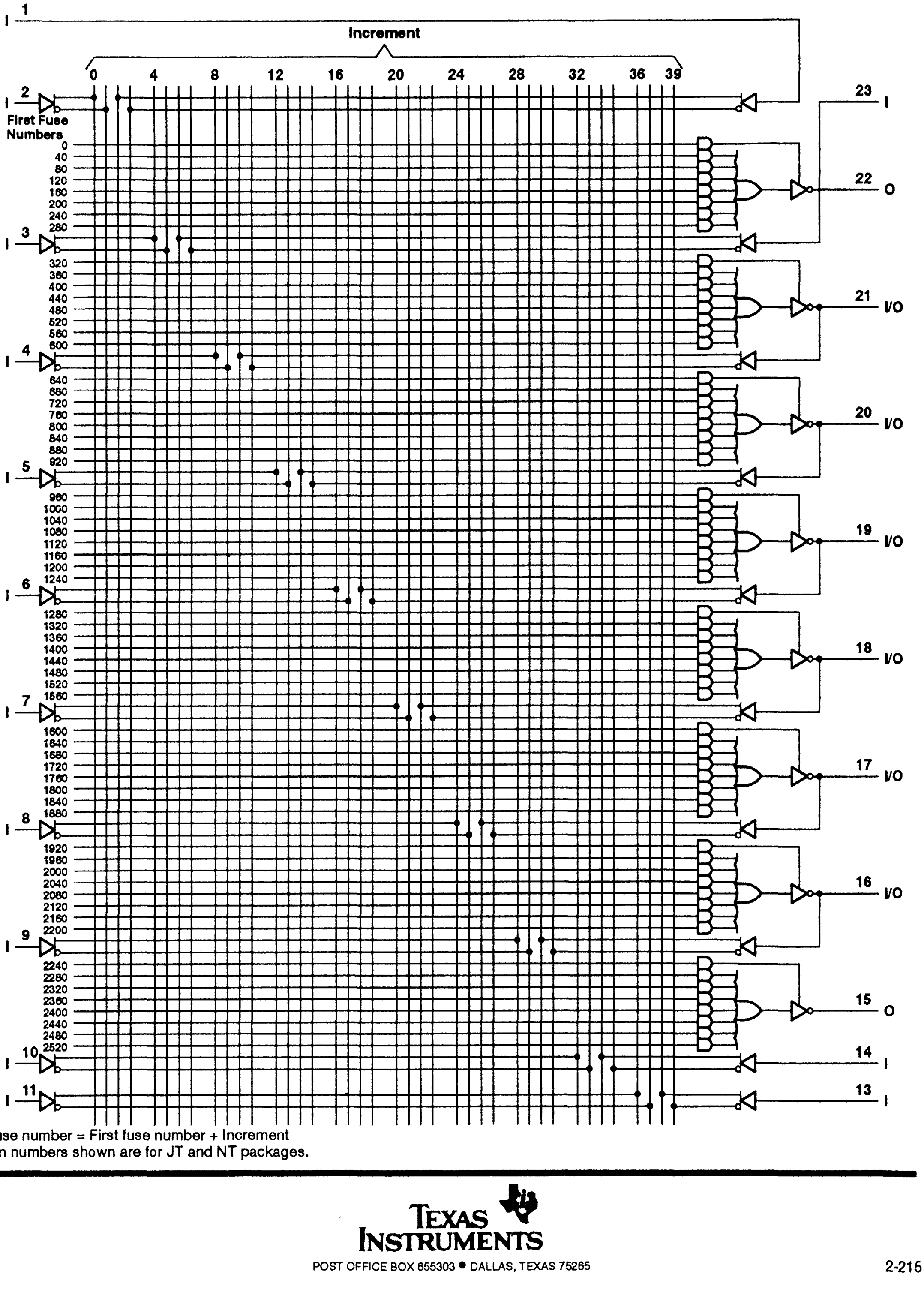


TIBPAL20R8'



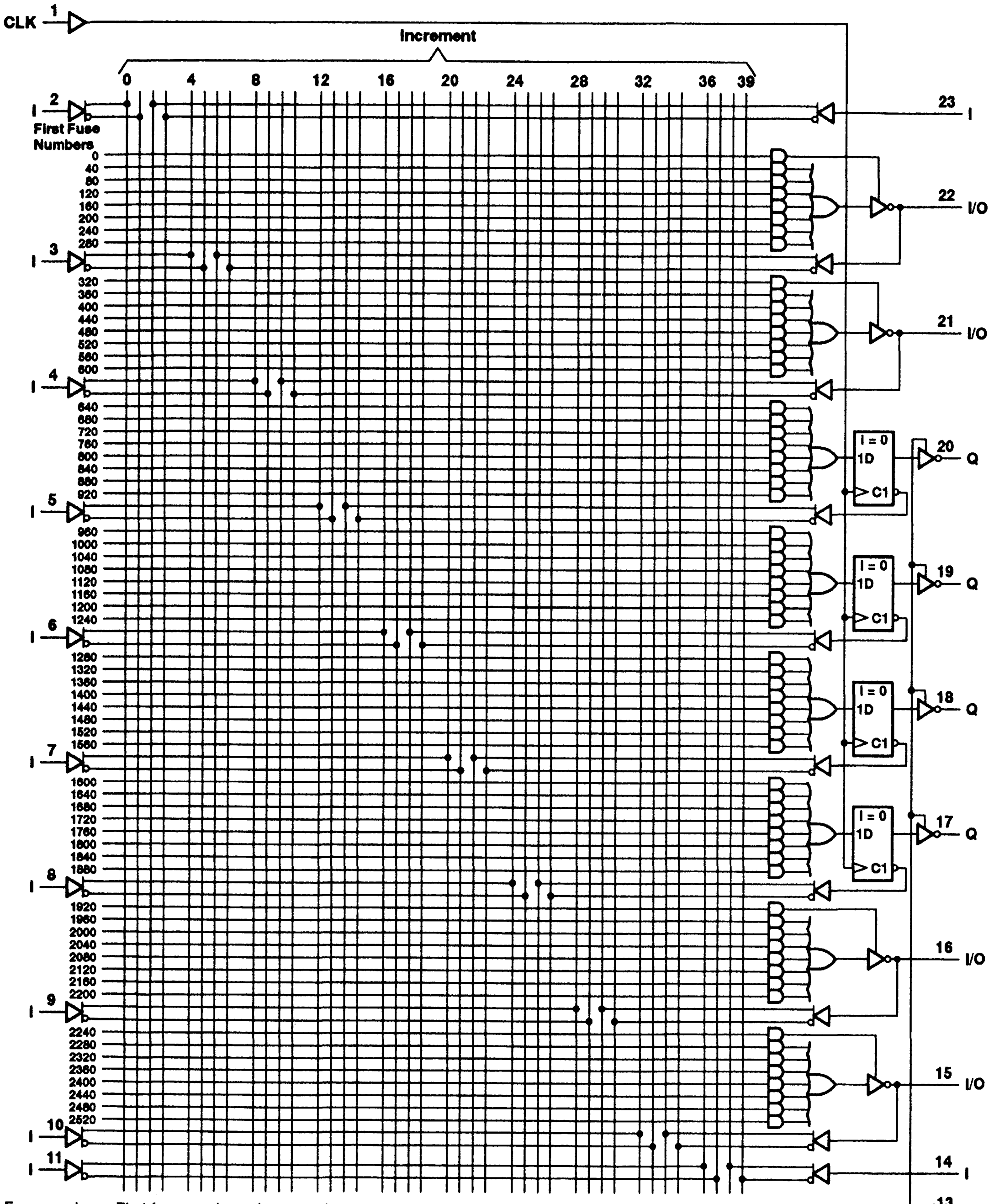
∿ denotes fused inputs

logic diagram (positive logic)



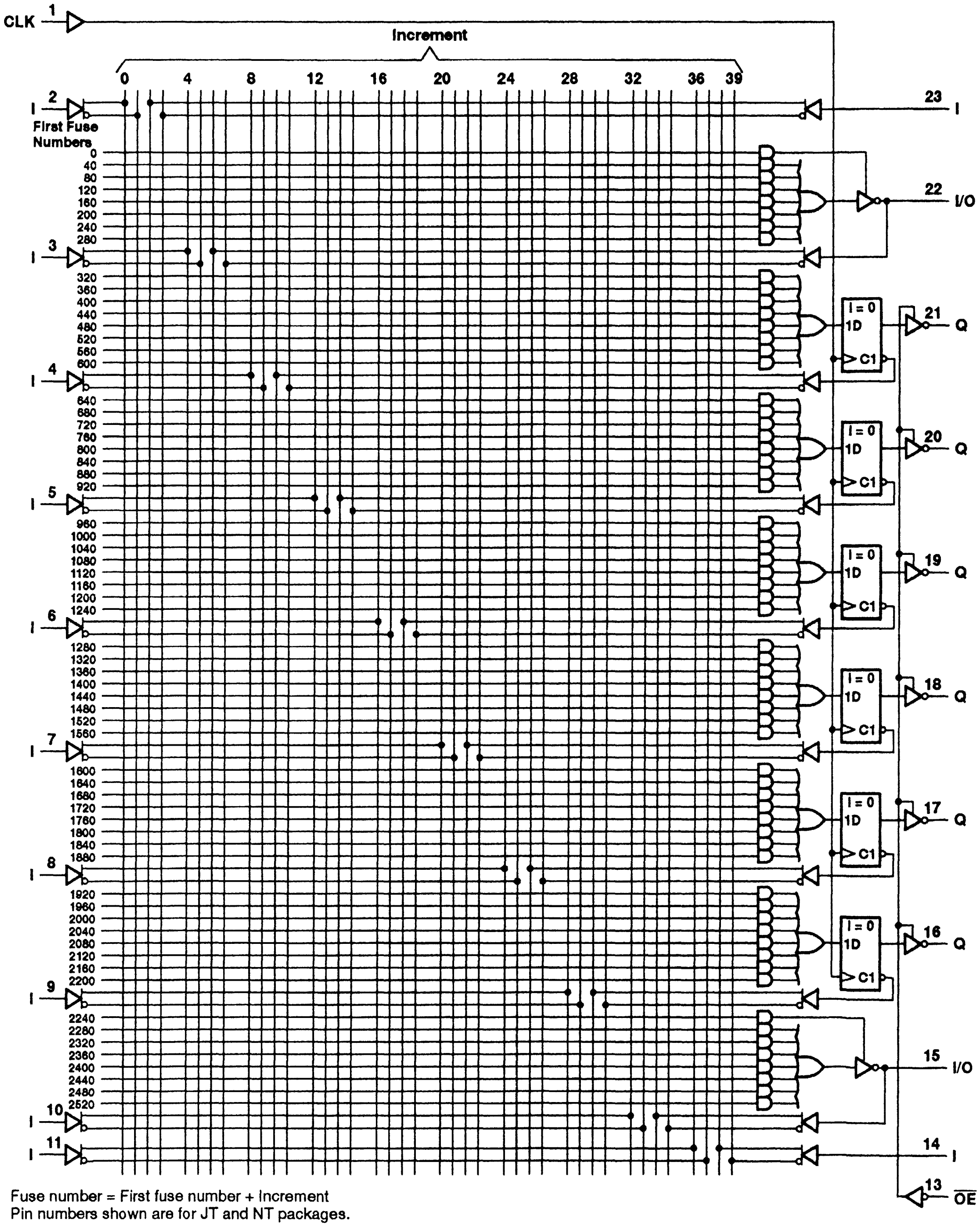
Fuse number = First fuse number + Increment
Pin numbers shown are for JT and NT packages.

logic diagram (positive logic)



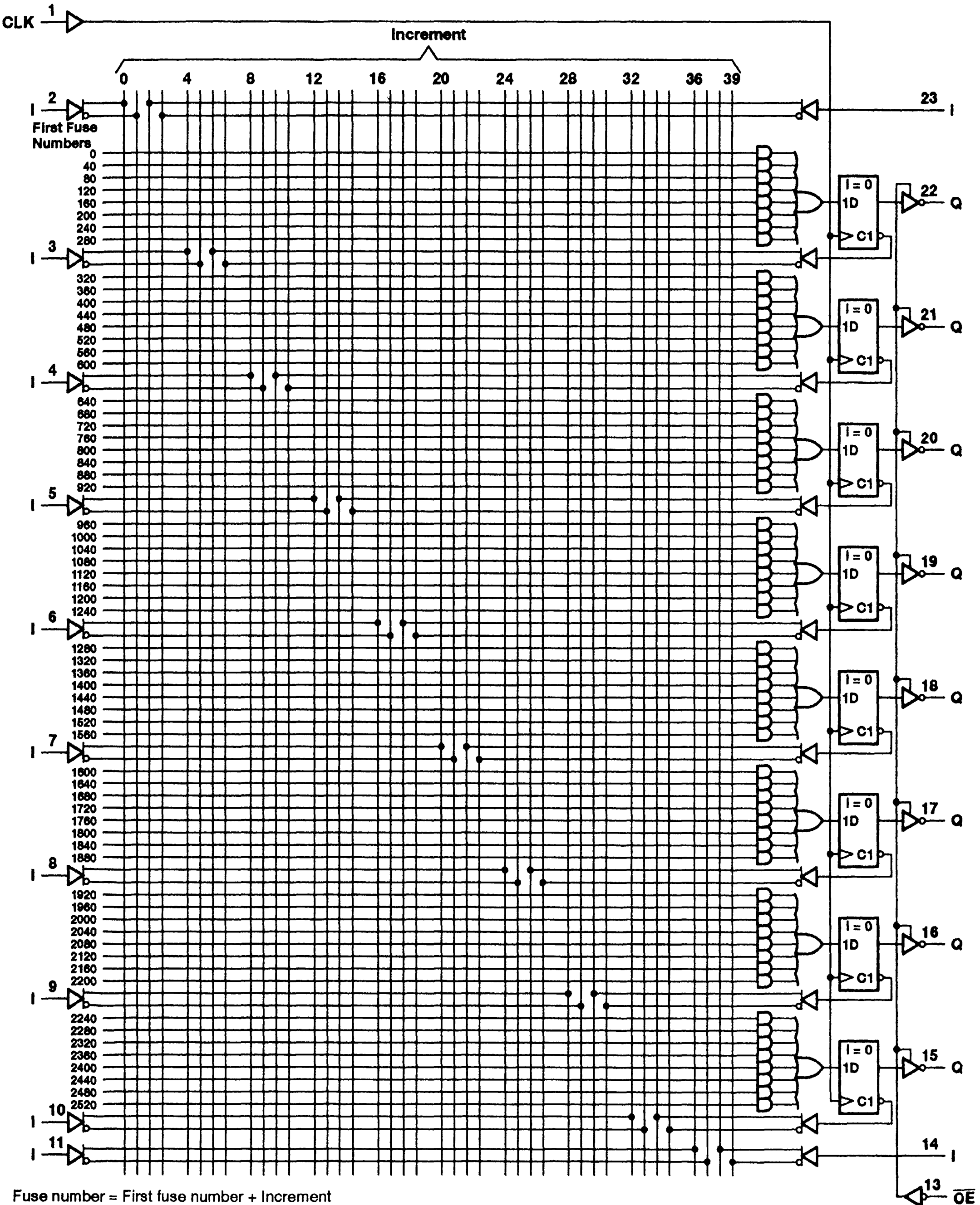
Fuse number = First fuse number + Increment
Pin numbers shown are for JT and NT packages.

logic diagram (positive logic)



Fuse number = First fuse number + Increment
Pin numbers shown are for JT and NT packages.

logic diagram (positive logic)



Fuse number = First fuse number + Increment
Pin numbers shown are for JT and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (see Note 1)	5.5 V
Voltage applied to disabled output (see Note 1)	5.5 V
Operating free-air temperature range	0°C to 75°C
Storage temperature range	–65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage (see Note 2)		2		5.5	V
V_{IL}	Low-level input voltage (see Note 2)				0.8	V
I_{OH}	High-level output current				–3.2	mA
I_{OL}	Low-level output current				24	mA
f_{clock}[†]	Clock frequency		0		100	MHz
t_w[†]	Pulse duration, clock (see Note 2)	High	5			ns
		Low	5			
t_{su}[†]	Setup time, input or feedback before clock↑		7			ns
t_h[†]	Hold time, input or feedback after clock↑		0			ns
T_A	Operating free-air temperature		0	25	75	°C

[†] f_{clock}, t_w, t_{su}, and t_h do not apply for TIBPAL20L8'.

NOTE 2: These are absolute voltage levels with respect to the ground pin of the device and include all overshoots due to system and/or tester noise. Testing these parameters should not be attempted without suitable equipment.

electrical characteristics over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.75 V,	I_I = –18 mA			–0.8	–1.5	V
V_{OH}	V_{CC} = 4.75 V,	I_{OH} = –3.2 mA		2.4	3.2		V
V_{OL}	V_{CC} = 4.75 V,	I_{OL} = 24 mA			0.3	0.5	V
I_{OZH}‡	V_{CC} = 5.25 V,	V_O = 2.7 V				100	µA
I_{OZL}‡	V_{CC} = 5.25 V,	V_O = 0.4 V				–100	µA
I_I	V_{CC} = 5.25 V,	V_I = 5.5 V				100	µA
I_{IH}‡	V_{CC} = 5.25 V,	V_I = 2.7 V				25	µA
I_{IL}‡	V_{CC} = 5.25 V,	V_I = 0.4 V			–80	–250	µA
I_{OS}§	V_{CC} = 5.25 V,	V_O = 0.5 V		–30	–70	–130	mA
I_{CC}	V_{CC} = 5.25 V,	V_I = 0,	Outputs open		150	210	mA
C_i	f = 1 MHz,	V_I = 2 V			5		pF
C_o	f = 1 MHz,	V_O = 2 V			6		pF
C_{clk}	f = 1 MHz,	V_{CLK} = 2 V			6		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)		TEST CONDITION	MIN	TYP†	MAX	UNIT
f_{max}¶	without feedback			R1 = 500 Ω, R2 = 500 Ω, See Figure 6	100			MHz
	with internal feedback (counter configuration)				100			
	with external feedback				74			
t_{pd}	I, I/O	O, I/O	1 or 2 outputs switching		3	5.5	7	ns
			8 outputs switching		3	6	7.5	
t_{pd}	CLK↑	Q			2	4	6.5	ns
t_{pd}#	CLK↑	Feedback input					3	ns
t_{en}	OE↓	Q				4	7.5	ns
t_{dis}	OE↑	Q				4	7.5	ns
t_{en}	I, I/O	O, I/O				6	9	ns
t_{dis}	I, I/O	O, I/O				6	9	ns
$t_{sk(o)}$‖	Skew between registered outputs					0.5		ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ I/O leakage is the worst case of I_{OZL} and I_{IL} or I_{OZH} and I_{IH} respectively.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second. V_O is set at 0.5 V to avoid test problems caused by test equipment ground degradation.

¶ See section for f_{max} specifications.

This parameter applies to TIBPAL20R4' and TIBPAL20R6' only (see Figure 4 for illustration) and is calculated from the measured f_{max} with internal feedback in the counter configuration.

‖ This parameter is the measurement of the difference between the fastest and slowest t_{pd} (CLK-to-Q) observed when multiple registered outputs are switching in the same direction.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (see Note 1)	5.5 V
Voltage applied to disabled output (see Note 1)	5.5 V
Operating free-air temperature range	−55°C to 125°C
Storage temperature range	−65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−2	mA
I_{OL}	Low-level output current				12	mA
f_{clock}†	Clock frequency		0		62.5	MHz
t_w†	Pulse duration, clock (see Note 2)	High	8			ns
		Low	8			
t_{su}†	Setup time, input or feedback before clock↑		10			ns
t_h†	Hold time, input or feedback after clock↑		0			ns
T_A	Operating free-air temperature		−55	25	125	°C

† f_{clock}, t_w, t_{su}, and t_h do not apply for TIBPAL20L8'.

NOTE 2: These are absolute voltage levels with respect to the ground pin of the device and include all overshoots due to system and/or tester noise. Testing these parameters should not be attempted without suitable equipment.

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA		–0.8	–1.5	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = –2 mA	2.4	3.2		V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.3	0.5	V
I_{OZH}‡		V_{CC} = 5.5 V,	V_O = 2.7 V			20	μA
I_{OZL}‡		V_{CC} = 5.5 V,	V_O = 0.4 V			–0.1	mA
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V			1	mA
I_{IH}‡	I/O ports	V_{CC} = 5.5 V,	V_I = 2.7 V			100	μA
	All others					25	
I_{IL}‡		V_{CC} = 5.5 V,	V_I = 0.4 V		–0.08	–0.25	mA
I_{OS}§		V_{CC} = 5.5 V,	V_O = 0.5 V	–30	–70	–130	mA
I_{CC}		V_{CC} = 5.5 V, V_I = 0,	Outputs open OE = V_{IH}		140	220	mA
C_i		f = 1 MHz,	V_I = 2 V		5		pF
C_o		f = 1 MHz,	V_O = 2 V		6		pF
C_{clk}		f = 1 MHz,	V_{CLK} = 2 V		6		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	TYP†	MAX	UNIT
f_{max}¶	without feedback		R1 = 390 Ω, R2 = 750 Ω, See Figure 6	62.5			MHz
	with internal feedback (counter configuration)			62.5			
	with external feedback			50			
t_{pd}	I, I/O	O, I/O		1	6	10	ns
t_{pd}	CLK↑	Q		1	4	10	ns
t_{pd}#	CLK↑	Feedback input				5	ns
t_{en}	OE↓	Q		1	4	10	ns
t_{dis}	OE↑	Q		1	4	10	ns
t_{en}	I, I/O	O, I/O		1	6	12	ns
t_{dis}	I, I/O	O, I/O		1	6	10	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ I/O leakage is the worst case of I_{OZL} and I_{IL} or I_{OZH} and I_{IH} respectively.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second. V_O is set at 0.5 V to avoid test problems caused by test equipment ground degradation.

¶ See section for f_{max} specifications. f_{max} with external feedback is not production tested but is calculated from the equation found in the f_{max} specification section.

This parameter applies to TIBPAL20R4' and TIBPAL20R6' only (see Figure 4 for illustration) and is calculated from the measured f_{max} with internal feedback in the counter configuration.

programming information

Texas Instruments programmable logic devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments programmable logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

preload procedure for registered outputs (see Figure 1 and Note 3)

The output registers can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below.

Step 1. With V_{CC} at 5 volts and Pin 1 at V_{IL}, raise Pin 13 to V_{IHH}.
Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.
Step 3. Pulse Pin 1, clocking in preload data.
Step 4. Remove output voltage, then lower Pin 13 to V_{IL}. Preload can be verified by observing the voltage level at the output pin.

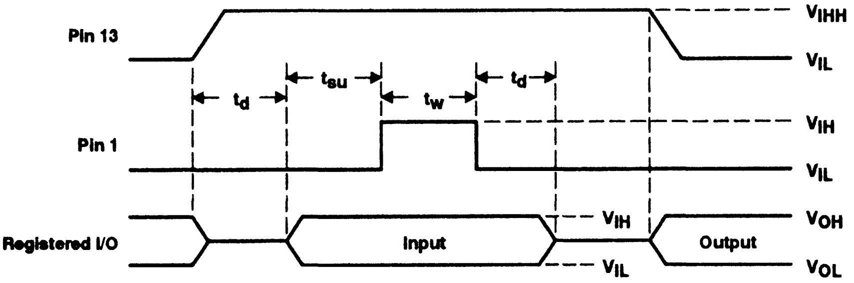
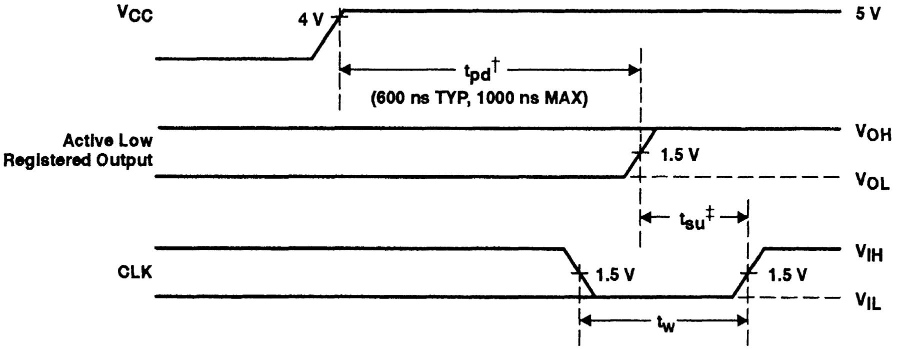


Figure 1. Preload Waveforms

NOTE 3: $t_d = t_{su} = t_h$ = 100 ns to 1000 ns V_{IHH} = 10.25 V to 10.75 v

power-up reset (see Figure 2)

Following power up, all registers are reset to zero. This feature provides extra flexibility to the system designer and is especially valuable in simplifying state-machine initialization. To ensure a valid power-up reset, it is important that the rise of V_{CC} be monotonic. Following power-up reset, a low-to-high clock transition must not occur until all applicable input and feedback setup times are met.



† This is the power-up reset time and applies to registered outputs only. The values shown are from characterization data.
‡ This is the setup time for input or feedback.

Figure 2. Power-Up Reset Waveforms

f_{max} SPECIFICATIONS

f_{max} without feedback, see Figure 3

In this mode, data is presented at the input to the flip-flop and clocked through to the Q output with no feedback. Under this condition, the clock period is limited by the sum of the data setup time and the data hold time ($t_{su} + t_h$). However, the minimum f_{max} is determined by the minimum clock period (t_w high + t_w low).

Thus, f_{max} without feedback $= \dfrac{1}{(t_w\text{high} + t_w\text{low})}$ or $\dfrac{1}{(t_{su} + t_h)}$.

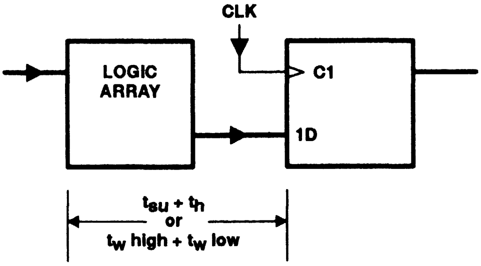


Figure 3. f_{max} Without Feedback

f_{max} with internal feedback, see Figure 4

This configuration is most popular in counters and on-chip state-machine designs. The flip-flop inputs are defined by the device inputs and flip-flop outputs. Under this condition, the period is limited by the internal delay from the flip-flop outputs through the internal feedback and logic array to the inputs of the next flip-flop.

Thus, f_{max} with internal feedback $= \dfrac{1}{(t_{su} + t_{pd}\ \text{CLK-to-FB})}$.

Where tpd CLK-to-FB is the deduced value of the delay from CLK to the input of the logic array.

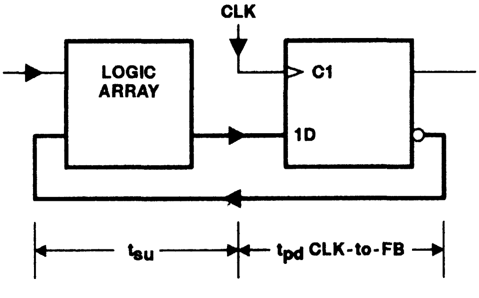


Figure 4. f_{max} With Internal Feedback

f_{max} SPECIFICATIONS

f_{max} with external feedback, see Figure 5

This configuration is a typical state-machine design with feedback signals sent off-chip. This external feedback could go back to the device inputs or to a second device in a multi-chip state machine. The slowest path defining the period is the sum of the clock-to-output time and the input setup time for the external signals (t_{su} + t_{pd} CLK-to-Q).

Thus, f_{max} with external feedback $= \dfrac{1}{(t_{su} + t_{pd}\ \text{CLK}-\text{to}-\text{Q})}$.

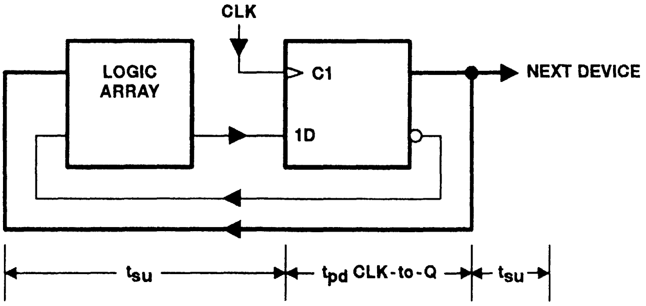
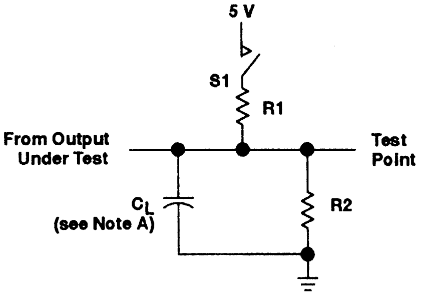
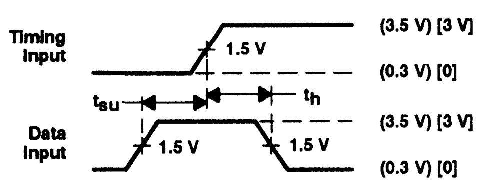


Figure 5. f_{max} With External Feedback

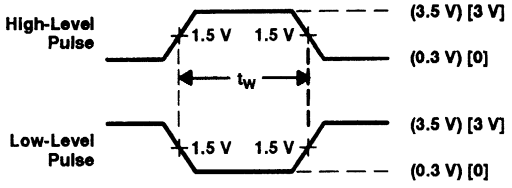
PARAMETER MEASUREMENT INFORMATION



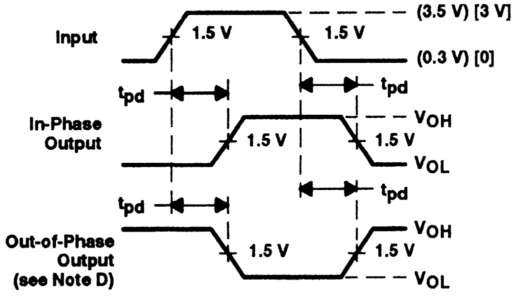
LOAD CIRCUIT FOR
3-STATE OUTPUTS



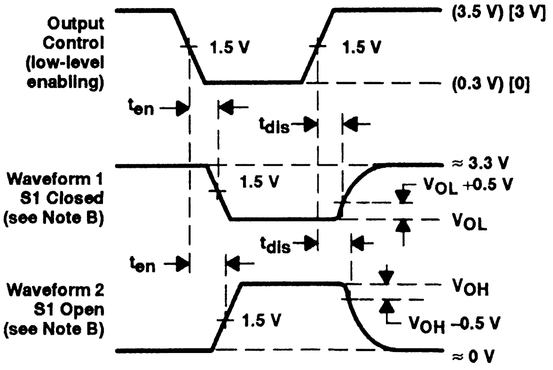
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses have the following characteristics: PRR ≤ 10 MHz, t_r and t_f ≤ 2 ns, duty cycle = 50%. For C suffix, use the voltage levels indicated inparentheses ( ). For M suffix, use the voltage levels indicated in brackets [ ].

D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.

E. Equivalent loads may be used for testing.

Figure 6. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

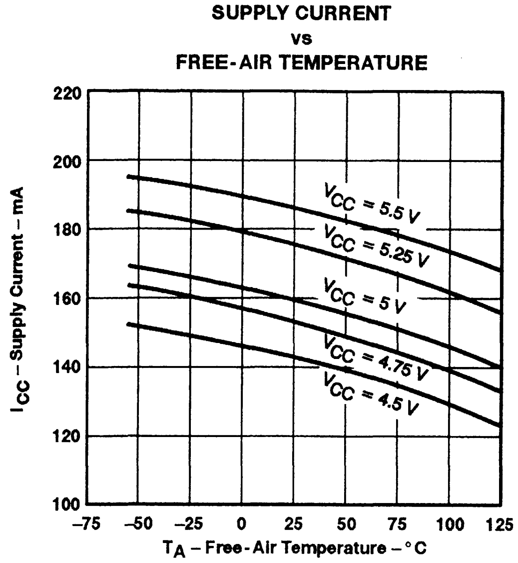

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

Figure 7

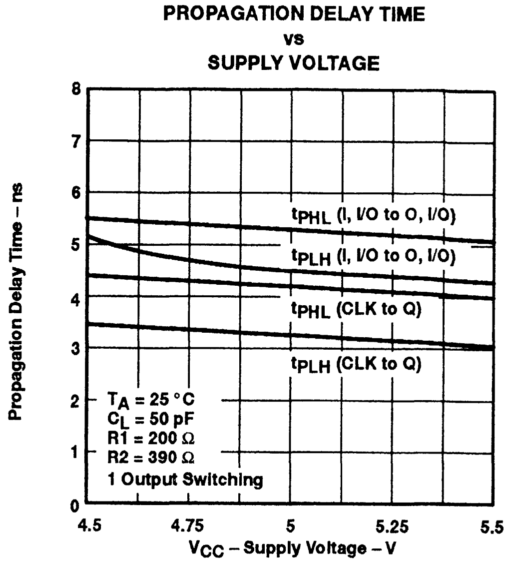

PROPAGATION DELAY TIME
vs
SUPPLY VOLTAGE

Figure 8

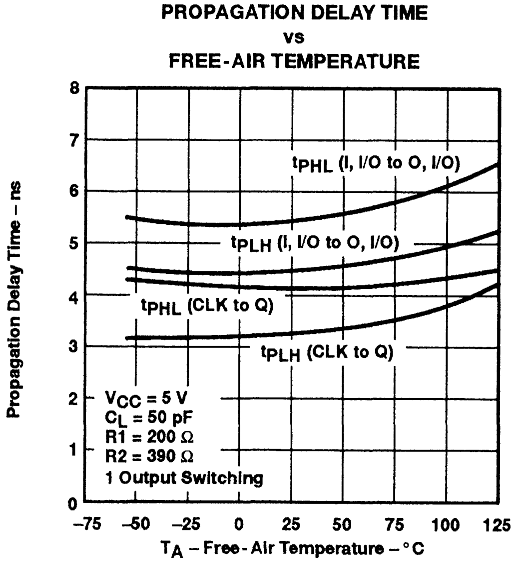

PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

Figure 9

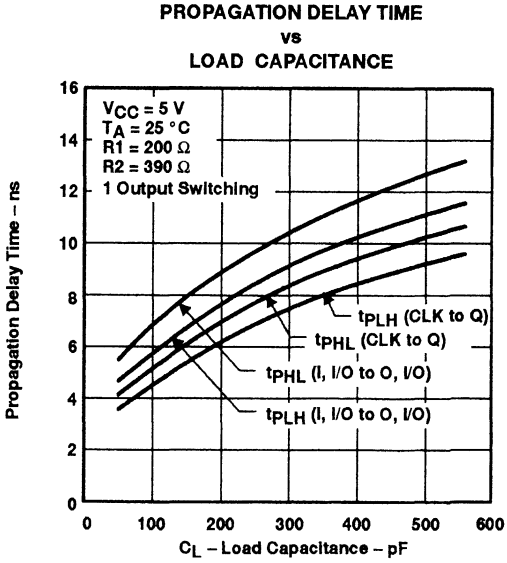

PROPAGATION DELAY TIME
vs
LOAD CAPACITANCE

Figure 10

TYPICAL CHARACTERISTICS

POWER DISSIPATION vs FREQUENCY 8-BIT COUNTER MODE

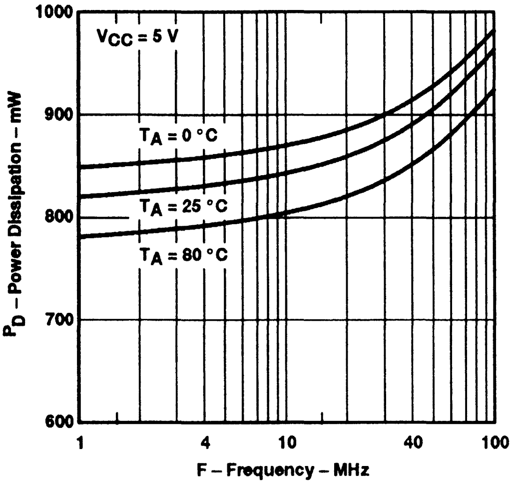


Figure 11

PROPAGATION DELAY TIME† vs NUMBER OF OUTPUTS SWITCHING

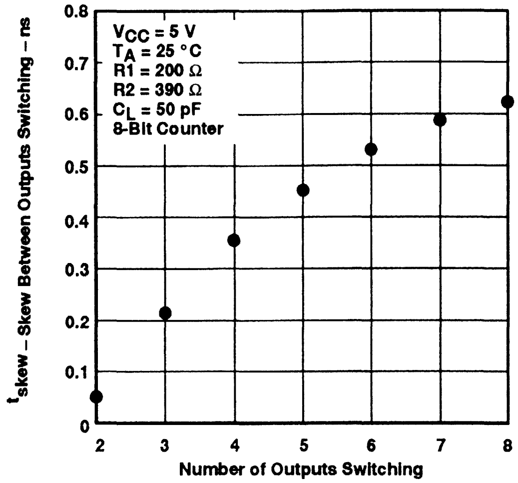


Figure 12

PROPAGATION DELAY TIME vs NUMBER OF OUTPUTS SWITCHING

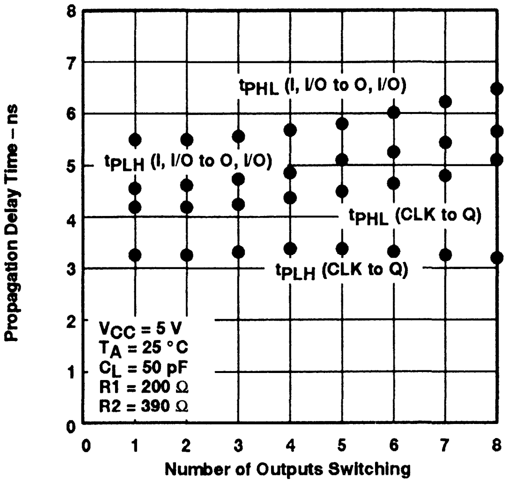


Figure 13

---

†Outputs switching in the same direction (t_{PLH} compared to t_{PLH}/t_{PHL} to t_{PHL})

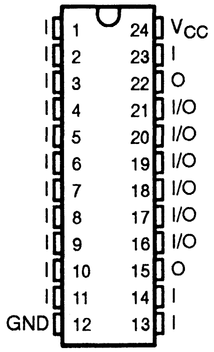
TIBPAL20L8-10C, TIBPAL20R4-10C, TIBPAL20R6-10C, TIBPAL20R8-10C
HIGH-PERFORMANCE *IMPACT-X*™ *PAL*® CIRCUITS

SRPS008A – D3336, OCTOBER 1989 – REVISED MARCH 1992

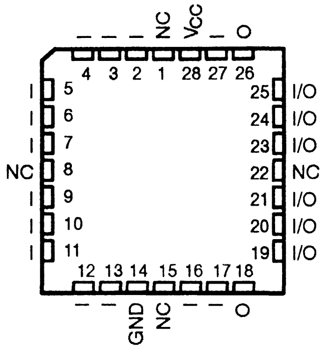
- **High-Performance Operation:**
  f_{max} (no feedback)
  TIBPAL20R' . . . 71.4 MHz
  f_{max} (internal feedback)
  TIBPAL20R' . . . 58.8 MHz
  f_{max} (external feedback)
  TIBPAL20R' . . . 55.5 MHz
  Propagation Delay
  TIBPAL20' . . . 10 ns Max
- **Functionally Equivalent, but Faster Than Existing 24-Pin PLD Circuits**
- **Preload Capability on Output Registers Simplifies Testing**
- **Power-Up Clear on Registered Devices (All Register Outputs are Set Low, but Voltage Levels at the Output Pins Go High)**
- **Package Options Include Plastic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Security Fuse Prevents Duplication**
- **Dependable Texas Instruments Quality and Reliability**

DEVICE	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
PAL20L8	14	2	0	6
PAL20R4	12	0	4 (3-state buffers)	4
PAL20R6	12	0	6 (3-state buffers)	2
PAL20R8	12	0	8 (3-state buffers)	0

TIBPAL20L8'
JT OR NT PACKAGE
(TOP VIEW)



TIBPAL20L8'
FN PACKAGE
(TOP VIEW)



NC – No internal connection
Pin assignments in operating mode

description

These programmable array logic devices feature high speed and functional equivalency when compared with currently available devices. These IMPACT-X™ circuits combine the latest Advanced Low-Power Schottky technology with proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional TTL logic. Their easy programmability allows for quick design of custom functions and typically results in a more compact circuit board. In addition, chip carriers are available for futher reduction in board space.

All of the register outputs are set to a low level during power up. Extra circuitry has been provided to allow loading of each register asynchronously to either a high or low state. This feature simplifies testing because the registers can be set to an initial state prior to executing the test sequence.

The TIBPAL20' C series is characterized from 0°C to 75°C.

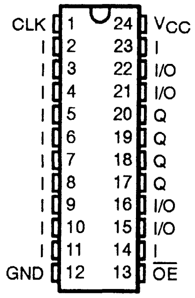
These devices are covered by U.S. Patent 4,410,987.
IMPACT-X is a trademark of Texas Instruments Incorporated.
PAL is a registered trademark of Advanced Micro Devices Inc.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

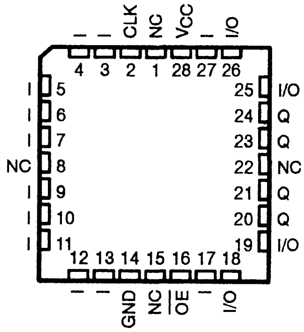
Copyright © 1992, Texas Instruments Incorporated

TIBPAL20R4-10C, TIBPAL20R6-10C, TIBPAL20R8-10C
HIGH-PERFORMANCE *IMPACT-X*™ *PAL*® CIRCUITS

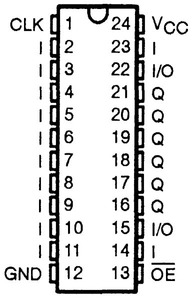
TIBPAL20R4'
JT OR NT PACKAGE
(TOP VIEW)



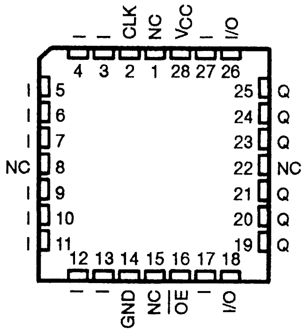
TIBPAL20R4'
FN PACKAGE
(TOP VIEW)



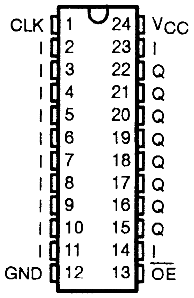
TIBPAL20R6'
JT OR NT PACKAGE
(TOP VIEW)



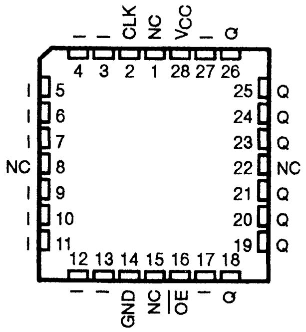
TIBPAL20R6'
FN PACKAGE
(TOP VIEW)



TIBPAL20R8'
JT OR NT PACKAGE
(TOP VIEW)



TIBPAL20R8'
FN PACKAGE
(TOP VIEW)

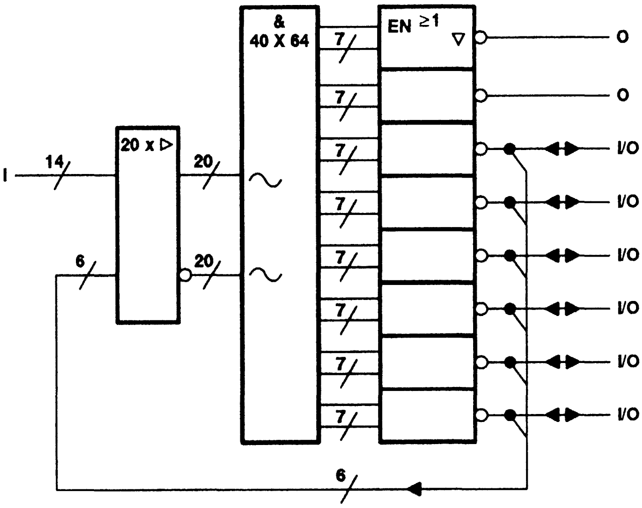


Pin assignments in operating mode

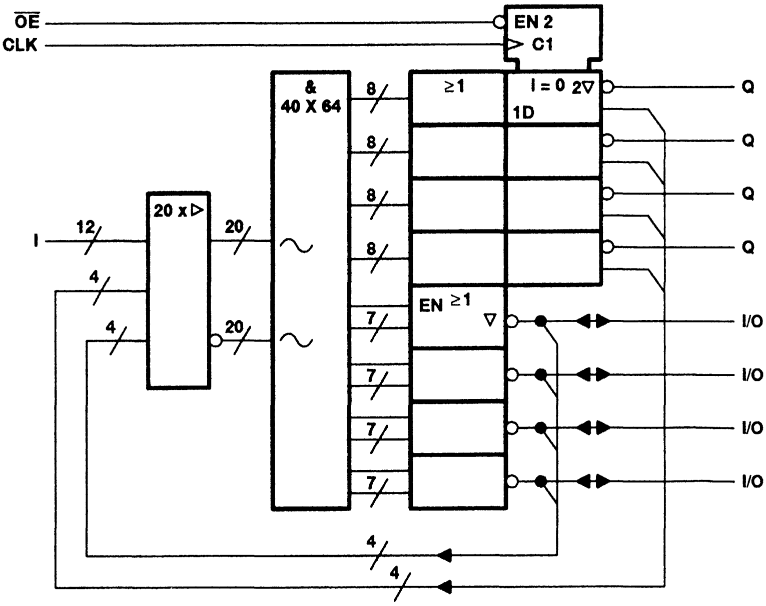
NC – No internal connection

functional block diagrams (positive logic)

TIBPAL20L8'



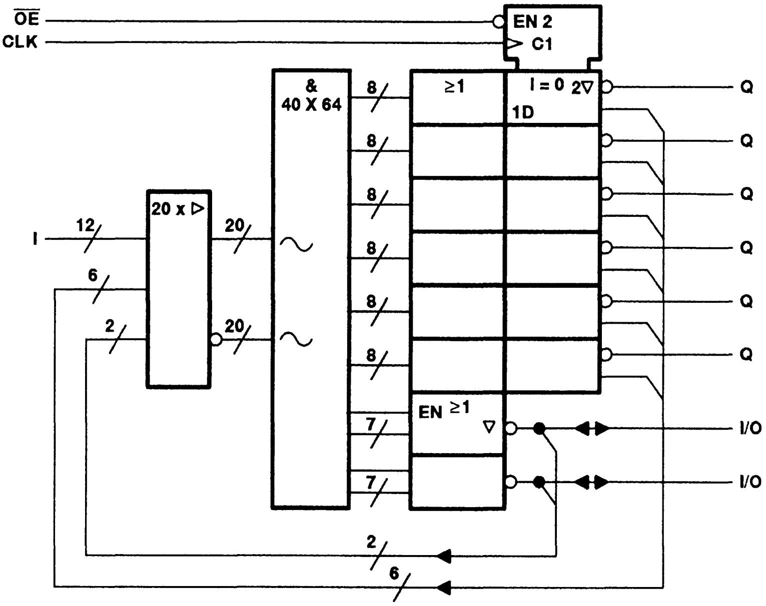
TIBPAL20R4'



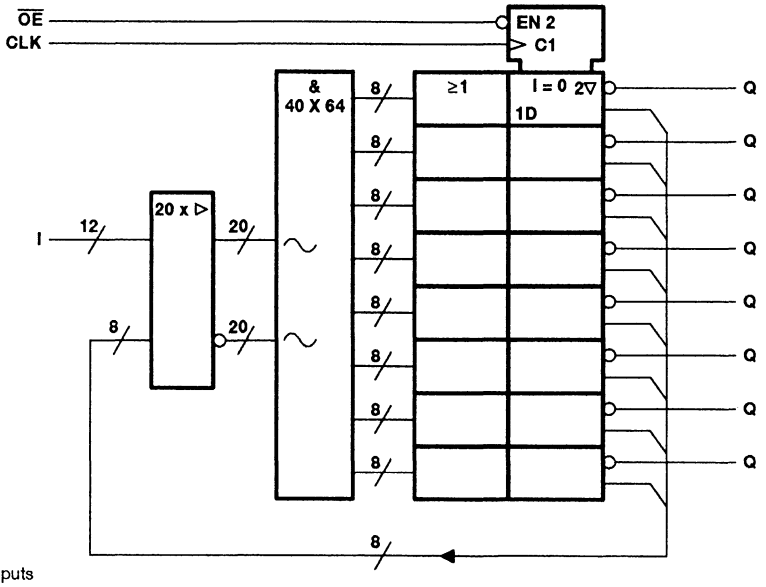
∿ denotes fused inputs

functional block diagrams (positive logic)

TIBPAL20R6'

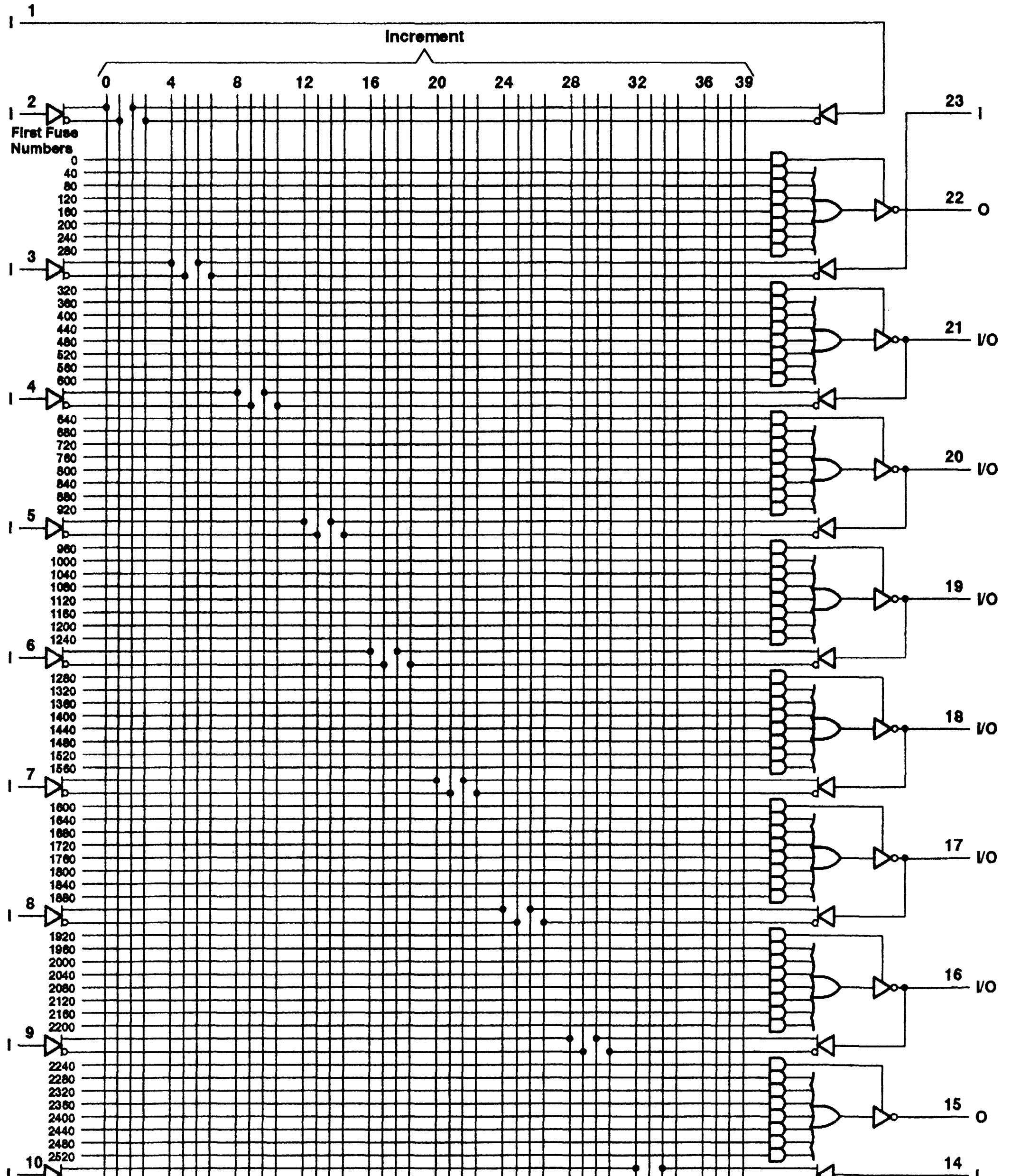


TIBPAL20R8'



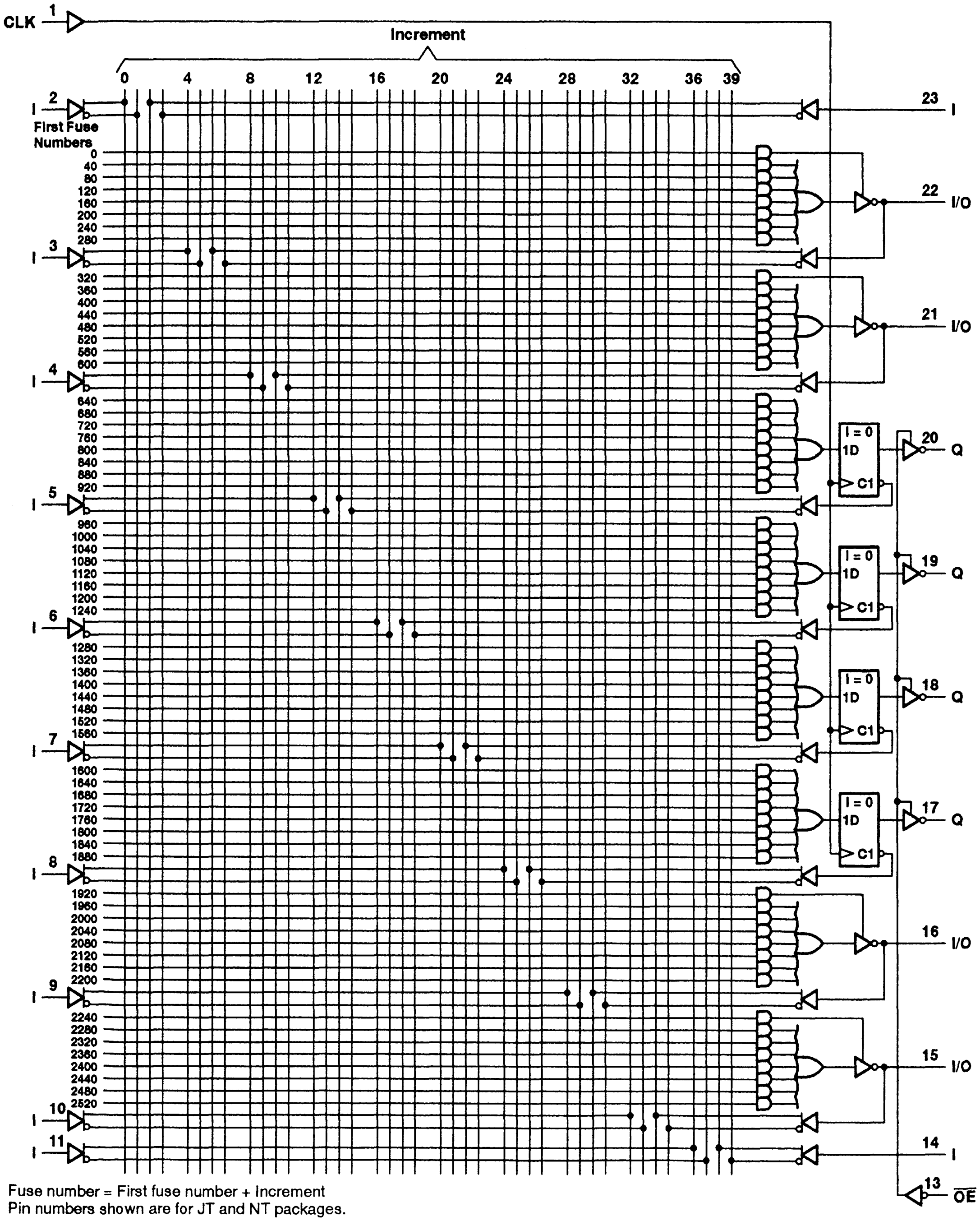
∿ denotes fused inputs

logic diagram (positive logic)



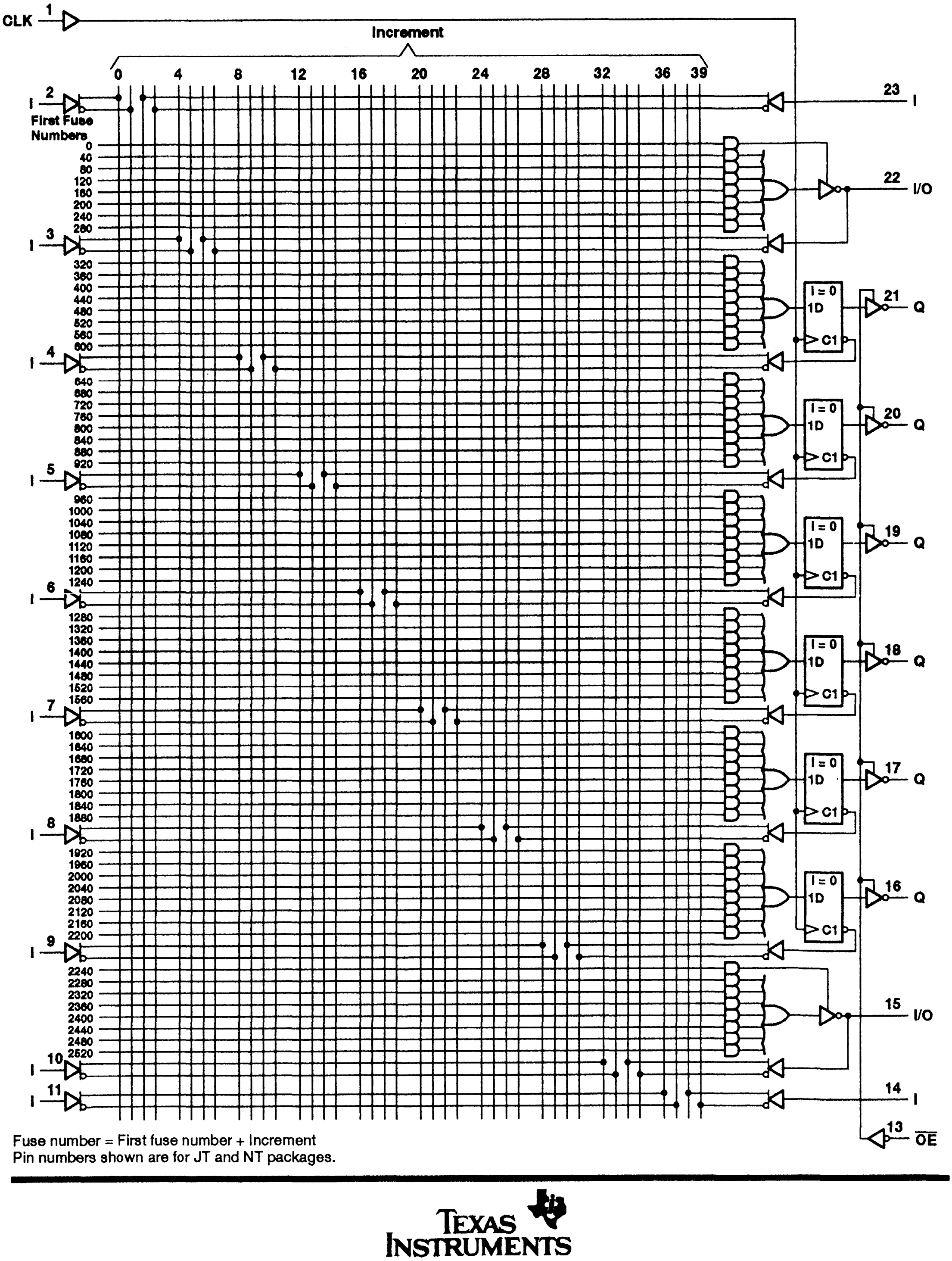
Fuse number = First fuse number + Increment
Pin numbers shown are for JT and NT packages.

logic diagram (positive logic)



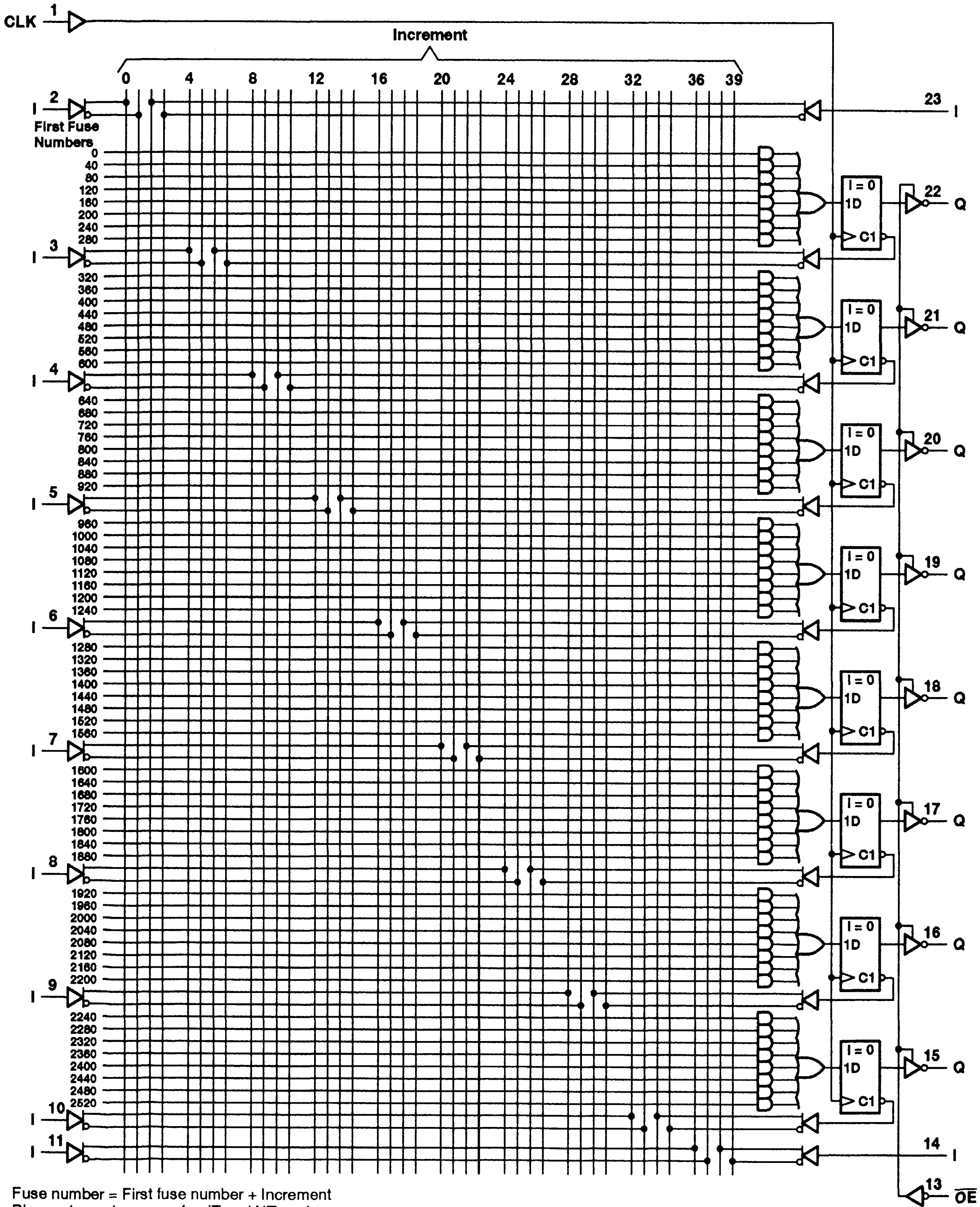
Fuse number = First fuse number + Increment
Pin numbers shown are for JT and NT packages.

logic diagram (positive logic)



Fuse number = First fuse number + Increment
Pin numbers shown are for JT and NT packages.

logic diagram (positive logic)



Fuse number = First fuse number + Increment
Pin numbers shown are for JT and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) .... 7 V
Input voltage (see Note 1) .... 5.5 V
Voltage applied to disabled output (see Note 1) .... 5.5 V
Operating free-air temperature range .... 0°C to 75°C
Storage temperature range .... −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−3.2	mA
I_{OL}	Low-level output current				24	mA
f_{clock}[†]	Clock frequency		0		71.4	MHz
t_w[†]	Pulse duration, clock (see Note 2)	High	7			ns
		Low	7			
t_{su}[†]	Setup time, input or feedback before clock↑		10			ns
t_h[†]	Hold time, input or feedback after clock↑		0			ns
T_A	Operating free-air temperature		0	25	75	°C

[†] f_{clock}, t_w, t_{su}, and t_h do not apply for TIBPAL20L8'.

NOTE 2: These are absolute voltage levels with respect to the ground pin of the device and include all overshoots due to system and/or tester noise. Testing these parameters should not be attempted without suitable equipment.

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP[†]	MAX	UNIT
V_{IK}		V_{CC} = 4.75 V,	I_I = −18 mA		−0.8	−1.5	V
V_{OH}		V_{CC} = 4.75 V,	I_{OH} = −3.2 mA	2.4			V
V_{OL}		V_{CC} = 4.75 V,	I_{OL} = 24 mA		0.3	0.5	V
I_{OZH}[‡]	O, Q outputs	V_{CC} = 5.25 V,	V_O = 2.7 V			20	µA
	I/O ports					100	
I_{OZL}[‡]	O, Q outputs	V_{CC} = 5.25 V,	V_O = 0.4 V			−20	µA
	I/O ports					−100	
I_I		V_{CC} = 5.25 V,	V_I = 5.5 V			0.2	mA
I_{IH}[‡]		V_{CC} = 5.25 V,	V_I = 2.7 V			25	µA
I_{IL}[‡]		V_{CC} = 5.25 V,	V_I = 0.4 V			−0.25	mA
I_{OS}[§]		V_{CC} = 5.25 V,	V_O = 0.5 V	−30	−70	−130	mA
I_{CC}		V_{CC} = 5.25 V, Outputs open,	V_I = 0, $\overline{OE}$ = V_{IH}			210	mA
C_i		f = 1 MHz,	V_I = 2 V		7		pF
C_o		f = 1 MHz,	V_O = 2 V		8		pF
C_{clk}		f = 1 MHz,	V_{CLK} = 2 V		12		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	TYP[†]	MAX	UNIT
f_{max}[¶]	without feedback		R1 = 200 Ω, R2 = 390 Ω, See Figure 6	71.4			MHz
	with internal feedback (counter configuration)			58.8			
	with external feedback			55.5			
t_{pd}	I, I/O	O, I/O		3	8	10	
t_{pd}	CLK↑	Q		2	5	8	ns
t_{pd}[#]	CLK↑	Feedback input				7	ns
t_{en}	OE↓	Q		2	6	10	ns
t_{dis}	OE↑	Q		2	6	10	ns
t_{en}	I, I/O	O, I/O		3	8	10	ns
t_{dis}	I, I/O	O, I/O		2	8	10	ns
$t_{sk(o)}$[‖]	Skew between registered outputs				0.5		ns

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[‡] I/O leakage is the worst case of I_{OZL} and I_{IL} or I_{OZH} and I_{IH} respectively.

[§] Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second. V_O is set at 0.5 V to avoid test problems caused by test equipment ground degradation.

[¶] See section for f_{max} specifications. f_{max} does not apply for TIBPAL20L8'.

[#] This parameter applies to TIBPAL20R4' and TIBPAL20R6' only (see Figure 4 for illustration) and is calculated from the measured f_{max} with internal feedback in the counter configuration.

[‖] This parameter is the measurement of the difference between the fastest and slowest t_{pd} (CLK-to-Q) observed when multiple registered outputs are switching in the same direction.

programming information

Texas Instruments programmable logic devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments programmable logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

preload procedure for registered outputs (see Figure 1 and Note 3)

The output registers can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below.

Step 1. With V_{CC} at 5 volts and Pin 1 at V_{IL}, raise Pin 13 to V_{IHH}.
Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.
Step 3. Pulse Pin 1, clocking in preload data.
Step 4. Remove output voltage, then lower Pin 13 to V_{IL}. Preload can be verified by observing the voltage level at the output pin.

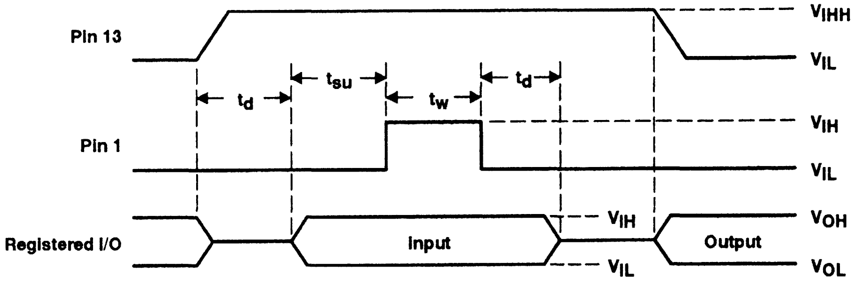
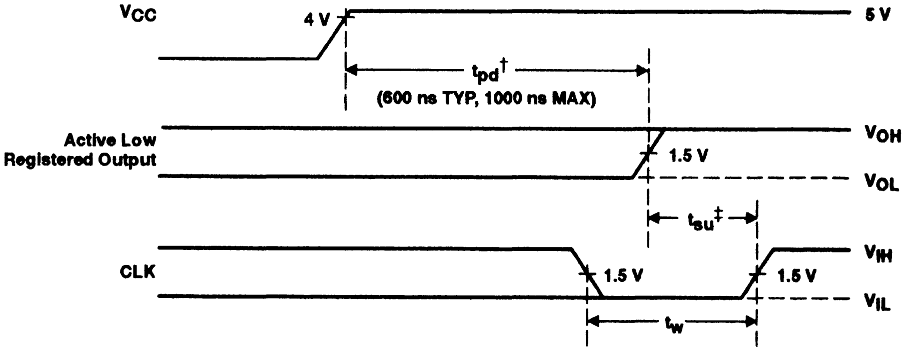


Figure 1. Preload Waveforms

NOTE 3: $t_d = t_{su} = t_h$ = 100 ns to 1000 ns V_{IHH} = 10.25 V to 10.75 v

power-up reset (see Figure 2)

Following power up, all registers are reset to zero. This feature provides extra flexibility to the system designer and is especially valuable in simplifying state-machine initialization. To ensure a valid power-up reset, it is important that the rise of V_{CC} be monotonic. Following power-up reset, a low-to-high clock transition must not occur until all applicable input and feedback setup times are met.



† This is the power-up reset time and applies to registered outputs only. The values shown are from characterization data.
‡ This is the setup time for input or feedback.

Figure 2. Power-Up Reset Waveforms

f_{max} SPECIFICATIONS

f_{max} without feedback, see Figure 3

In this mode, data is presented at the input to the flip-flop and clocked through to the Q output with no feedback. Under this condition, the clock period is limited by the sum of the data setup time and the data hold time ($t_{su} + t_h$). However, the minimum f_{max} is determined by the minimum clock period (t_w high + t_w low).

$$\text{Thus, } f_{max} \text{ without feedback} = \frac{1}{(t_w\text{high} + t_w\text{low})} \text{ or } \frac{1}{(t_{su} + t_h)}.$$

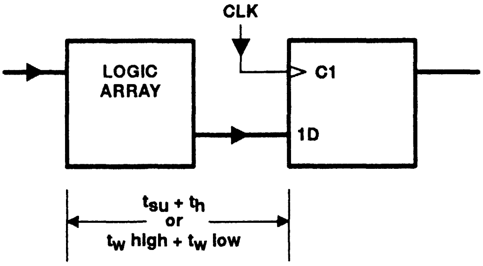


Figure 3. f_{max} Without Feedback

f_{max} with internal feedback, see Figure 4

This configuration is most popular in counters and on-chip state-machine designs. The flip-flop inputs are defined by the device inputs and flip-flop outputs. Under this condition, the period is limited by the internal delay from the flip-flop outputs through the internal feedback and logic array to the inputs of the next flip-flop.

$$\text{Thus, } f_{max} \text{ with internal feedback} = \frac{1}{(t_{su} + t_{pd} \text{ CLK-to-FB})}.$$

Where tpd CLK-to-FB is the deduced value of the delay from CLK to the input of the logic array.

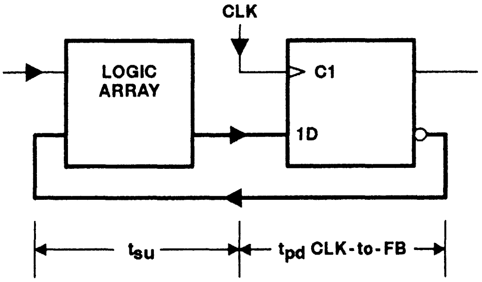


Figure 4. f_{max} With Internal Feedback

f_{max} SPECIFICATIONS

f_{max} with external feedback, see Figure 5

This configuration is a typical state-machine design with feedback signals sent off-chip. This external feedback could go back to the device inputs or to a second device in a multi-chip state machine. The slowest path defining the period is the sum of the clock-to-output time and the input setup time for the external signals (t_{su} + t_{pd} CLK-to-Q).

$$\text{Thus, } f_{max} \text{ with external feedback } = \frac{1}{(t_{su} + t_{pd} \text{ CLK}-\text{to}-\text{Q})}.$$

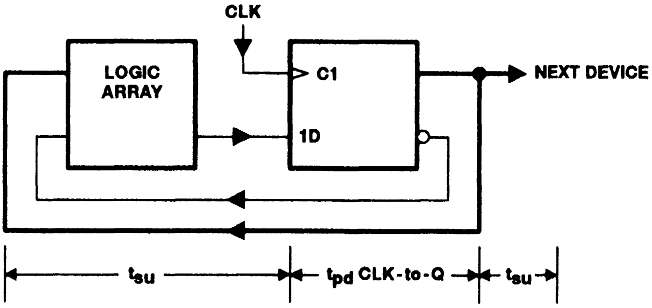
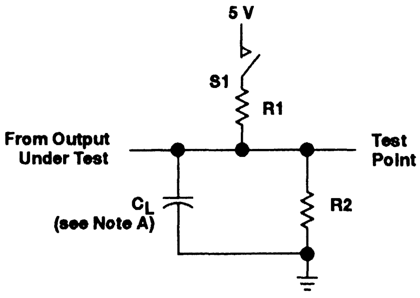
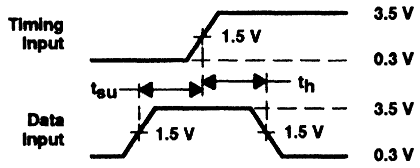


Figure 5. f_{max} With External Feedback

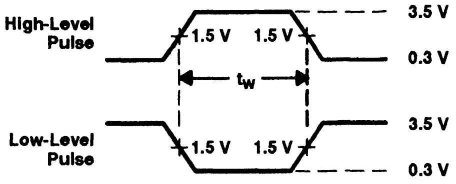
PARAMETER MEASUREMENT INFORMATION



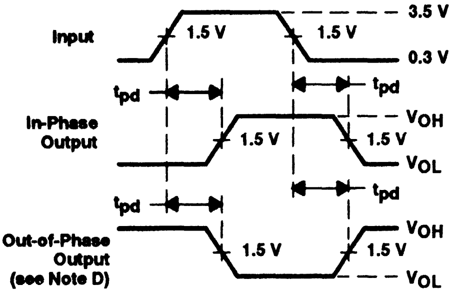
LOAD CIRCUIT FOR
3-STATE OUTPUTS



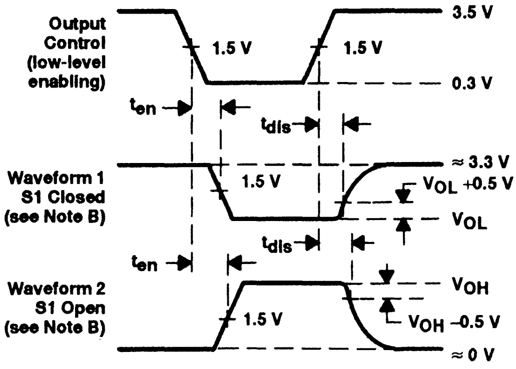
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f \leq 2$ ns, duty cycle = 50%.
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.
E. Equivalent loads may be used for testing.

Figure 6. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

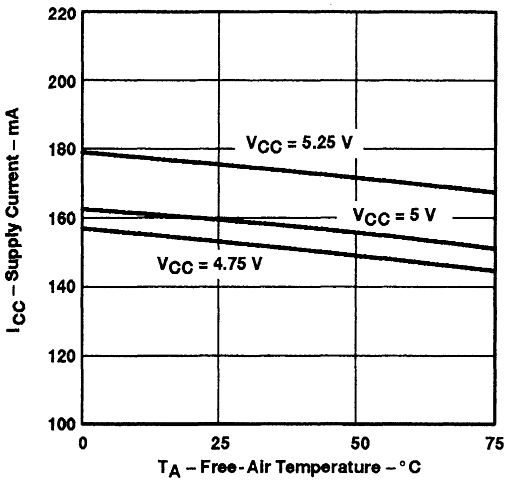


Figure 7

PROPAGATION DELAY TIME
vs
SUPPLY VOLTAGE

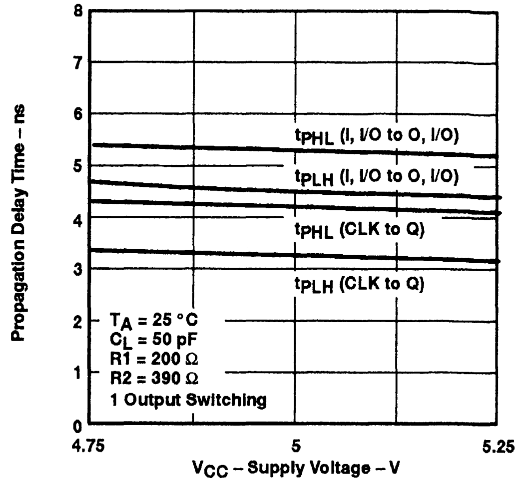


Figure 8

PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

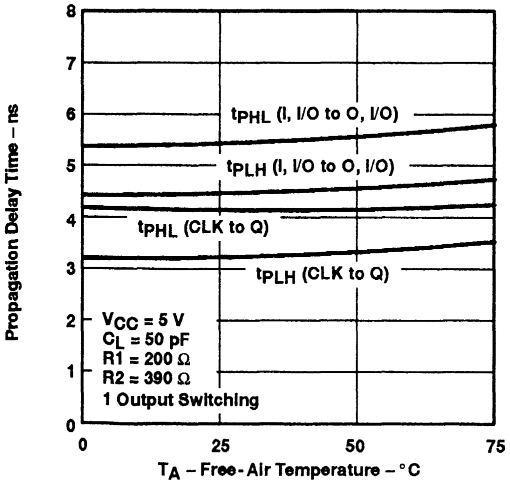


Figure 9

PROPAGATION DELAY TIME
vs
LOAD CAPACITANCE

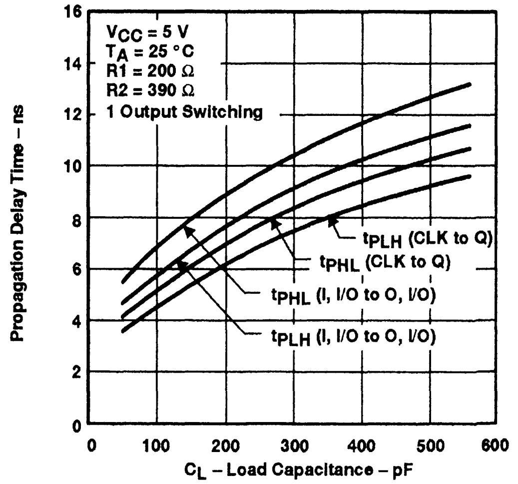


Figure 10

TYPICAL CHARACTERISTICS

POWER DISSIPATION vs FREQUENCY 8-BIT COUNTER MODE

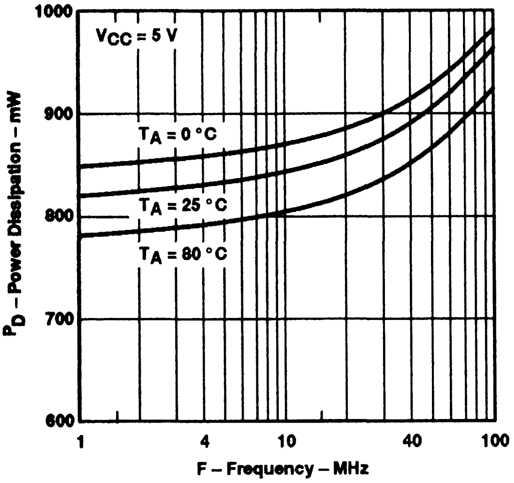


Figure 11

PROPAGATION DELAY TIME† vs NUMBER OF OUTPUTS SWITCHING

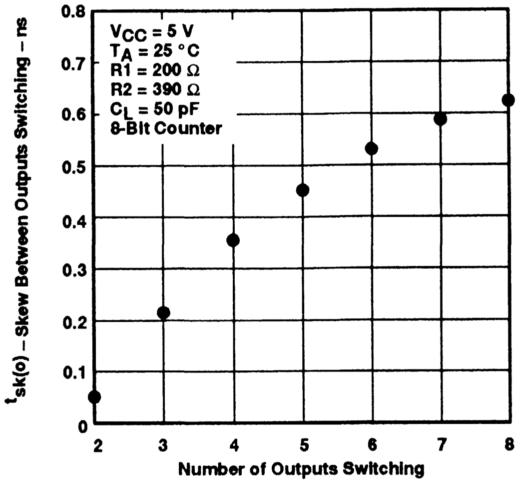


Figure 12

PROPAGATION DELAY TIME vs NUMBER OF OUTPUTS SWITCHING

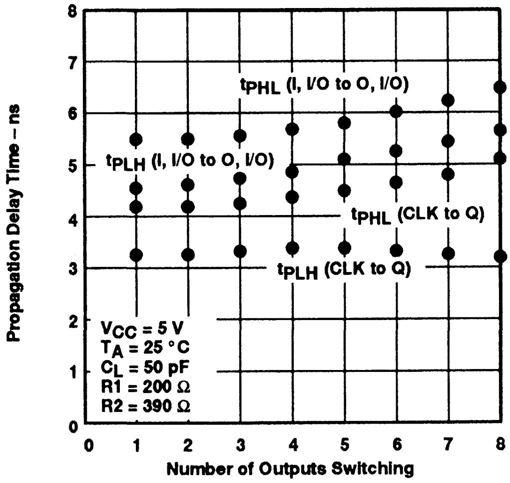


Figure 13

---

† Outputs switching in the same direction (t_{PLH} compared to t_{PLH}/t_{PHL} to t_{PHL})

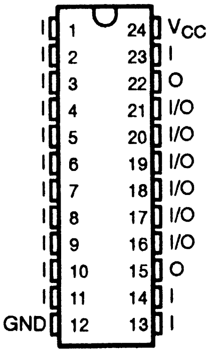
TIBPAL20L8-15C, TIBPAL20R4-15C, TIBPAL20R6-15C, TIBPAL20R8-15C
TIBPAL20L8-20M, TIBPAL20R4-20M, TIBPAL20R6-20M, TIBPAL20R8-20M
HIGH-PERFORMANCE *IMPACT*™ *PAL*® CIRCUITS

SRPS021 – D2920, JUNE 1986 – REVISED AUGUST 1989

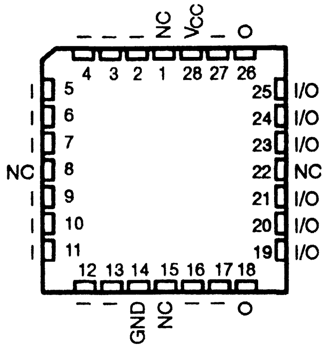
- **High-Performance: f_{max} (w/o feedback)**
  TIBPAL20R' -15C Series . . . 45 MHz
  TIBPAL20R' -20M Series . . . 41.6 MHz
- **High-Performance . . . 45 MHz Min**
- **Reduced I_{CC} of 180 mA Max**
- **Functionally Equivalent, but Faster Than PAL20L8, PAL20R4, PAL20R6, PAL20R8**
- **Power-Up Clear on Registered Devices (All Register Outputs are Set Low, but Voltage Levels at the Output Pins Go High)**
- **Preload Capability on Output Registers Simplifies Testing**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**

DEVICE	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
PAL20L8	14	2	0	6
PAL20R4	12	0	4 (3-state buffers)	4
PAL20R6	12	0	6 (3-state buffers)	2
PAL20R8	12	0	8 (3-state buffers)	0

TIBPAL20L8'
C SUFFIX . . . JT OR NT PACKAGE
M SUFFIX . . . JT OR W PACKAGE
(TOP VIEW)



TIBPAL20L8'
C SUFFIX . . . FN PACKAGE
M SUFFIX . . . FK PACKAGE
(TOP VIEW)



NC — No internal connection
Pin assignments in operating mode

description

These programmable array logic devices feature high speed and functional equivalency when compared with currently available devices. These IMPACT™ circuits combine the latest Advanced Low-Power Schottky technology with proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional TTL logic. Their easy programmability allows for quick design of custom functions and typically results in a more compact circuit board. In addition, chip carriers are available for futher reduction in board space.

Extra circuitry has been provided to allow loading of each register asynchronously to either a high or low state. This feature simplifies testing because the registers can be set to an initial state prior to executing the test sequence.

The TIBPAL20' C series is characterized from 0°C to 75°C. The TIBPAL20' M series is characterized for operation over the full military temperature range of –55°C to 125°C.

These devices are covered by U.S. Patent 4,410,987.
IMPACT is a trademark of Texas Instruments Incorporated.
PAL is a registered trademark of Advanced Micro Devices Inc.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

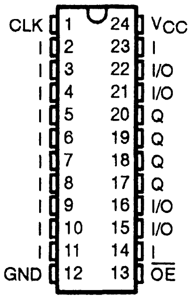
Copyright © 1989, Texas Instruments Incorporated

TIBPAL20R4-15C, TIBPAL20R6-15C, TIBPAL20R8-15C
TIBPAL20R4-20M, TIBPAL20R6-20M, TIBPAL20R8-20M
HIGH-PERFORMANCE *IMPACT*™ *PAL*® CIRCUITS

SRPS021 – D2920, JUNE 1986 – REVISED AUGUST 1989

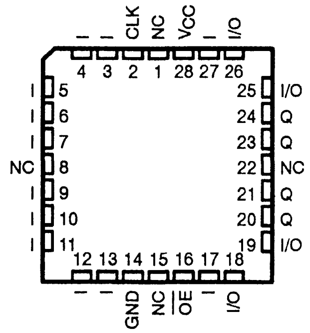
TIBPAL20R4'
C SUFFIX . . . JT OR NT PACKAGE
M SUFFIX . . . JT OR W PACKAGE

(TOP VIEW)



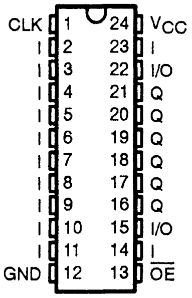
TIBPAL20R4'
C SUFFIX . . . FN PACKAGE
M SUFFIX . . . FK PACKAGE

(TOP VIEW)



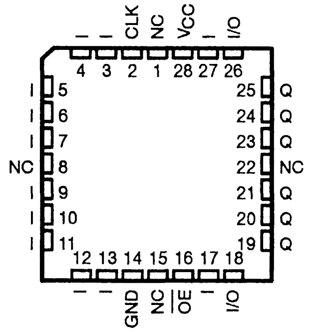
TIBPAL20R6'
C SUFFIX . . . JT OR NT PACKAGE
M SUFFIX . . . JT OR W PACKAGE

(TOP VIEW)



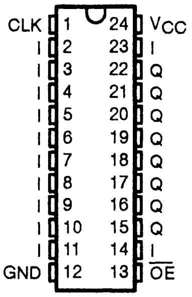
TIBPAL20R6'
C SUFFIX . . . FN PACKAGE
M SUFFIX . . . FK PACKAGE

(TOP VIEW)



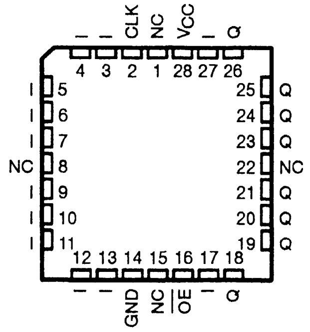
TIBPAL20R8'
C SUFFIX . . . JT OR NT PACKAGE
M SUFFIX . . . JT OR W PACKAGE

(TOP VIEW)



TIBPAL20R8'
C SUFFIX . . . FN PACKAGE
M SUFFIX . . . FK PACKAGE

(TOP VIEW)

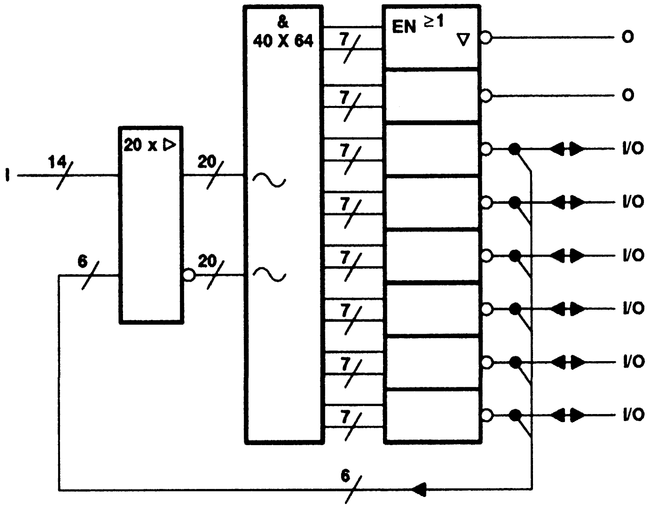


Pin assignments in operating mode

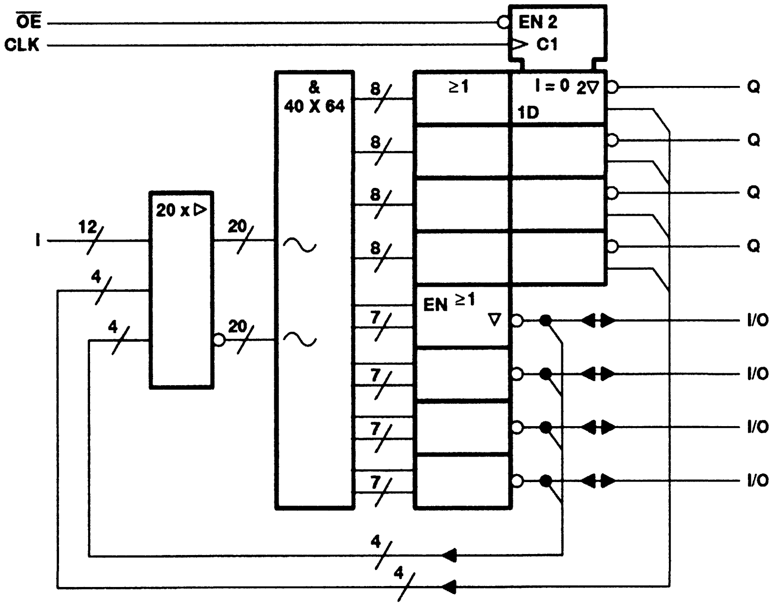
NC – No internal connection

functional block diagrams (positive logic)

TIBPAL20L8'



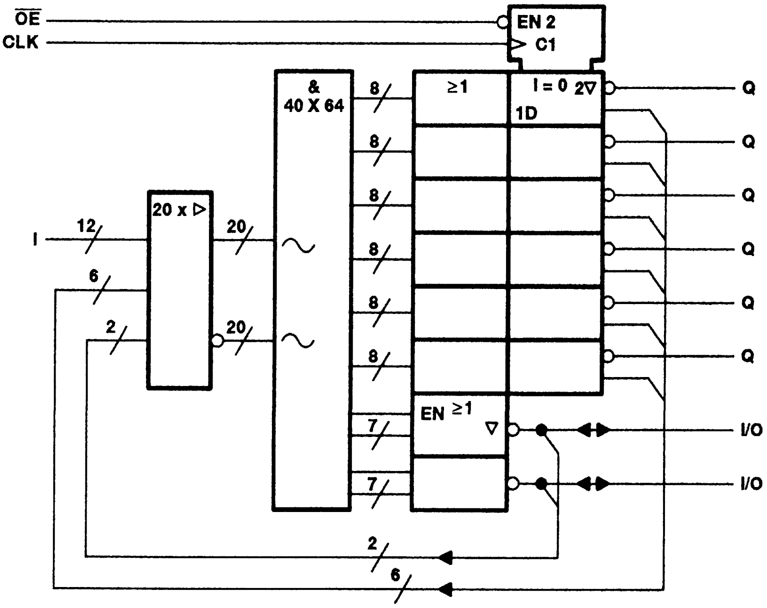
TIBPAL20R4'



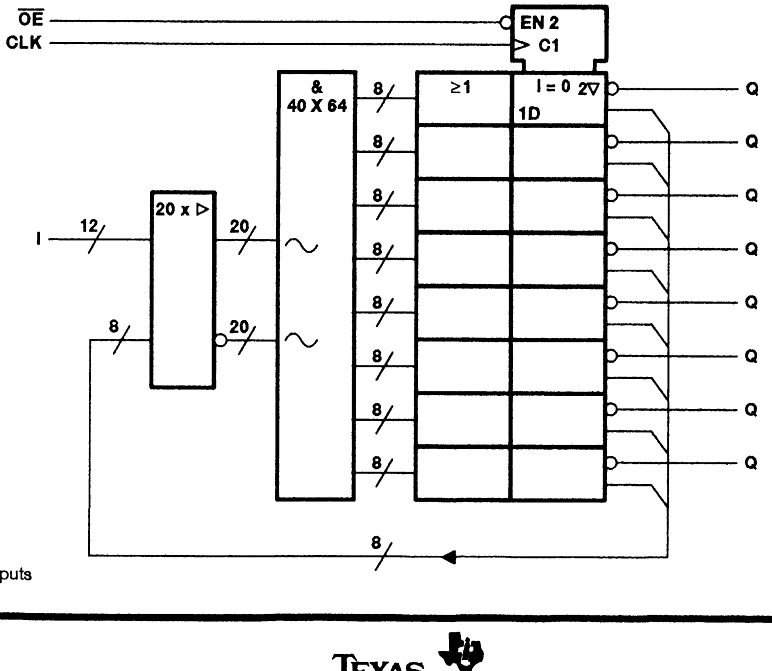
∿ denotes fused inputs

functional block diagrams (positive logic)

TIBPAL20R6'

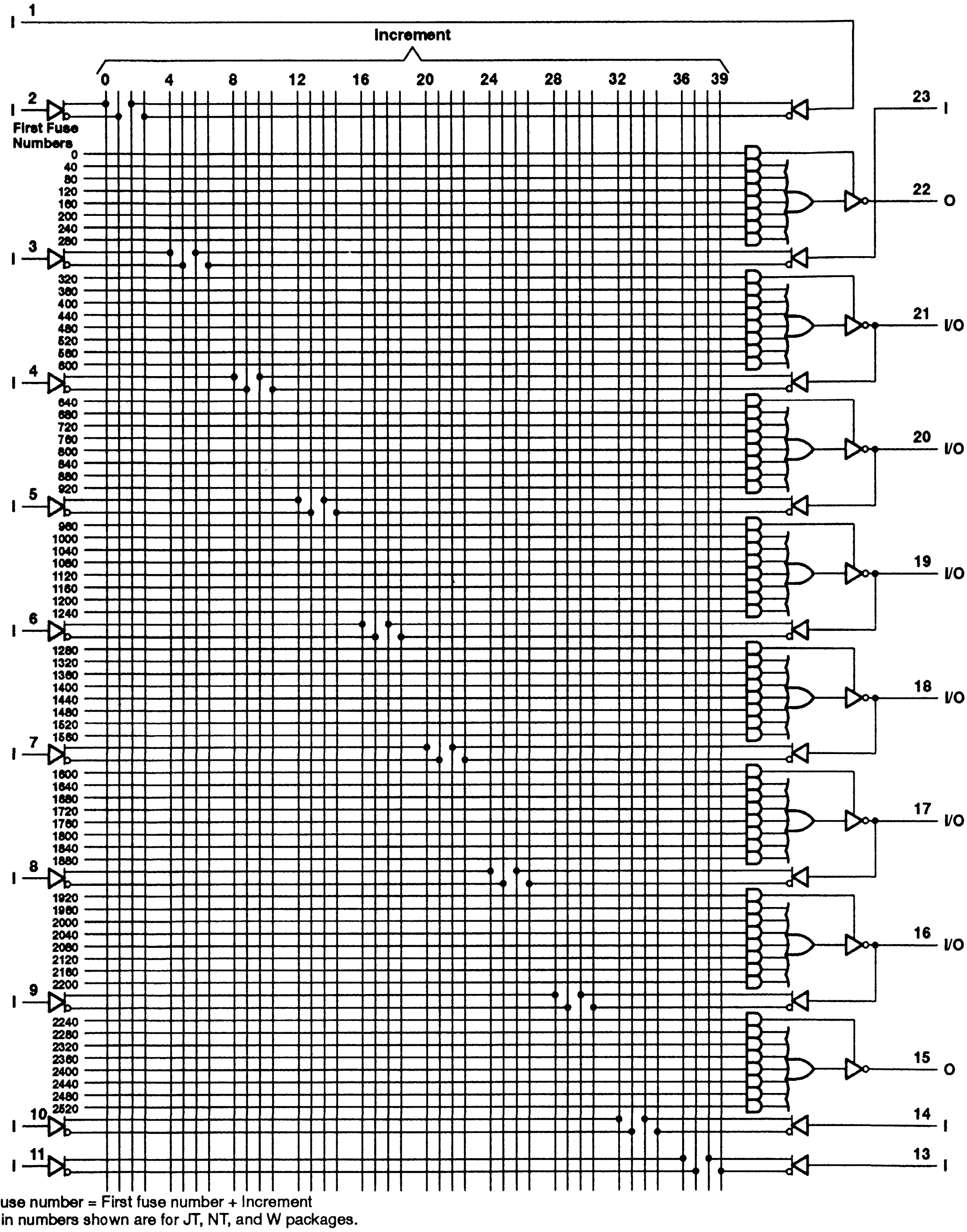


TIBPAL20R8'



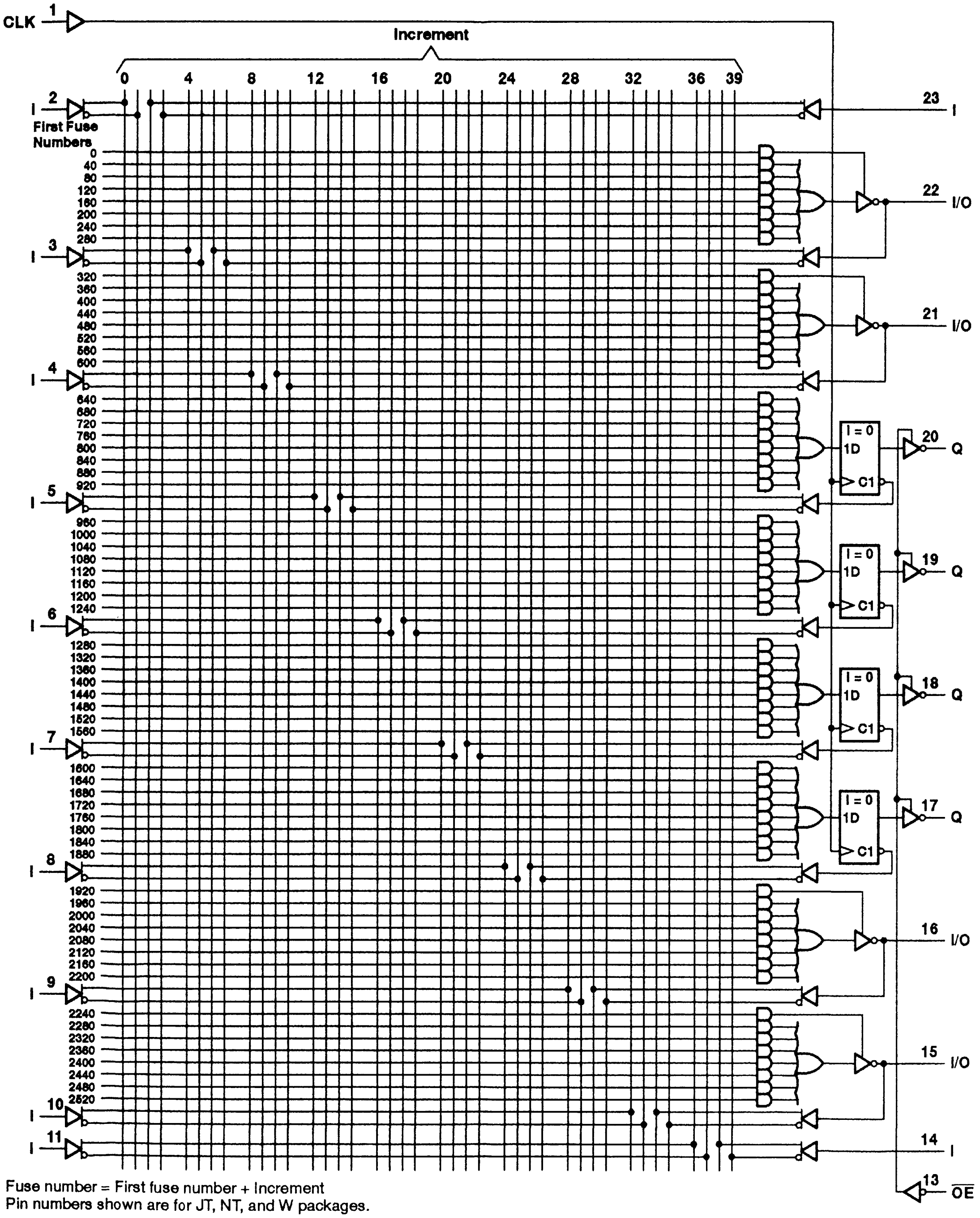
∿ denotes fused inputs

logic diagram (positive logic)



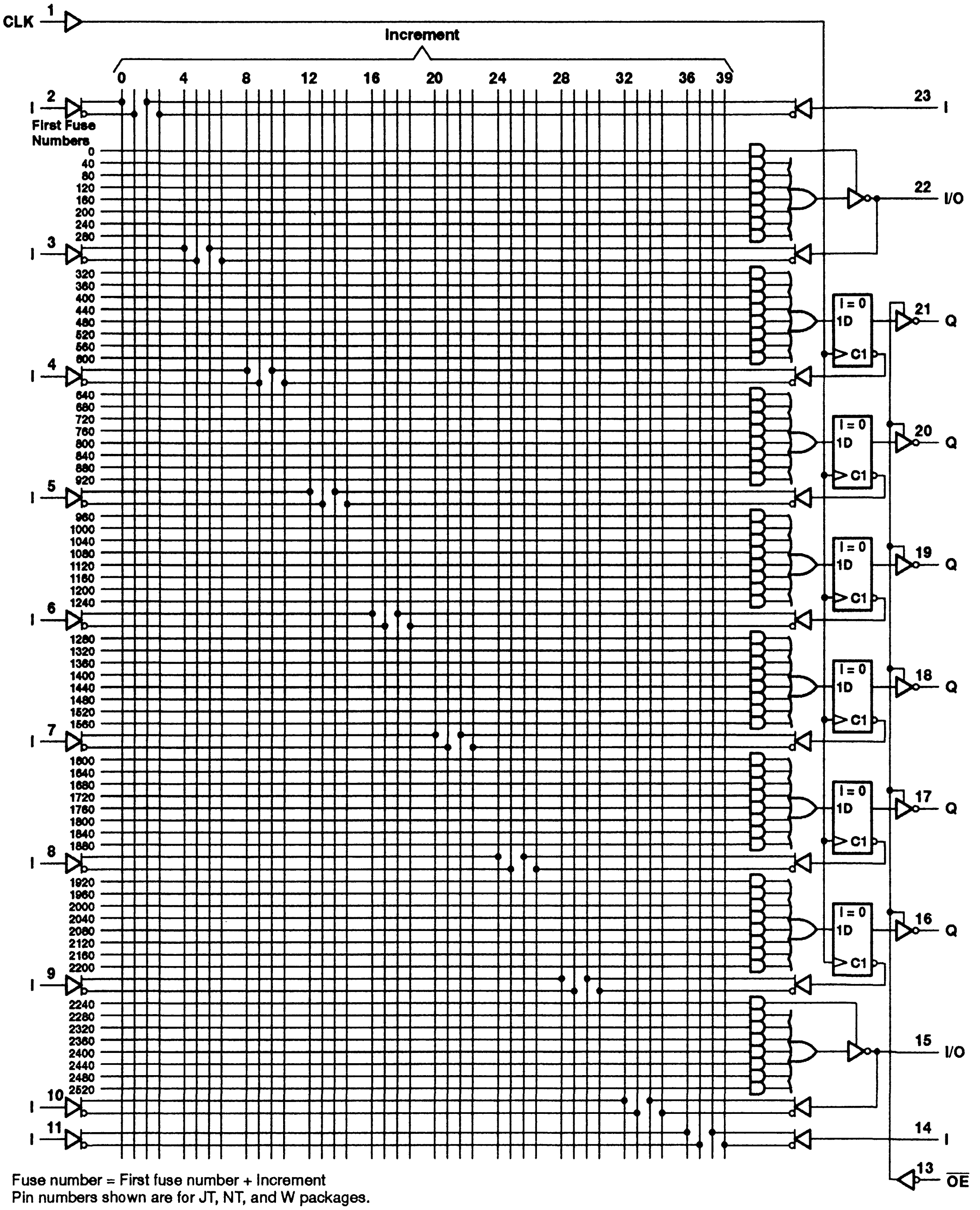
Fuse number = First fuse number + Increment
Pin numbers shown are for JT, NT, and W packages.

logic diagram (positive logic)



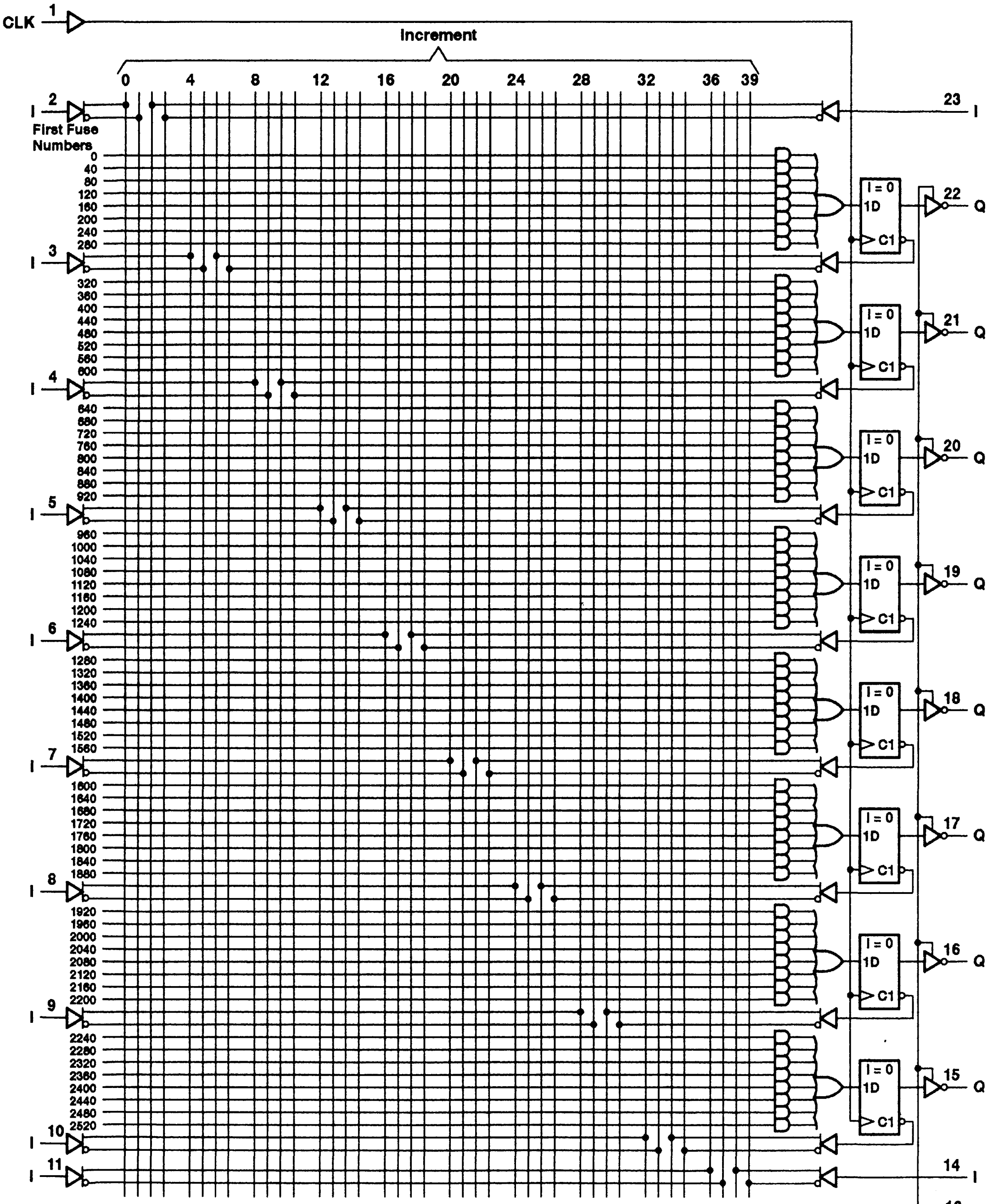
Fuse number = First fuse number + Increment
Pin numbers shown are for JT, NT, and W packages.

logic diagram (positive logic)



Fuse number = First fuse number + Increment
Pin numbers shown are for JT, NT, and W packages.

logic diagram (positive logic)



Fuse number = First fuse number + Increment
Pin numbers shown are for JT, NT, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (see Note 1)	5.5 V
Voltage applied to disabled output (see Note 1)	5.5 V
Operating free-air temperature range	0°C to 75°C
Storage temperature range	−65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−3.2	mA
I_{OL}	Low-level output current				24	mA
f_{clock}[†]	Clock frequency		0		45	MHz
t_w[†]	Pulse duration, clock	High	10			ns
		Low	12			
t_{su}[†]	Setup time, input or feedback before clock↑		15			ns
t_h[†]	Hold time, input or feedback after clock↑		0			ns
T_A	Operating free-air temperature		0	25	75	°C

[†] f_{clock}, t_w, t_{su}, and t_h do not apply for TIBPAL20L8'.

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.75 V,	I_I = –18 mA		–0.8	–1.5	V
V_{OH}		V_{CC} = 4.75 V,	I_{OH} = –3.2 mA	2.4			V
V_{OL}		V_{CC} = 4.75 V,	I_{OL} = 24 mA		0.3	0.5	V
I_{OZH}	O, Q outputs	V_{CC} = 5.25 V,	V_O = 2.7 V			20	µA
	I/O ports					100	
I_{OZL}	O, Q outputs	V_{CC} = 5.25 V,	V_O = 0.4 V			–20	µA
	I/O ports					–250	
I_I		V_{CC} = 5.25 V,	V_I = 5.5 V			0.1	mA
I_{IH}‡		V_{CC} = 5.25 V,	V_I = 2.7 V			25	µA
I_{IL}‡		V_{CC} = 5.25 V,	V_I = 0.4 V			–0.25	mA
I_{OS}§		V_{CC} = 5.25 V,	V_O = 0.5 V	–30	–70	–130	mA
I_{CC}		V_{CC} = 5.25 V, Outputs open,	V_I = 0, $\overline{OE}$ at V_{IH}		120	180	mA

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	TYP†	MAX	UNIT
f_{max}¶	With feedback		R1 = 200 Ω, R2 = 390 Ω, See Figure 3	37	40		MHz
	Without feedback			45	50		
t_{pd}	I, I/O	O, I/O			12	15	ns
t_{pd}	CLK↑	Q			8	12	ns
t_{en}	$\overline{OE}$	Q			10	15	ns
t_{dis}	$\overline{OE}$↑	Q			8	12	ns
t_{en}	I, I/O	O, I/O			12	18	ns
t_{dis}	I, I/O	O, I/O			12	15	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

¶ $f_{max}(\text{with feedback}) = \dfrac{1}{t_{su} + t_{pd}\ (\text{CLK to Q})}$, $f_{max}(\text{without feedback}) = \dfrac{1}{t_w\ \text{high} + t_w\ \text{low}}$,

f_{max} does not apply for TIBPAL20L8,.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (see Note 1)	5.5 V
Voltage applied to disabled output (see Note 1)	5.5 V
Operating free-air temperature range	−55°C to 125°C
Storage temperature range	−65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−2	mA
I_{OL}	Low-level output current				12	mA
f_{clock}[†]	Clock frequency		0		41.6	MHz
t_w[†]	Pulse duration, clock	High	12			ns
		Low	12			
t_{su}[†]	Setup time, input or feedback before clock↑		20			ns
t_h[†]	Hold time, input or feedback after clock↑		0			ns
T_A	Operating free-air temperature		−55	25	125	°C

[†] f_{clock}, t_w, t_{su}, and t_h do not apply for TIBPAL20L8'.

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA		−0.8	−1.5	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −2 mA	2.4	3.2		V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA		0.3	0.5	V
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V			100	µA
I_{OZL}‡	O, Q outputs	V_{CC} = 5.5 V,	V_O = 0.4 V			−20	µA
	I/O ports					−250	
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V			1	mA
I_{IH}‡	I/O ports	V_{CC} = 5.5 V,	V_I = 2.7 V			100	µA
	All others					25	
I_{IL}‡		V_{CC} = 5.5 V,	V_I = 0.4 V			−0.25	mA
I_{OS}§		V_{CC} = 5.5 V,	V_O = 0.5 V	−30	−70	−250	mA
I_{CC}		V_{CC} = 5.5 V, Outputs open,	V_I = 0, OE = V_{IH}		120	180	mA

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	TYP†	MAX	UNIT
f_{max}¶	With feedback		R1 = 390 Ω, R2 = 750 Ω, See Figure 3	28.5	40		MHz
	Without feedback			41.6	50		
t_{pd}	I, I/O	O, I/O			12	20	ns
t_{pd}	CLK↑	Q			8	15	ns
t_{en}	$\overline{OE}$	Q			10	20	ns
t_{dis}	$\overline{OE}$↑	Q			8	20	ns
t_{en}	I, I/O	O, I/O			12	25	ns
t_{dis}	I, I/O	O, I/O			12	20	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second. Set V_O at 0.5 V to avoid test equipment ground degradation.

¶ $f_{max}(\text{with feedback}) = \dfrac{1}{t_{su} + t_{pd}\ (\text{CLK to Q})}$, $f_{max}(\text{without feedback}) = \dfrac{1}{t_w\ \text{high} + t_w\ \text{low}}$,

f_{max} does not apply for TIBPAL20L8,.

programming information

Texas Instruments programmable logic devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments programmable logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

preload procedure for registered outputs (see Figure 1 and Notes 2 and 3)

The output registers can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below.

Step 1. With V_{CC} at 5 volts and Pin 1 at V_{IL}, raise Pin 13 to V_{IHH}.
Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.
Step 3. Pulse Pin 1, clocking in preload data.
Step 4. Remove output voltage, then lower Pin 13 to V_{IL}. Preload can be verified by observing the voltage level at the output pin.

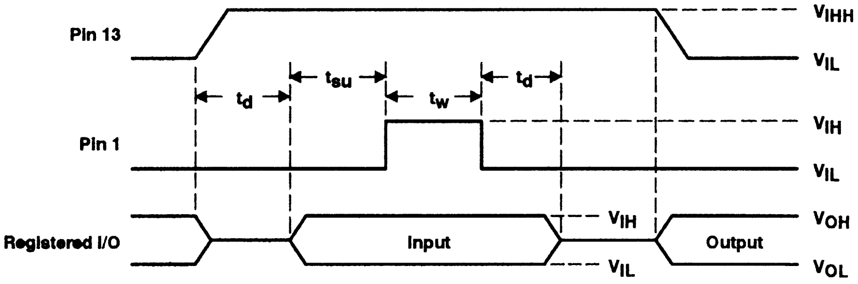
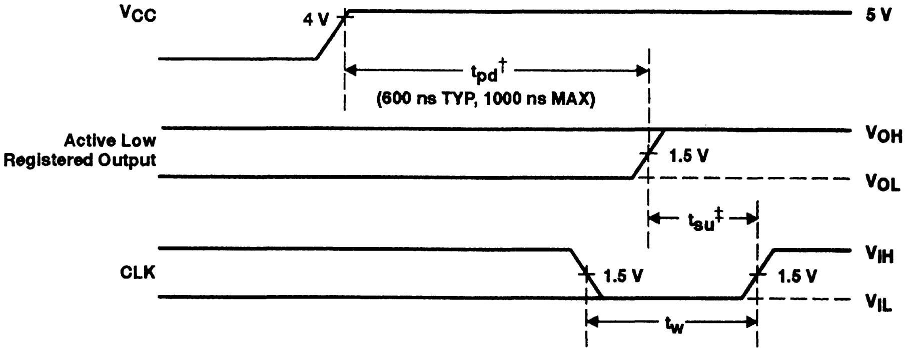


Figure 1. Preload Waveforms

NOTES: 2. Pin numbers shown are for JT, NT, and W packages only. If chip carrier socket adapter is not used, pin numbers must be changed accordingly.
3. $t_d = t_{su} = t_h$ = 100 ns to 1000 ns V_{IHH} = 10.25 V to 10.75 v

power-up reset (see Figure 2)

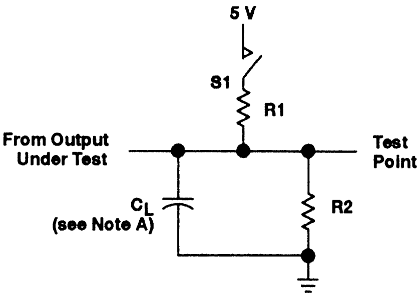
Following power up, all registers are reset to zero. This feature provides extra flexibility to the system designer and is especially valuable in simplifying state-machine initialization. To ensure a valid power-up reset, it is important that the rise of V_{CC} be monotonic. Following power-up reset, a low-to-high clock transition must not occur until all applicable input and feedback setup times are met.



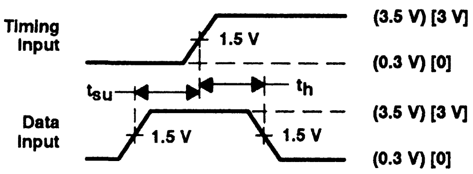
† This is the power-up reset time and applies to registered outputs only. The values shown are from characterization data.
‡ This is the setup time for input or feedback.

Figure 2. Power-Up Reset Waveforms

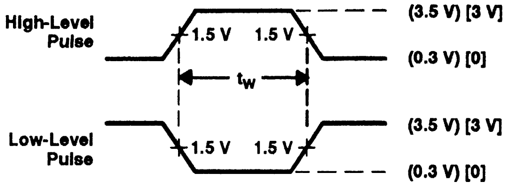
PARAMETER MEASUREMENT INFORMATION



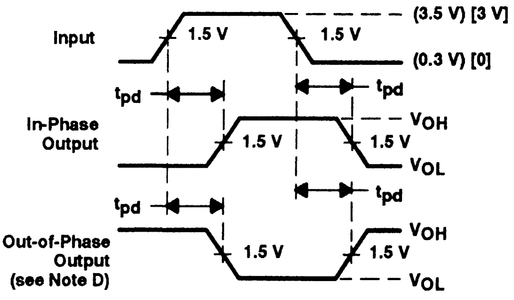
LOAD CIRCUIT FOR
3-STATE OUTPUTS



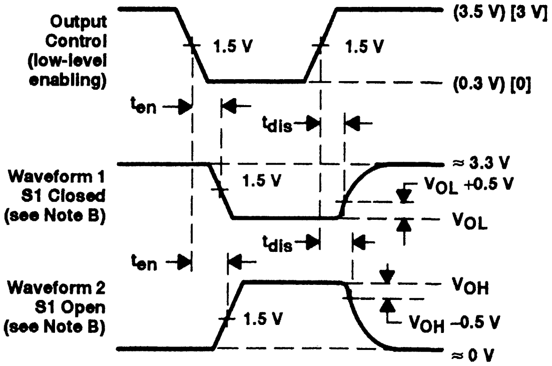
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES:
- A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses have the following characteristics: For C suffix, use the voltage levels indicated in parentheses ( ). PRR ≤ 1 MHz, $t_r = t_f \le 2$ ns, duty cycle = 50%. For M suffix, use the voltage levels indicated in brackets [ ]. PRR ≤ 10 MHz, t_r and $t_f \le 2$ ns, duty cycle = 50%.
- D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.
- E. Equivalent loads may be used for testing.

Figure 3. Load Circuit and Voltage Waveforms

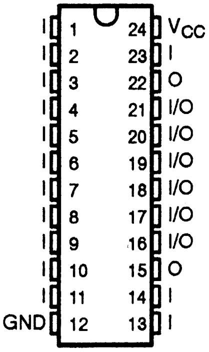
TIBPAL20L8-25C, TIBPAL20R4-25C, TIBPAL20R6-25C, TIBPAL20R8-25C
LOW-POWER HIGH-PERFORMANCE *IMPACT*™ *PAL*® CIRCUITS

SRPS022 – D2920, MAY 1987 – REVISED MARCH 1992

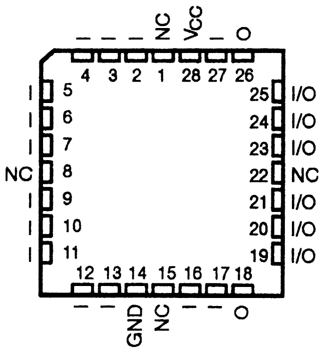
- **Low-Power, High-Performance**
  Reduced I_{CC} of 105 mA Max
  f_{max}:
  Without Feedback . . . 33 MHz Min
  With Feedback . . . 25 MHz Min
  t_{pd} . . . 25 ns Max
- **Direct Replacement for PAL20L8A, PAL20R4A, PAL20R6A, PAL20L8A, with at Least 50% Reduction in Power**
- **Preload Capability on Output Registers Simplifies Testing**
- **Power-Up Clear on Registered Devices (All Register Outputs are Set Low, but Voltage Levels at the Output Pins Go High)**
- **Package Options Include Plastic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Dependable Texas Instruments Quality and Reliability**

DEVICE	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
PAL20L8	14	2	0	6
PAL20R4	12	0	4 (3-state buffers)	4
PAL20R6	12	0	6 (3-state buffers)	2
PAL20R8	12	0	8 (3-state buffers)	0

TIBPAL20L8'
JT OR NT PACKAGE
(TOP VIEW)



TIBPAL20L8'
FN PACKAGE
(TOP VIEW)



NC – No internal connection
Pin assignments in operating mode

description

These programmable array logic devices feature high speed and functional equivalency when compared with currently available devices. These IMPACT™ circuits combine the latest AdvancedLow-Power Schottky technology with proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional TTL logic. Their easy programmability allows forquick design of custom functions and typically results in a more compact circuit board. In addition, chip carriers are available for futher reduction in board space.

All of the register outputs are set to a low level during power-up. Extra circuitry has been provided to allow loading of each register asynchronously to either a high or low state. This feature simplifies testing because the registers can be set to an initial state prior to executing the test sequence.

The TIBPAL20' C series is characterized from 0°C to 75°C.

These devices are covered by U.S. Patent 4,410,987
IMPACT is a trademark of Texas Instruments Incorporated.
PAL is a registered trademark of Advanced Micro Devices Inc.

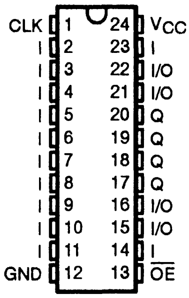
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 1992, Texas Instruments Incorporated

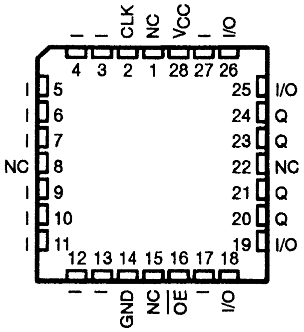
TIBPAL20R4-25C, TIBPAL20R6-25C, TIBPAL20R8-25C
LOW-POWER HIGH-PERFORMANCE *IMPACT*™ *PAL*® CIRCUITS

SRPS022 – D2920, MAY 1987 – REVISED MARCH 1992

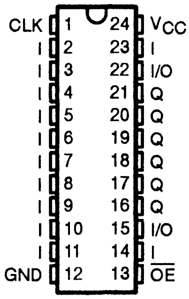
TIBPAL20R4'
JT OR NT PACKAGE
(TOP VIEW)



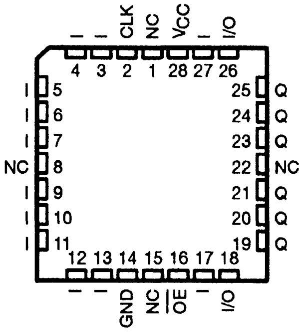
TIBPAL20R4'
FN PACKAGE
(TOP VIEW)



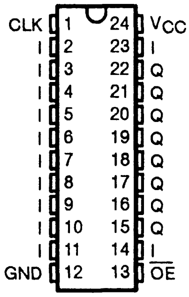
TIBPAL20R6'
JT OR NT PACKAGE
(TOP VIEW)



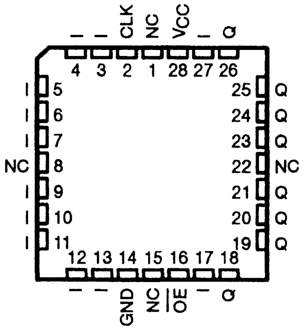
TIBPAL20R6'
FN PACKAGE
(TOP VIEW)



TIBPAL20R8'
JT OR NT PACKAGE
(TOP VIEW)



TIBPAL20R8'
FN PACKAGE
(TOP VIEW)

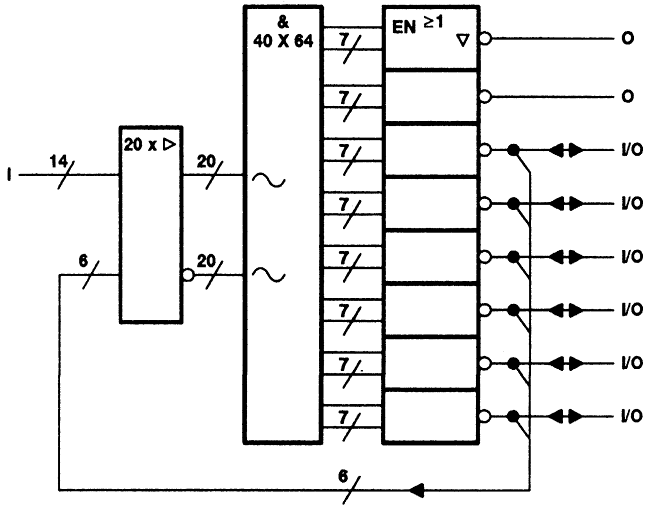


Pin assignments in operating mode

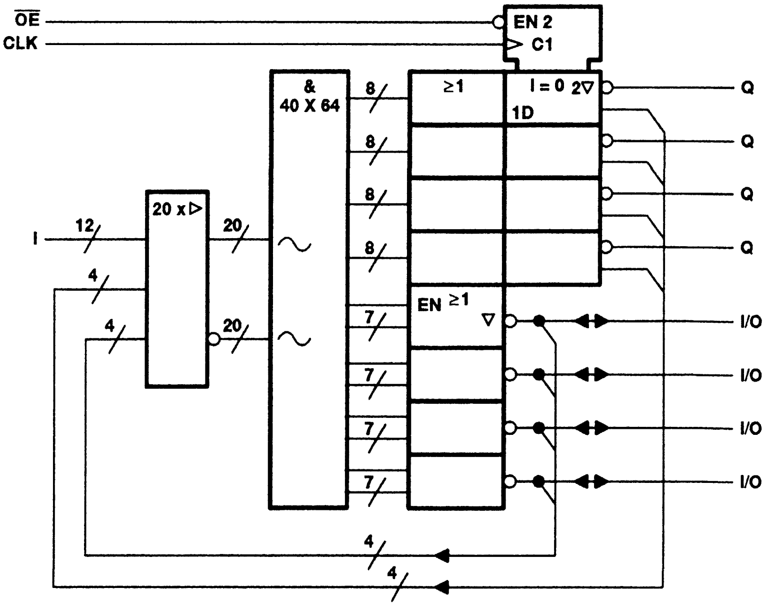
NC – No internal connection

functional block diagrams (positive logic)

TIBPAL20L8'



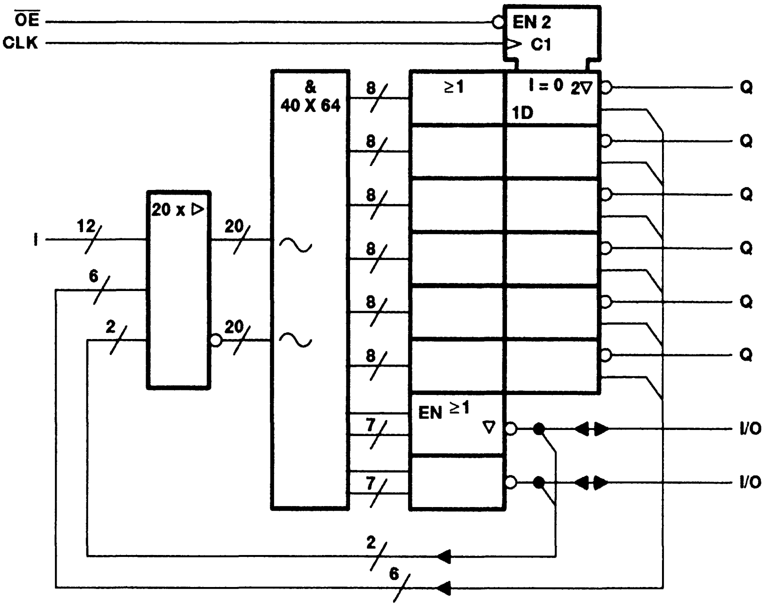
TIBPAL20R4'



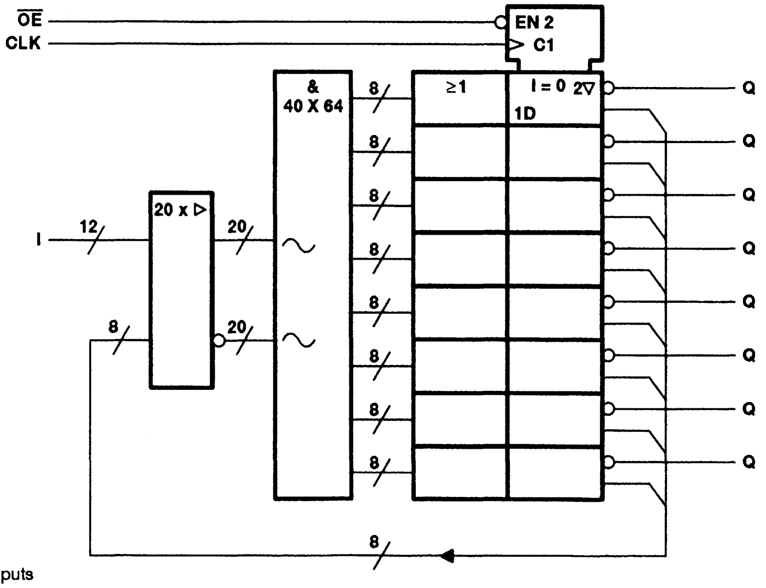
∿ denotes fused inputs

functional block diagrams (positive logic)

TIBPAL20R6'

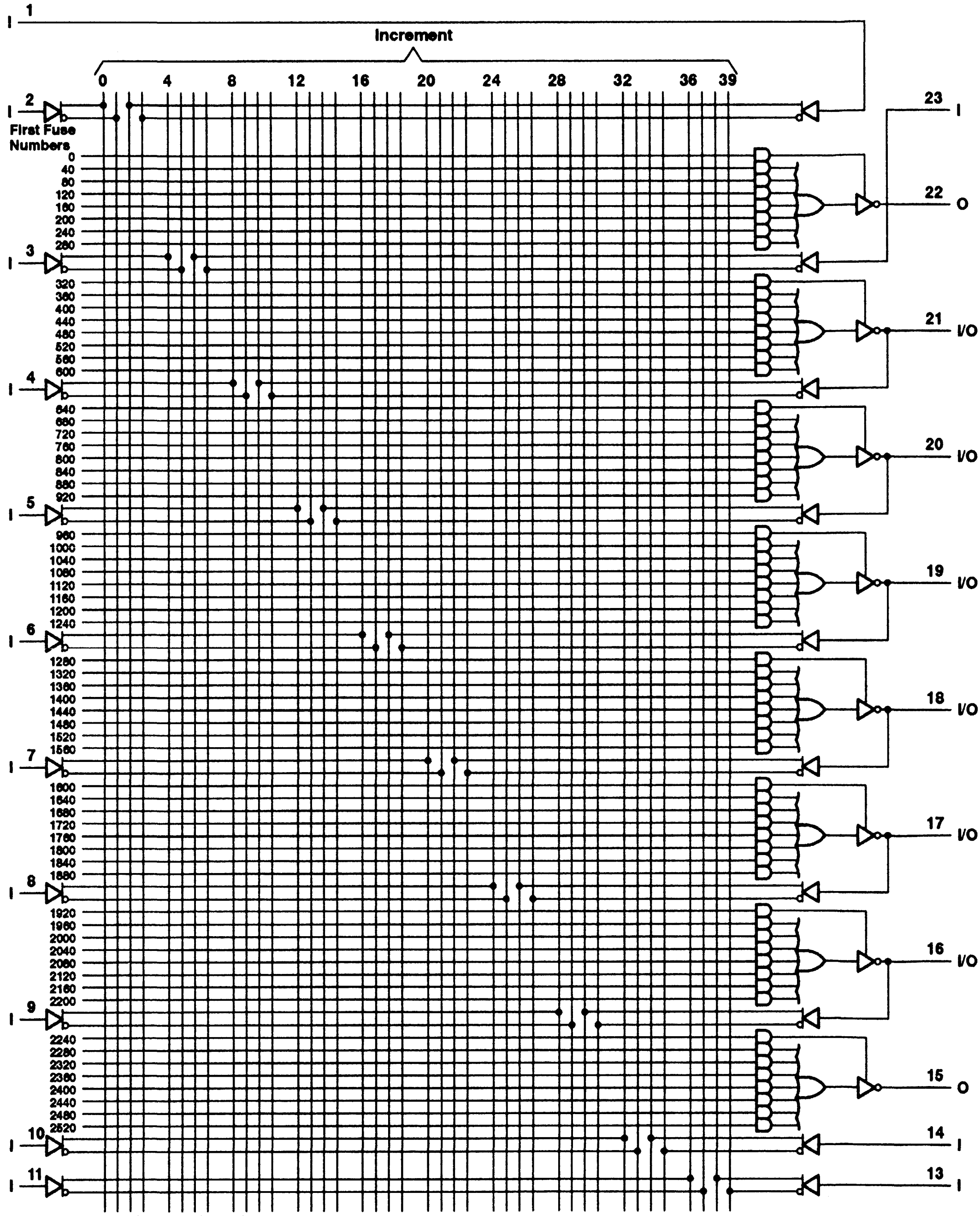


TIBPAL20R8'



∿ denotes fused inputs

logic diagram (positive logic)

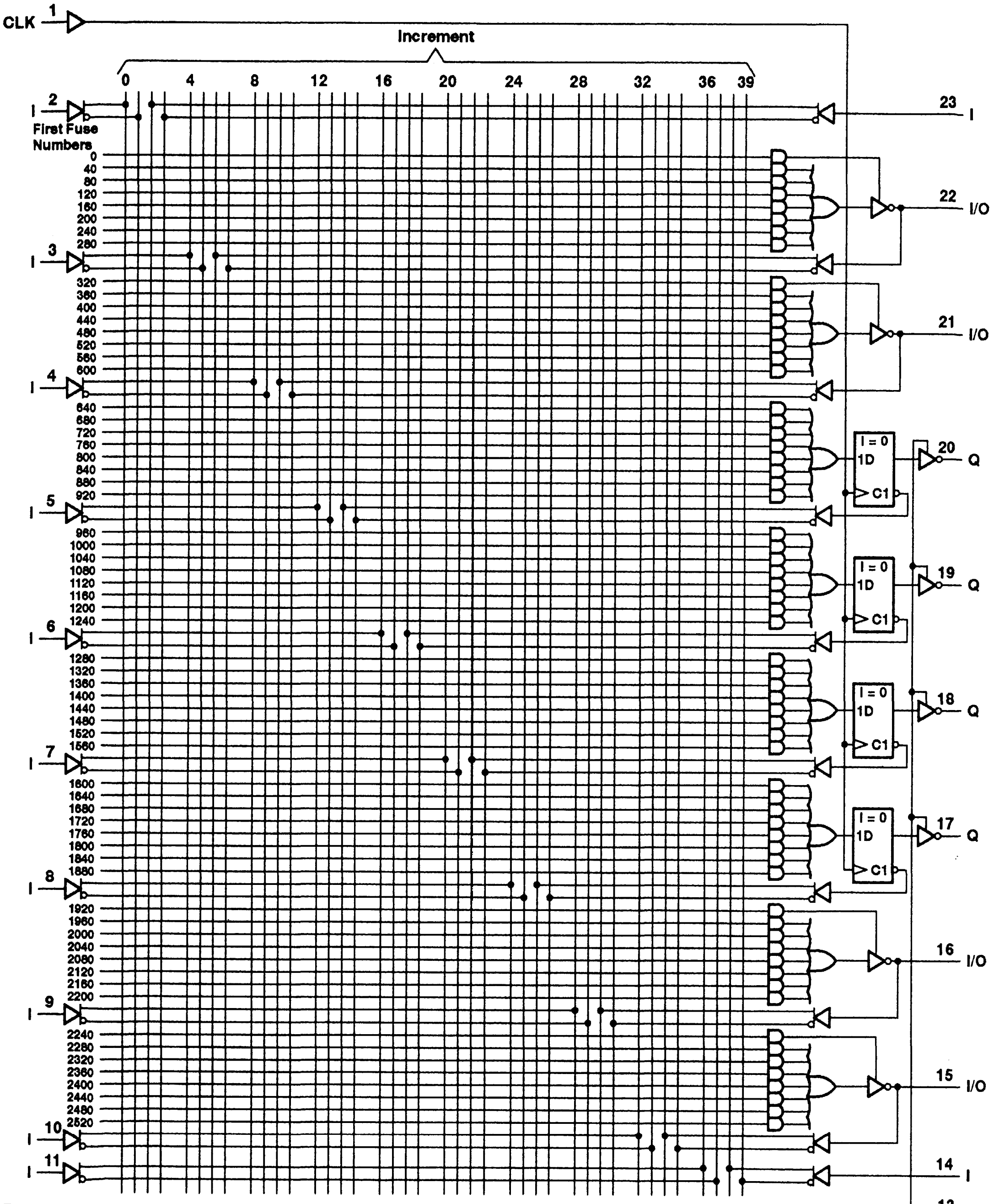


Fuse number = First fuse number + Increment
Pin numbers shown are for JT and NT packages.

TIBPAL20R4-25C
LOW-POWER HIGH-PERFORMANCE *IMPACT*™ *PAL*® CIRCUITS

SRPS022 – D2920, MAY 1987 – REVISED MARCH 1992

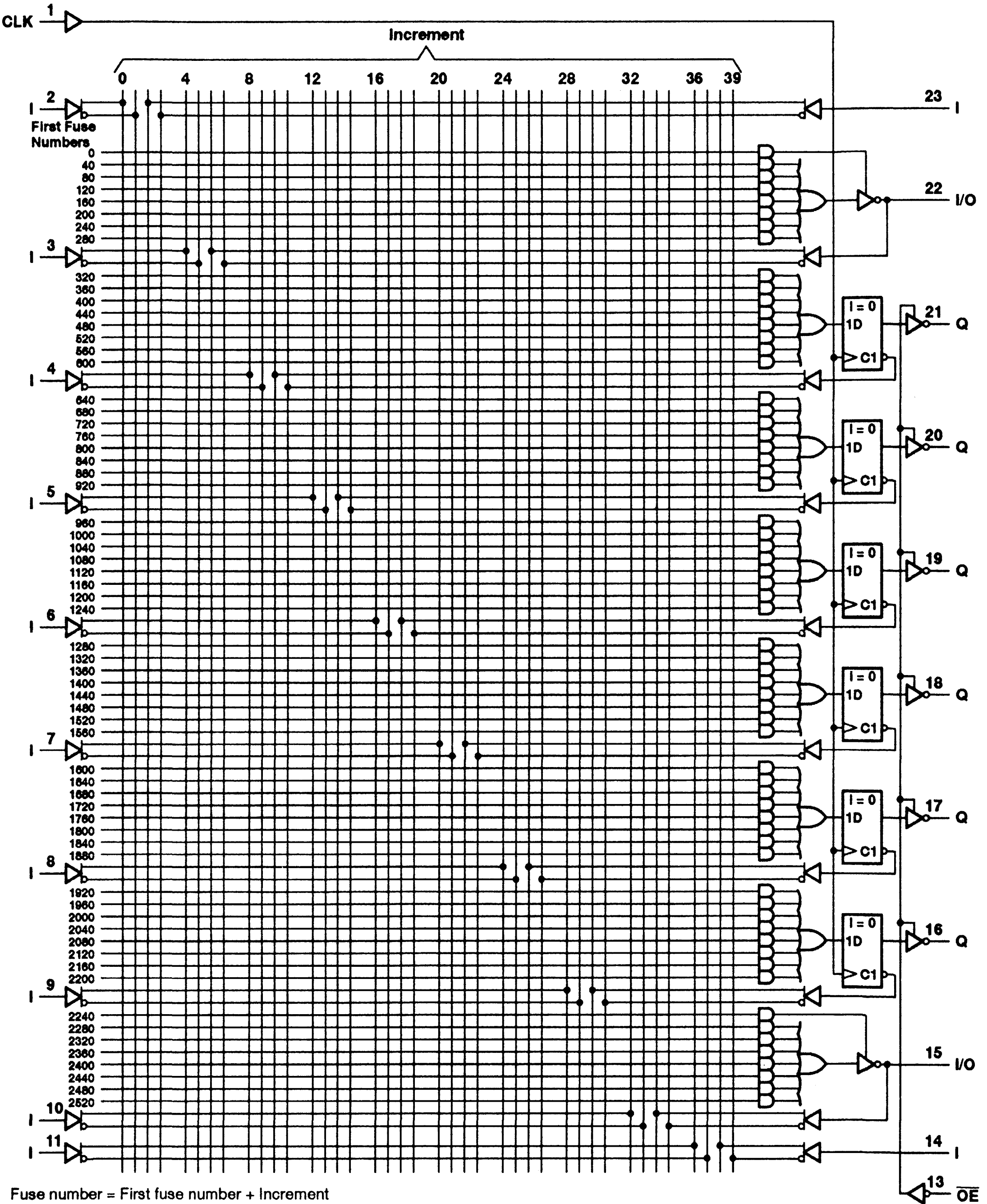
logic diagram (positive logic)



Fuse number = First fuse number + Increment

Pin numbers shown are for JT and NT packages.

logic diagram (positive logic)

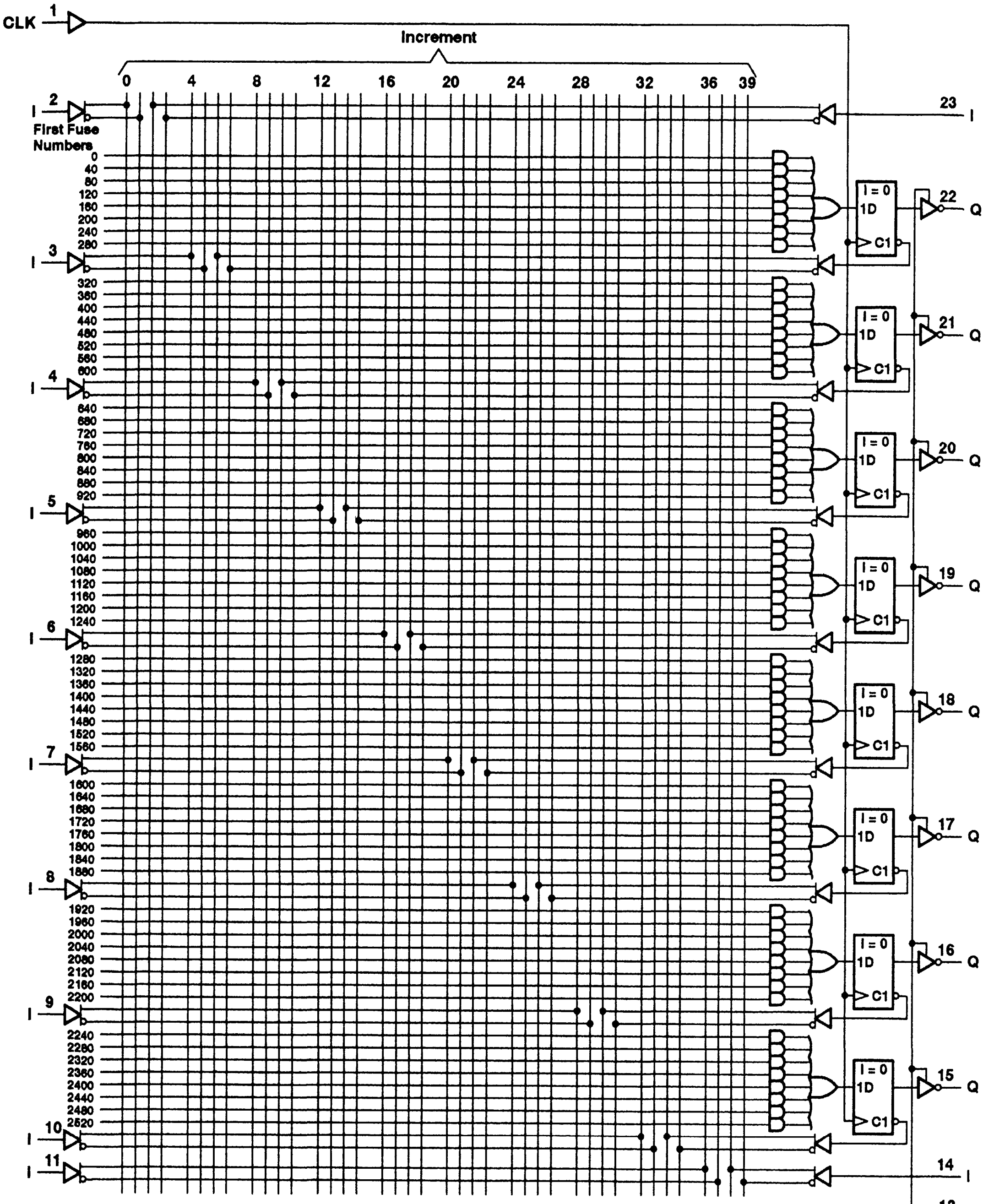


Fuse number = First fuse number + Increment
Pin numbers shown are for JT and NT packages.

TIBPAL20R8-25C
LOW-POWER HIGH-PERFORMANCE *IMPACT*™ *PAL*® CIRCUITS

SRPS022 – D2920, MAY 1987 – REVISED MARCH 1992

logic diagram (positive logic)



Fuse number = First fuse number + Increment
Pin numbers shown are for JT and NT packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (see Note 1)	5.5 V
Voltage applied to disabled output (see Note 1)	5.5 V
Operating free-air temperature range	0°C to 75°C
Storage temperature range	–65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				–3.2	mA
I_{OL}	Low-level output current				24	mA
f_{clock}†	Clock frequency		0		33	MHz
t_w†	Pulse duration, clock	High	15			ns
		Low	15			
t_{su}†	Setup time, input or feedback before clock↑		25			ns
t_h†	Hold time, input or feedback after clock↑		0			ns
T_A	Operating free-air temperature		0	25	75	°C

† f_{clock}, t_w, t_{su}, and t_h do not apply for TIBPAL20L8'.

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		$V_{CC} = 4.75$ V,	$I_I = -18$ mA		−0.8	−1.5	V
V_{OH}		$V_{CC} = 4.75$ V,	$I_{OH} = -3.2$ mA	2.4	3.3		V
V_{OL}		$V_{CC} = 4.75$ V,	$I_{OL} = 24$ mA		0.3	0.5	V
I_{OZH}	O, Q outputs	$V_{CC} = 5.25$ V,	$V_O = 2.7$ V			20	μA
	I/O ports					100	
I_{OZL}	O, Q outputs	$V_{CC} = 5.25$ V,	$V_O = 0.4$ V			−20	μA
	I/O ports					−250	
I_I		$V_{CC} = 5.25$ V,	$V_I = 5.5$ V			0.1	mA
I_{IH}‡		$V_{CC} = 5.25$ V,	$V_I = 2.7$ V			20	μA
I_{IL}‡		$V_{CC} = 5.25$ V,	$V_I = 0.4$ V			−0.25	mA
I_{OS}§		$V_{CC} = 5.25$ V,	$V_O = 0$	−30	−70	−130	mA
I_{CC}		$V_{CC} = 5.25$ V, Outputs open,	$V_I = 0$, $\overline{OE}$ at V_{IH}		75	105	mA

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	TYP†	MAX	UNIT
f_{max}¶	With feedback			25	40		MHz
	Without feedback			33	50		
t_{pd}	I, I/O	O, I/O	R1 = 200 Ω, R2 = 390 Ω, See Figure 3	3	14	25	ns
t_{pd}	CLK↑	Q		2	10	15	ns
t_{en}	$\overline{OE}$	Q		2	8	15	ns
t_{dis}	$\overline{OE}$↑	Q		2	8	15	ns
t_{en}	I, I/O	O, I/O		3	15	25	ns
t_{dis}	I, I/O	O, I/O		3	15	25	ns

† All typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

¶ $f_{max}(\text{with feedback}) = \dfrac{1}{t_{su} + t_{pd}\ (\text{CLK to Q})}$, $f_{max}(\text{without feedback}) = \dfrac{1}{t_w\ \text{high} + t_w\ \text{low}}$,

f_{max} does not apply for TIBPAL20L8,.

programming information

Texas Instruments programmable logic devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments programmable logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

preload procedure for registered outputs (see Figure 1 and Notes 2 and 3)

The output registers can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below.

Step 1. With V_{CC} at 5 volts and Pin 1 at V_{IL}, raise Pin 13 to V_{IHH}.
Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.
Step 3. Pulse Pin 1, clocking in preload data.
Step 4. Remove output voltage, then lower Pin 13 to V_{IL}. Preload can be verified by observing the voltage level at the output pin.

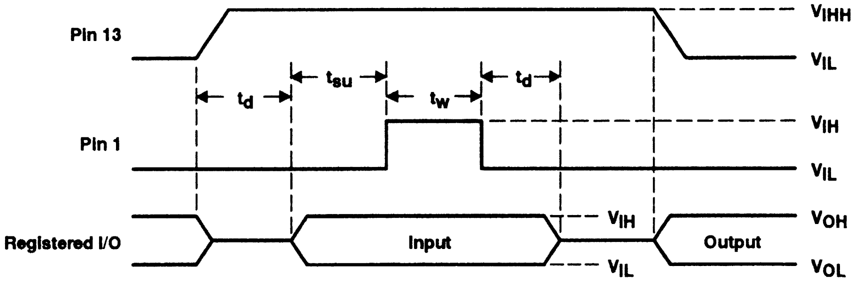
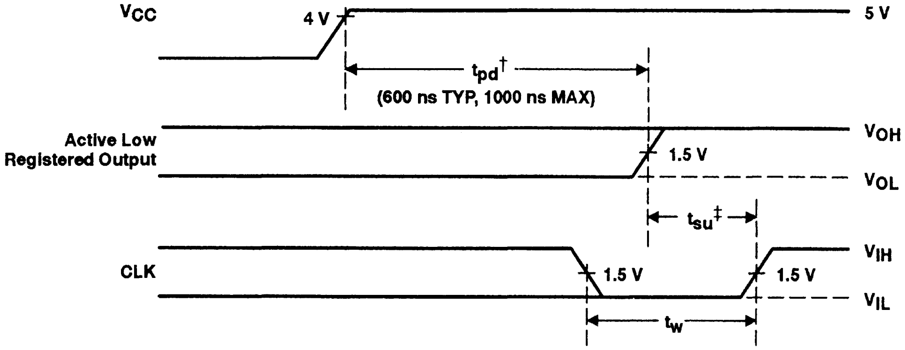


Figure 1. Preload Waveforms

NOTES: 2. Pin numbers shown are for JT and NT packages only. If chip carrier socket adapter is not used, pin numbers must be changed accordingly.
3. $t_d = t_{su} = t_h$ = 100 ns to 1000 ns V_{IHH} = 10.25 V to 10.75 v

power-up reset (see Figure 2)

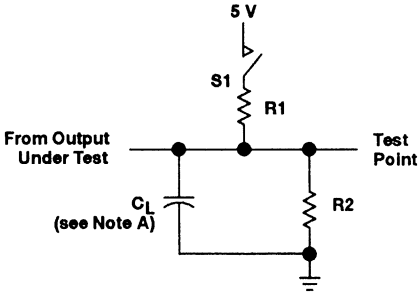
Following power up, all registers are reset to zero. This feature provides extra flexibility to the system designer and is especially valuable in simplifying state-machine initialization. To ensure a valid power-up reset, it is important that the rise of V_{CC} be monotonic. Following power-up reset, a low-to-high clock transition must not occur until all applicable input and feedback setup times are met.



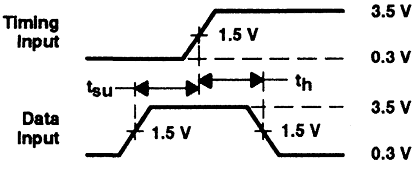
† This is the power-up reset time and applies to registered outputs only. The values shown are from characterization data.
‡ This is the setup time for input or feedback.

Figure 2. Power-Up Reset Waveforms

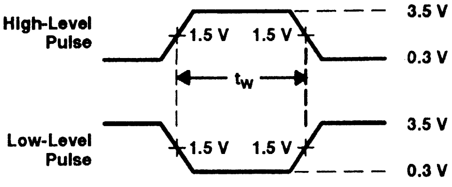
PARAMETER MEASUREMENT INFORMATION



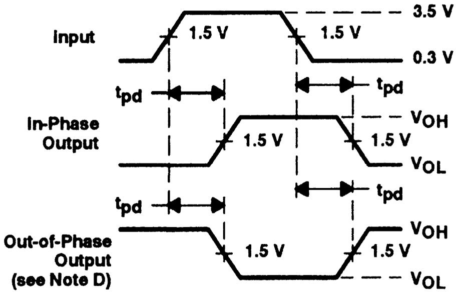
LOAD CIRCUIT FOR 3-STATE OUTPUTS



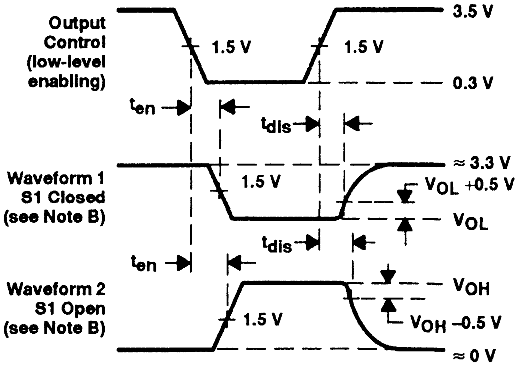
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATIONS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 1 MHz, t_r and $t_f \leq 2$ ns, duty cycle = 50%.
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.
E. Equivalent loads may be used for testing.

Figure 3. Load Circuit and Voltage Waveforms

TIBPAL20L8-15CNL, TIBPAL20R4-15CNL, TIBPAL20R6-15CNL, TIBPAL20R8-15CNL
TIBPAL20L8-25CNL, TIBPAL20R4-25CNL, TIBPAL20R6-25CNL, TIBPAL20R8-25CNL
HIGH-PERFORMANCE *IMPACT*™ *PAL*® CIRCUITS

SRPS023 – D3095, JANUARY 1988 – REVISED AUGUST 1989

- **High-Performance: f_{max} (w/o feedback)**
  TIBPAL20R' -15CNL Series . . . 45 MHz
  TIBPAL20R' -25CNL Series . . . 33 MHz
- **-15CNL Devices are Direct Replacements for PAL20L8BCNL, PAL20R4BCNL, PAL20R6BCNL, and PAL20R8BCNL**
- **-25CNL Devices are Direct Replacements for PAL20L8B-2CNL, PAL20R4B-2CNL, PAL20R6B-2CNL, and PAL20R8B-2CNL**
- **Power-Up Clear on Registered Devices (All Register Outputs are Set Low, but Voltage Levels at the Output Pins Go High)**
- **Preload Capability on Output Registers Simplifies Testing**

DEVICE	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
PAL20L8	14	2	0	6
PAL20R4	12	0	4 (3-state buffers)	4
PAL20R6	12	0	6 (3-state buffers)	2
PAL20R8	12	0	8 (3-state buffers)	0

ordering information

Devices with the AMD chip-carrier pin-out shown here may be ordered by using the indicated part number with the NL suffix. Do not include the package suffix (FN).

description

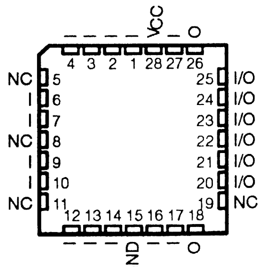
These programmable array logic devices feature high speed and functional equivalency when compared with currently available devices. These IMPACT™ circuits combine the latest Advanced Low-Power Schottky technology with proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional TTL logic. Their easy programmability allows for quick design of custom functions and typically results in a more compact circuit board. In addition, chip carriers are available for futher reduction in board space.

Extra circuitry has been provided to allow loading of each register asynchronously to either a high or low state. This feature simplifies testing because the registers can be set to an initial state prior to executing the test sequence.

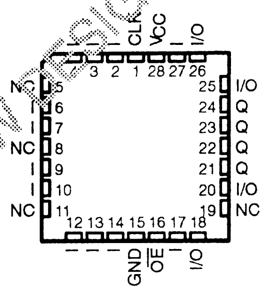
The TIBPAL20' C series is characterized from 0°C to 75°C.

NOT RECOMMENDED FOR NEW DESIGNS

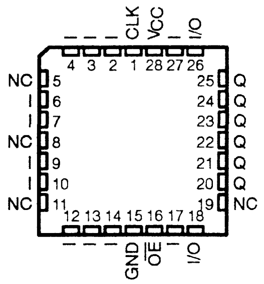
TIBPAL20L8' . . . FN PACKAGE
(TOP VIEW)



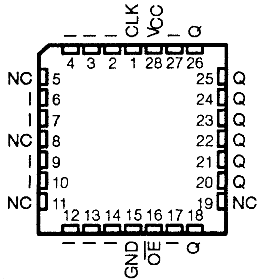
TIBPAL20R4' . . . FN PACKAGE
(TOP VIEW)



TIBPAL20R6' . . . FN PACKAGE
(TOP VIEW)



TIBPAL20R8' . . . FN PACKAGE
(TOP VIEW)



NC — No internal connection

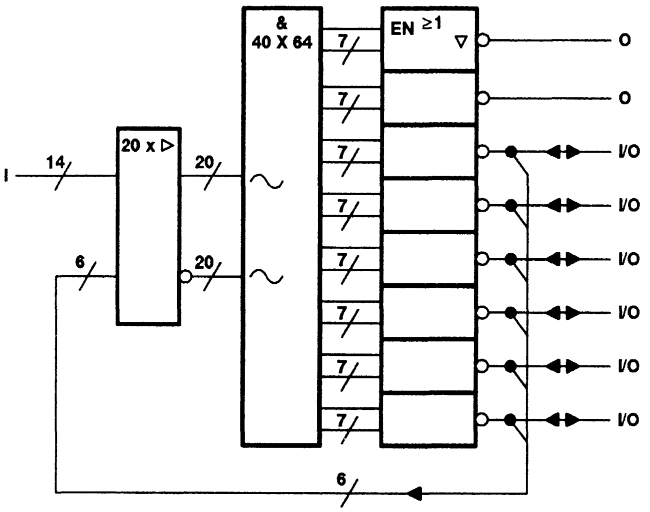
These devices are covered by U.S. Patent 4,410,987.
IMPACT is a trademark of Texas Instruments Incorporated.
PAL is a registered trademark of Advanced Micro Devices Inc.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

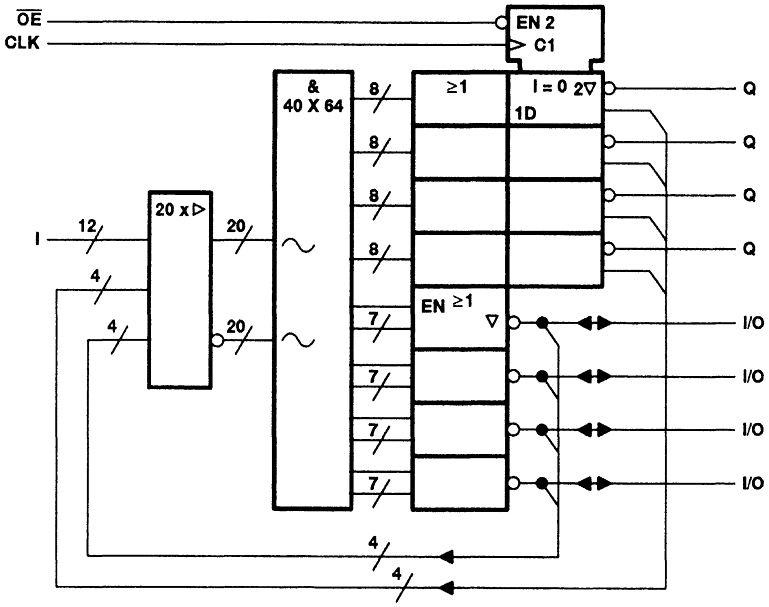
Copyright © 1989, Texas Instruments Incorporated

functional block diagrams (positive logic)

TIBPAL20L8'



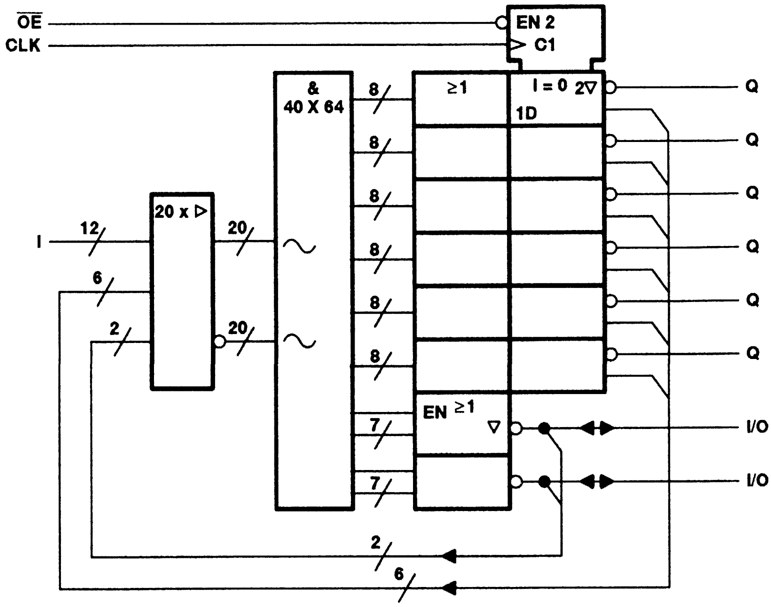
TIBPAL20R4'



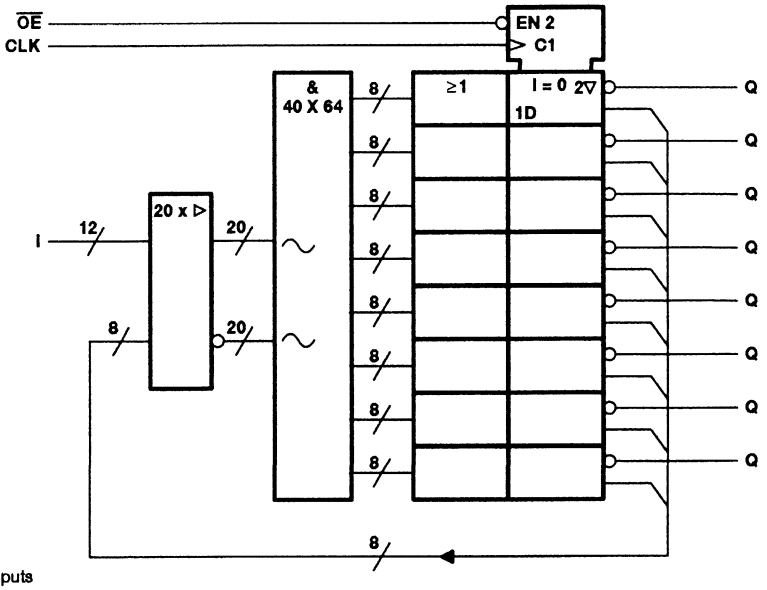
∿ denotes fused inputs

functional block diagrams (positive logic)

TIBPAL20R6'

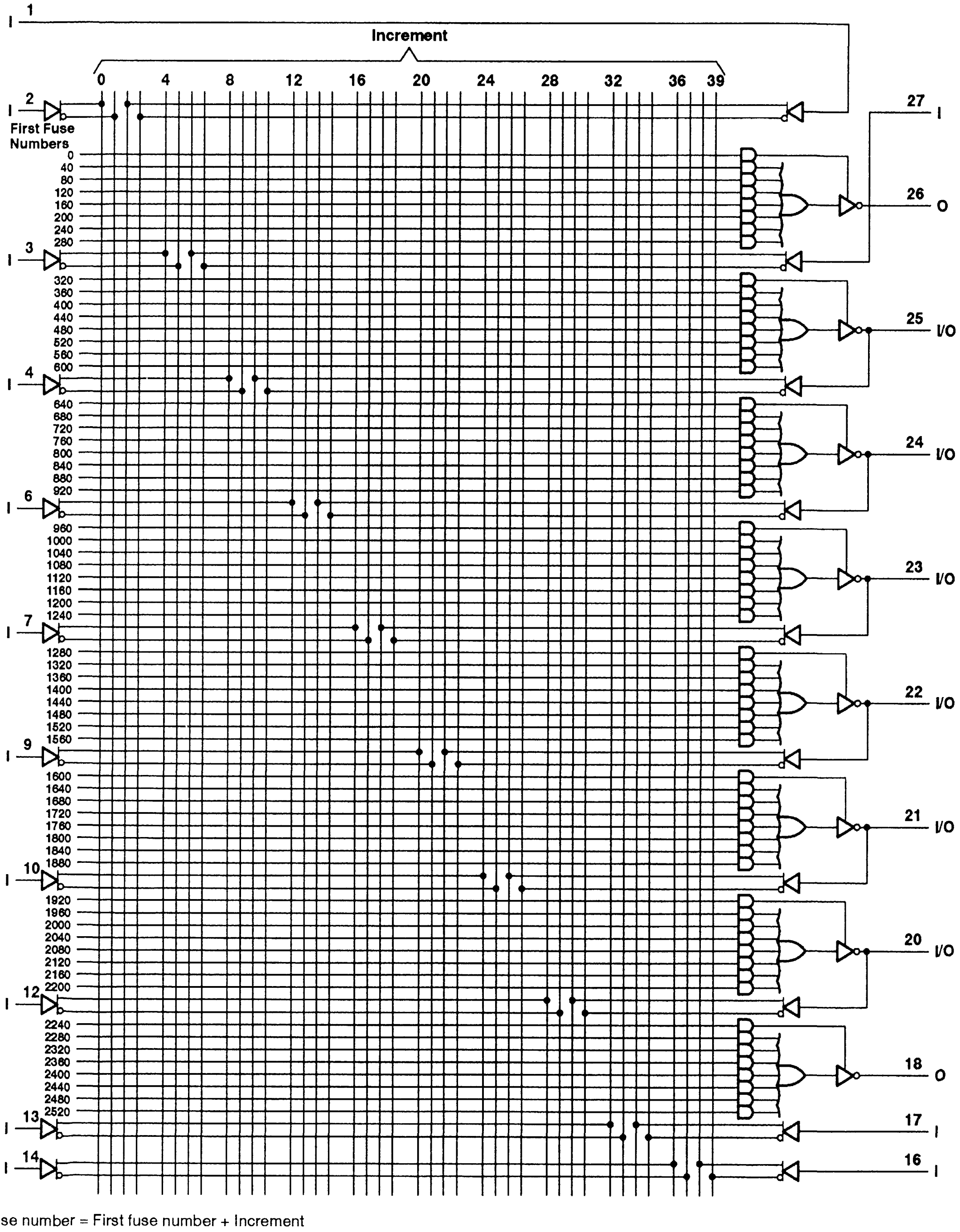


TIBPAL20R8'



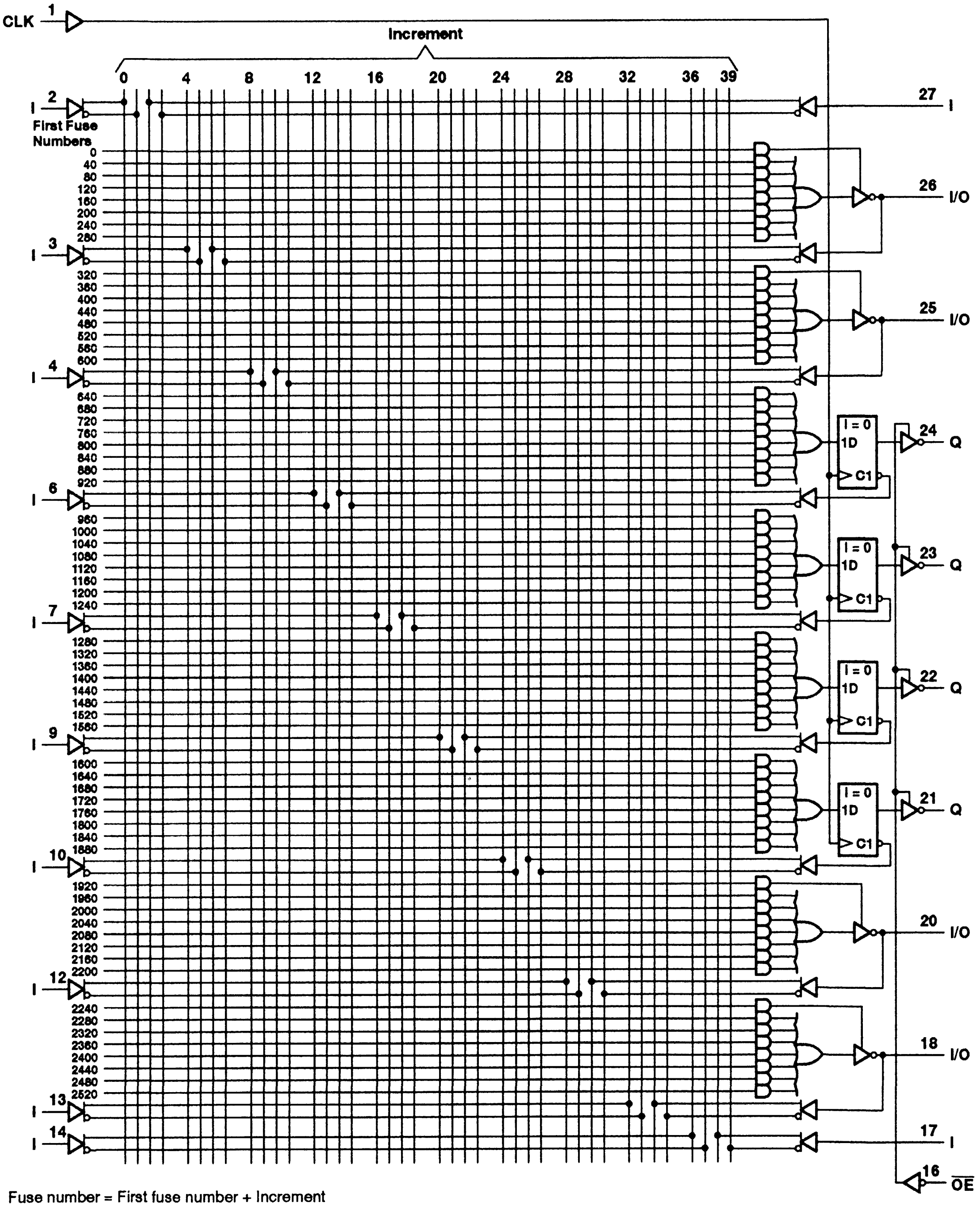
∿ denotes fused inputs

logic diagram (positive logic)



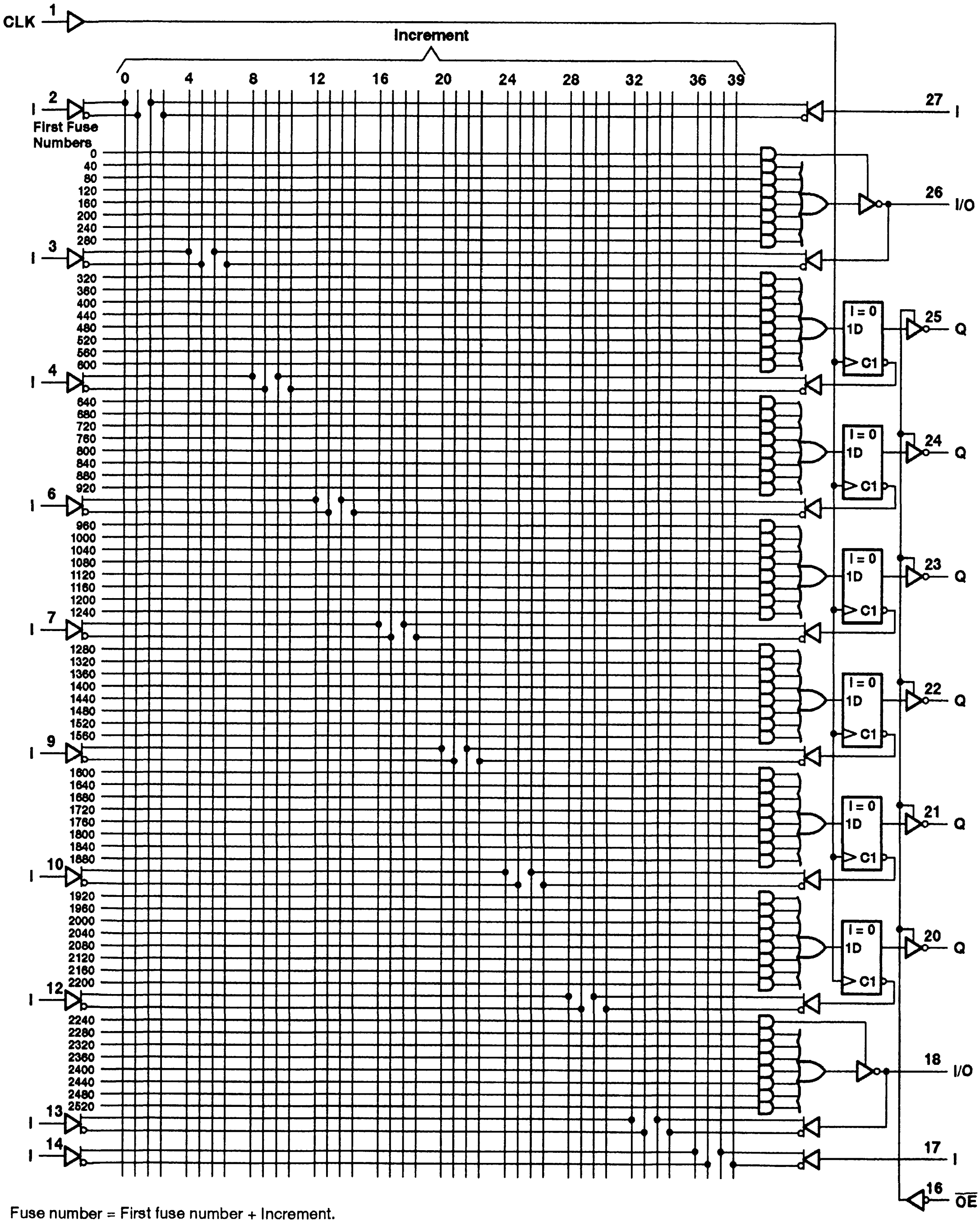
Fuse number = First fuse number + Increment

logic diagram (positive logic)



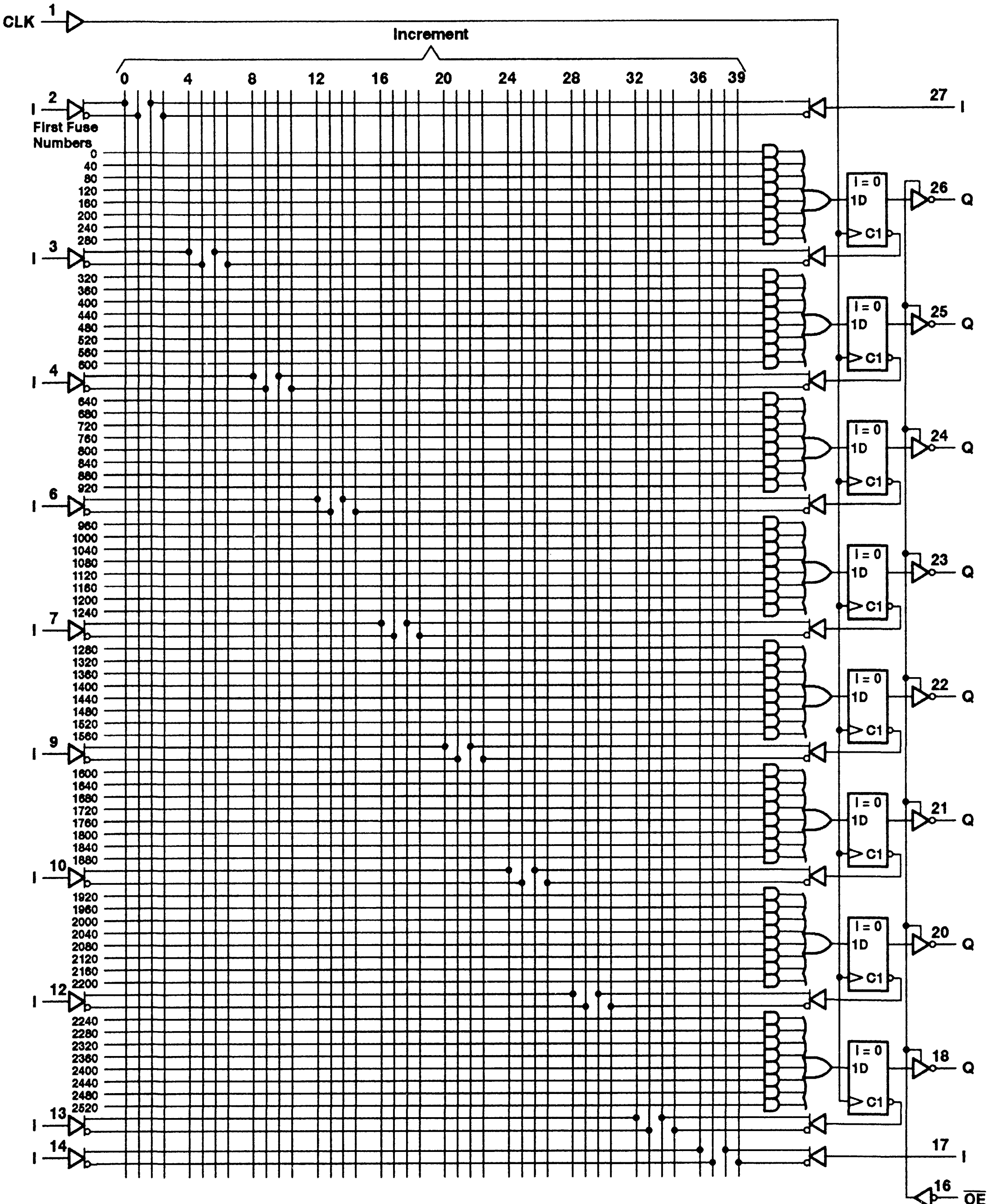
Fuse number = First fuse number + Increment

logic diagram (positive logic)



Fuse number = First fuse number + Increment.

logic diagram (positive logic)



Fuse number = First fuse number + Increment

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (see Note 1)	5.5 V
Voltage applied to disabled output (see Note 1)	5.5 V
Operating free-air temperature range	0°C to 75°C
Storage temperature range	−65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

			-25CNL			-15CNL			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.75	5	5.25	4.75	5	5.25	V
V_{IH}	High-level input voltage		2		5.5	2		5.5	V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−3.2			−3.2	mA
I_{OL}	Low-level output current				24			24	mA
f_{clock}†	Clock frequency		0		33	0		45	MHz
t_w†	Pulse duration, clock	High	15			10			ns
		Low	15			12			
t_{su}†	Setup time, input or feedback before clock↑		25			15			ns
t_h†	Hold time, input or feedback after clock↑		0			0			ns
T_A	Operating free-air temperature		0	25	75	0	25	75	°C

† f_{clock}, t_w, t_{su}, and t_h do not apply for TIBPAL20L8'.

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		$V_{CC} = 4.75$ V,	$I_I = -18$ mA		–0.8	–1.5	V
V_{OH}		$V_{CC} = 4.75$ V,	$I_{OH} = -3.2$ mA	2.4			V
V_{OL}		$V_{CC} = 4.75$ V,	$I_{OL} = 24$ mA		0.3	0.5	V
I_{OZH}	O, Q outputs	$V_{CC} = 5.25$ V,	$V_O = 2.7$ V			20	µA
	I/O ports					100	
I_{OZL}	O, Q outputs	$V_{CC} = 5.25$ V,	$V_O = 0.4$ V			–20	µA
	I/O ports					–250	
I_I		$V_{CC} = 5.25$ V,	$V_I = 5.5$ V			0.1	mA
I_{IH}‡		$V_{CC} = 5.25$ V,	$V_I = 2.7$ V			25	µA
I_{IL}‡		$V_{CC} = 5.25$ V,	$V_I = 0.4$ V			–0.25	mA
I_{OS}§		$V_{CC} = 5.25$ V,	$V_O = 0$	–30	–70	–130	mA
I_{CC}		$V_{CC} = 5.25$ V, Outputs open,	$V_I = 0$, $\overline{OE}$ at V_{IH}		120	180	mA

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	TYP†	MAX	UNIT
f_{max}¶	With feedback		R1 = 200 Ω, R2 = 390 Ω, See Figure 2	37	40		MHz
	Without feedback			45	50		
t_{pd}	I, I/O	O, I/O			12	15	ns
t_{pd}	CLK↑	Q			8	12	ns
t_{en}	$\overline{OE}$	Q			10	15	ns
t_{dis}	$\overline{OE}$↑	Q			8	12	ns
t_{en}	I, I/O	O, I/O			12	18	ns
t_{dis}	I, I/O	O, I/O			12	15	ns

† All typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

¶ $f_{max}(\text{with feedback}) = \dfrac{1}{t_{su} + t_{pd}\ (\text{CLK to Q})}$, $f_{max}(\text{without feedback}) = \dfrac{1}{t_w\ \text{high} + t_w\ \text{low}}$,

f_{max} does not apply for TIBPAL20L8'

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.75 V,	I_I = −18 mA		−0.8	−1.5	V
V_{OH}		V_{CC} = 4.75 V,	I_{OH} = −3.2 mA	2.4	3.3		V
V_{OL}		V_{CC} = 4.75 V,	I_{OL} = 24 mA		0.3	0.5	V
I_{OZH}	O, Q outputs	V_{CC} = 5.25 V,	V_O = 2.7 V			20	µA
	I/O ports					100	
I_{OZL}	O, Q outputs	V_{CC} = 5.25 V,	V_O = 0.4 V			−20	µA
	I/O ports					−250	
I_I		V_{CC} = 5.25 V,	V_I = 5.5 V			0.1	mA
I_{IH}‡		V_{CC} = 5.25 V,	V_I = 2.7 V			20	µA
I_{IL}‡		V_{CC} = 5.25 V,	V_I = 0.4 V			−0.2	mA
I_{OS}§		V_{CC} = 5.25 V,	V_O = 0	−30	−70	−130	mA
I_{CC}		V_{CC} = 5.25 V, Outputs open,	V_I = 0, $\overline{OE}$ at V_{IH}		75	105	mA

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	TYP†	MAX	UNIT
f_{max}¶	With feedback		R1 = 200 Ω, R2 = 390 Ω, See Figure 2	25	40		MHz
	Without feedback			33	50		
t_{pd}	I, I/O	O, I/O		3	14	25	ns
t_{pd}	CLK↑	Q		2	10	15	ns
t_{en}	$\overline{OE}$	Q		2	8	15	ns
t_{dis}	$\overline{OE}$↑	Q		2	8	15	ns
t_{en}	I, I/O	O, I/O		3	15	25	ns
t_{dis}	I, I/O	O, I/O		3	15	25	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ For I/O ports, the parameters I_{IH} and I_{IL} include the off-state output current.

§ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

¶ $f_{max}\text{(with feedback)} = \dfrac{1}{t_{su} + t_{pd}\text{ (CLK to Q)}}$, $f_{max}\text{(without feedback)} = \dfrac{1}{t_w\text{ high} + t_w\text{ low}}$,

f_{max} does not apply for TIBPAL20L8'

programming information

Texas Instruments programmable logic devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments programmable logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

preload procedure for registered outputs (see Figure 1 and Note 2)

The output registers can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below.

Step 1. With V_{CC} at 5 volts and Pin 1 at V_{IL}, raise Pin 16 to V_{IHH}.
Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.
Step 3. Pulse Pin 1, clocking in preload data.
Step 4. Remove output voltage, then lower Pin 16 to V_{IL}. Preload can be verified by observing the voltage level at the output pin.

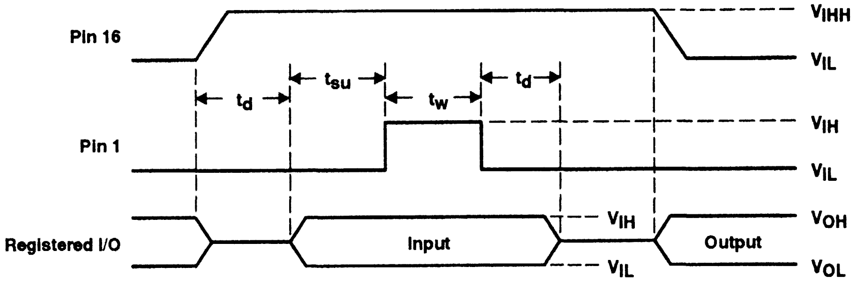
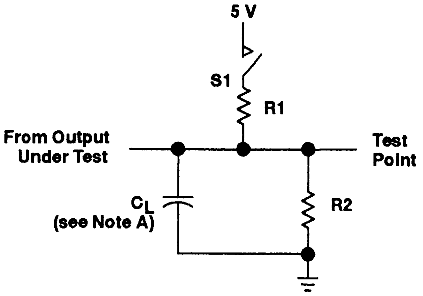


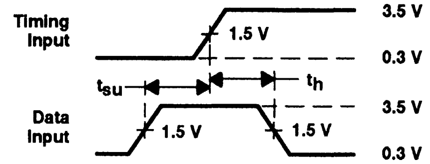
Figure 1. Preload Waveforms

NOTE 2: $t_d = t_{su} = t_h$ = 100 ns to 1000 ns V_{IHH} = 10.25 V to 10.75 v

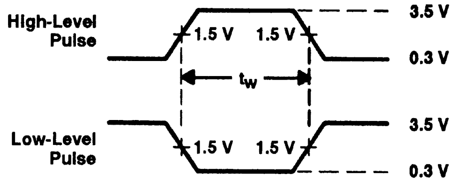
PARAMETER MEASUREMENT INFORMATION



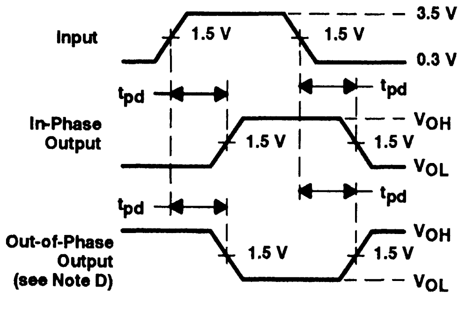
LOAD CIRCUIT FOR
3-STATE OUTPUTS



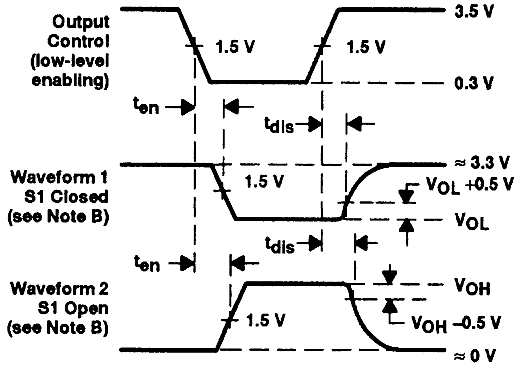
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 1 MHz, t_r and $t_f \le 2$ ns, duty cycle = 50%.
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.
E. Equivalent loads may be used for testing.

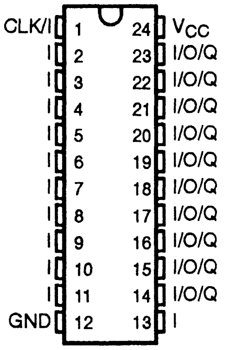
Figure 2. Load Circuit and Voltage Waveforms

TIBPAL22V10C, TIBPAL22V10AC, TIBPAL22V10AM
HIGH-PERFORMANCE *IMPACT*™ PROGRAMMABLE ARRAY LOGIC CIRCUITS

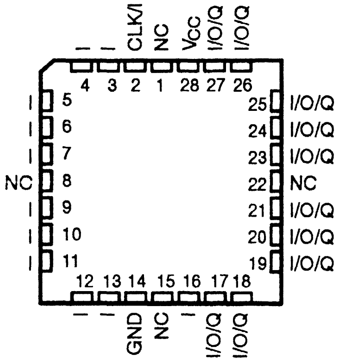
SRPS024 – D2943, OCTOBER 1986 – REVISED MARCH 1992

- **Second-Generation PLD Architecture**
- **Choice of Operating Speeds**
  - **TIBPAL22V10AC . . . 25 ns Max**
  - **TIBPAL22V10AM . . . 30 ns Max**
  - **TIBPAL22V10C . . . 35 ns Max**
- **Increased Logic Power – Up to 22 Inputs and 10 Outputs**
- **Increased Product Terms – Average of 12 Per Output**
- **Variable Product Term Distribution Allows More Complex Functions to Be Implemented**
- **Each Output Is User Programmable for Registered or Combinational Operation, Polarity, and Output Enable Control**
- **TTL-Level Preload for Improved Testability**
- **Extra Terms Provide Logical Synchronous Set and Asynchronous Reset Capability**
- **Fast Programming, High Programming Yield, and Unsurpassed Reliability Ensured Using Ti-W Fuses**
- **AC and DC Testing Done at the Factory Utilizing Special Designed-In Test Features**
- **Dependable Texas Instruments Quality and Reliability**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**
- **Functionally Equivalent to AMDs AMPAL22V10 and AMPAL22V10A**

C SUFFIX . . . NT PACKAGE
M SUFFIX . . . JT PACKAGE
(TOP VIEW)



C SUFFIX . . . FN PACKAGE
M SUFFIX . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection
Pin assignments in operating mode

description

The TIBPAL22V10 and TIBPAL22V10A are programmable array logic devices featuring high speed and functional equivalency when compared to presently available devices. They are implemented with the familiar sum-of-products (AND-OR) logic structure featuring the new concept "Programmable Output Logic Macrocell". These IMPACT™ circuits combine the latest Advanced Low-Power Schottky technology with proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional TTL logic.

These devices contain up to 22 inputs and 10 outputs. They incorporate the unique capability of defining and programming the architecture of each output on an individual basis. Outputs may be registered or nonregistered and inverting or noninverting as shown in the output logic macrocell diagram. The ten potential outputs are enabled through the use of individual product terms.

These devices are covered by U.S. Patent 4,410,987.
IMPACT is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 1992, Texas Instruments Incorporated

description (continued)

Further advantages can be seen in the introduction of variable product term distribution. This technique allocates from 8 to 16 logical product terms to each output for an average of 12 product terms per output. This variable allocation of terms allows far more complex functions to be implemented than in previously available devices.

Circuit design is enhanced by the addition of a synchronous set and an asynchronous reset product term. These functions are common to all registers. When the synchronous set product term is a logic 1, the output registers are loaded with a logic 1 on the next low-to-high clock transition. When the asynchronous reset product term is a logic 1, the output registers are loaded with a logic 0. The output logic level after set or reset depends on the polarity selected during programming. Output registers can be preloaded to any desired state during testing. Preloading permits full logical verification during product testing.

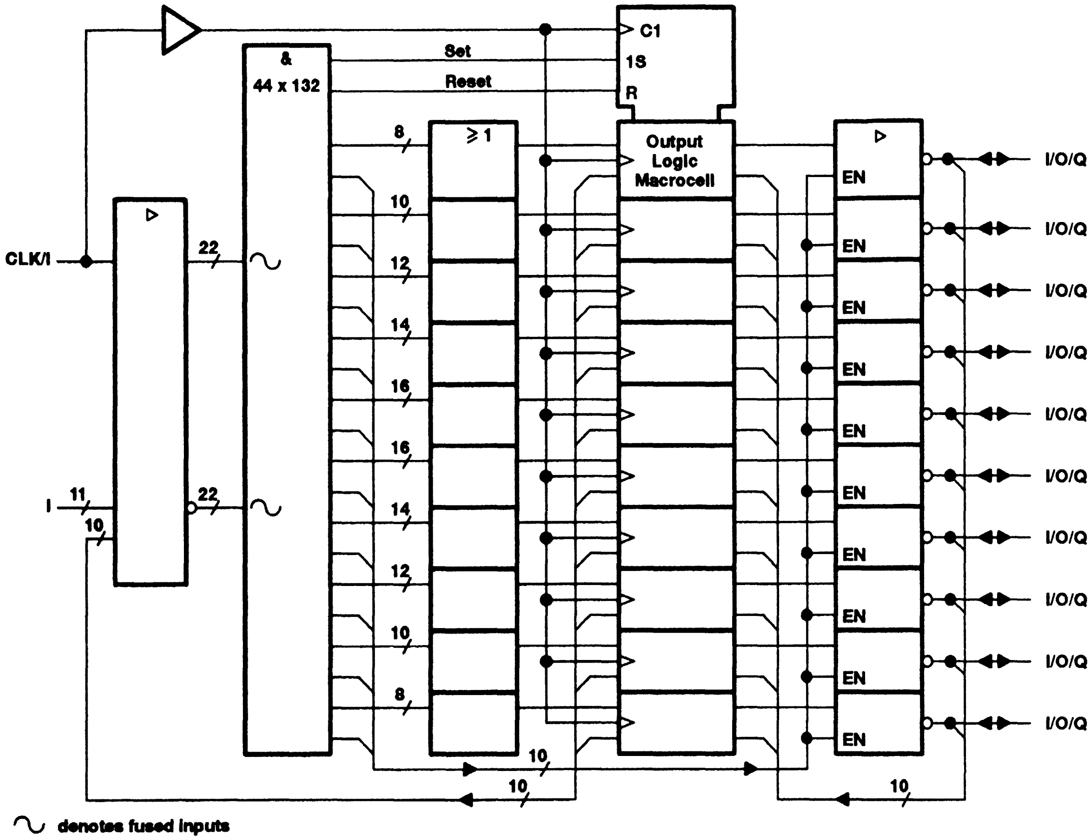
With features such as programmable output logic macrocells and variable product term distribution, the TIBPAL22V10 and TIBPAL22V10A offer quick design and development of custom LSI functions with complexities of 500 to 800 equivalent gates. Since each of the ten output pins may be individually configured as inputs on either a temporary or permanent basis, functions requiring up to 21 inputs and a single output or down to 12 inputs and 10 outputs are possible.

A power-up clear function is supplied that forces all registered outputs to a predetermined state after power is applied to the device. Registered outputs selected as active-low power up with their outputs high. Registered outputs selected as active-high power up with their outputs low.

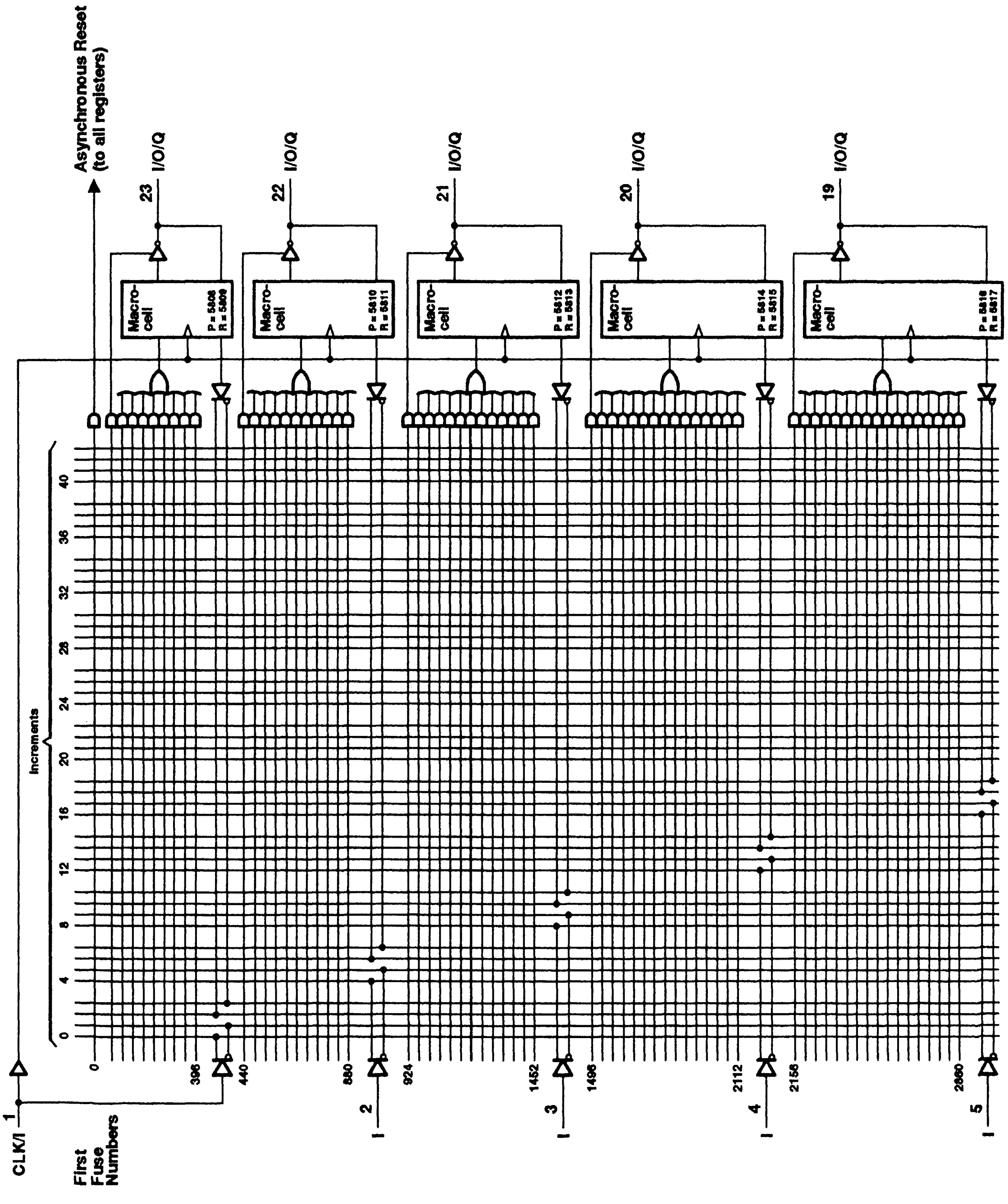
A single security fuse is provided on each device to discourage unauthorized copying of fuse patterns. Once blown, the verification circuitry is disabled and all other fuses will appear to be open.

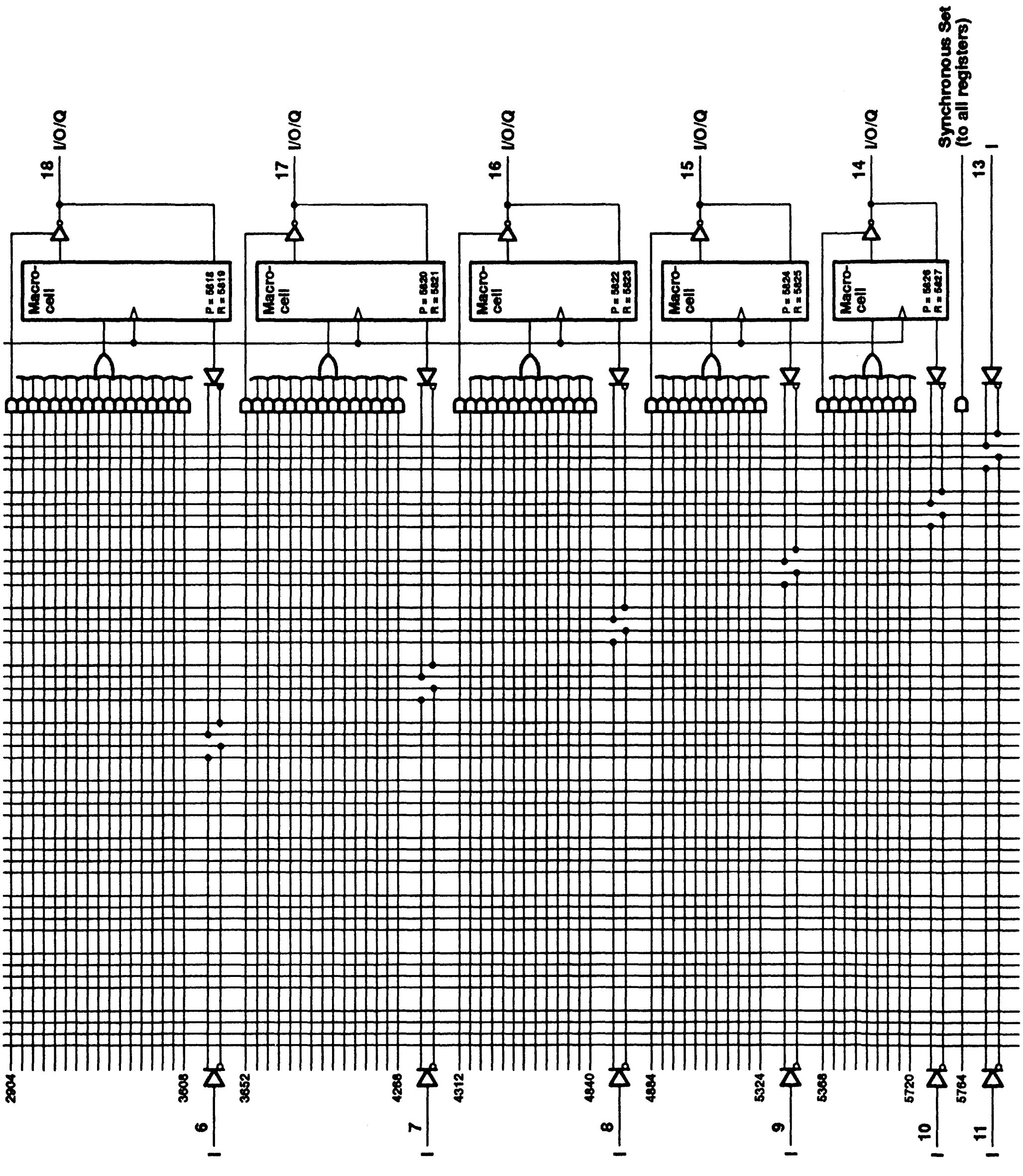
The TIBPAL22V10C and TIBPAL22V10AC are characterized for operation from 0°C to 75°C. The TIBPAL22V10AM is characterized for operation over the full military temperature range of –55°C to125°C.

functional block diagram (positive logic)



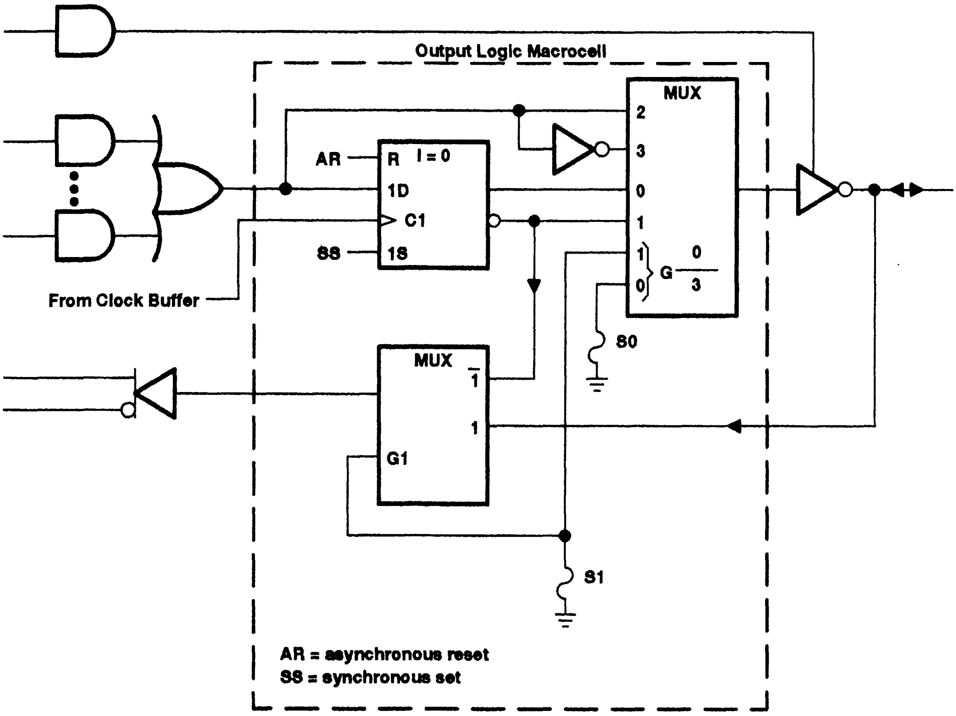
logic symbol (positive logic)

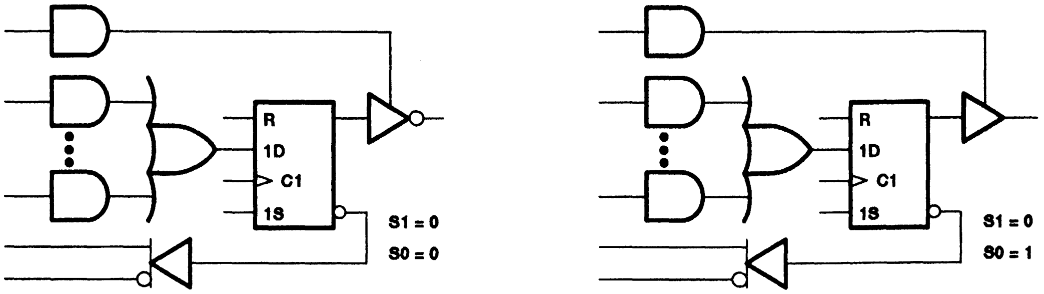




Fuse number = First fuse number + Increment
Inside each MACROCELL the "P" fuse is the polarity fuse and the "R" fuse is the register fuse.

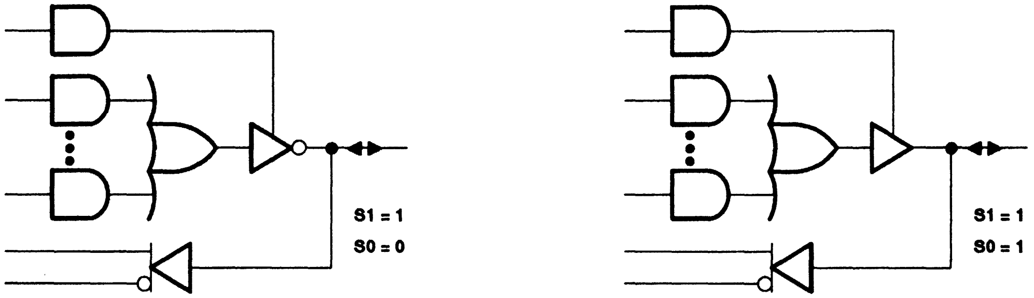
output logic macrocell diagram





REGISTER FEEDBACK, REGISTERED, ACTIVE-LOW OUTPUT

REGISTER FEEDBACK, REGISTERED, ACTIVE-HIGH OUTPUT



I/O FEEDBACK, COMBINATIONAL, ACTIVE-LOW OUTPUT

I/O FEEDBACK, COMBINATIONAL, ACTIVE-HIGH OUTPUT

MACROCELL FEEDBACK AND OUTPUT FUNCTION TABLE

FUSE SELECT		FEEDBACK AND OUTPUT CONFIGURATION		
S1	S0			
0	0	Register feedback	Registered	Active low
0	1	Register feedback	Registered	Active high
1	0	I/O feedback	Combinational	Active low
1	1	I/O feedback	Combinational	Active high

0 = unblown fuse, 1 = blown fuse

S1 and S0 are select-function fuses as shown in the output logic macrocell diagram.

Figure 1. Resultant Macrocell Feedback and Output Logic After Programming

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (see Note 1)	−5.5 V
Voltage range applied to disabled output (see Note 1)	5.5 V
Operating free-air temperature range	0°C to 75°C
Storage temperature range	−65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle or during a preload cycle.

recommended operating conditions

			TIBPAL22V10C			TIBPAL22V10AC			UNIT
			MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage		4.75	5	5.25	4.75	5	5.25	V
V_{IH}	High-level input voltage		2		5.5	2		5.5	V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−3.2			−3.2	mA
I_{OL}	Low-level output current				16			16	mA
f_{clock}	Clock frequency†				18			28.5	MHz
t_w	Pulse duration	Clock high or low	25			15			ns
		Asynchronous reset high or low	35			25			
t_{su}	Setup time before clock↑	Input	30			20			ns
		Feedback	30			20			
		Synchronous set	30			25			
		Asynchronous reset low (inactive)	35			25			
t_h	Hold time, input, set, or feedback after clock↑		0			0			ns
T_A	Operating free-air temperature		0		75	0		75	°C

† f_{clock} (with feedback) = $\frac{1}{t_{su} + t_{pd}(\text{CLK to Q})}$, f_{clock} (without feedback) = $\frac{1}{t_{w(low)} + t_{w(high)}}$

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS	TIBPAL22V10C			TIBPAL22V10AC			UNIT
			MIN	TYP†	MAX	MIN	TYP†	MAX	
V_{IK}		V_{CC} = 4.75 V, I_I = −18 mA			−1.2			−1.2	V
V_{OH}		V_{CC} = 4.75 V, I_{OH} = −3.2 mA	2.4	3.5		2.4	3.5		V
V_{OL}		V_{CC} = 4.75 V, I_{OL} = 16 mA		0.35	0.5		0.35	0.5	V
I_{OZH}		V_{CC} = 5.25 V, V_O = 2.7 V			0.1			0.1	mA
I_{IL}	Any output	V_{CC} = 5.25 V, V_I = 0.4 V			−100			−100	μA
	Any I/O				−250			−250	
I_I		V_{CC} = 5.25 V, V_I = 5.5 V			1			1	mA
I_{IH}		V_{CC} = 5.25 V, V_I = 2.7 V			25			25	μA
I_{IL}		V_{CC} = 5.25 V, V_I = 0.4 V			−0.25			−0.25	mA
I_{OS}‡		V_{CC} = 5.25 V, V_O = 0.5 V	−30		−90	−30		−90	mA
I_{CC}		V_{CC} = 5.25 V, V_I = GND, Outputs open		120	180		120	180	mA

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TIBPAL22V10C			TIBPAL22V10AC			UNIT
				MIN	TYP†	MAX	MIN	TYP†	MAX	
f_{max}¶	With feedback		R1 = 300 Ω, R2 = 390 Ω, See Figure 4	18			28.5			MHz
t_{pd}	I, I/O	I/O			15	35		15	25	ns
t_{pd}	I, I/O (reset)	Q			15	40		15	30	ns
t_{pd}	CLK	Q			10	25		10	15	ns
t_{en}	I, I/O	I/O, Q			15	35		15	25	ns
t_{dis}	I, I/O	I/O, Q			15	35		15	25	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second. V_O is set at 0.5 V to avoid test problems caused by test equipment ground degradation.

¶ $f_{max}\text{ (with feedback)} = \dfrac{1}{t_{su} + t_{pd}\text{(CLK to Q)}}$, $f_{max}\text{ (without feedback)} = \dfrac{1}{t_{w}\text{(low)} + t_{w}\text{(high)}}$

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (see Note 1)	–5.5 V
Voltage range applied to disabled output (see Note 1)	5.5 V
Operating free-air temperature range	–55°C to 125°C
Storage temperature range	–65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle or during a preload cycle.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				–2	mA
I_{OL}	Low-level output current				12	mA
f_{clock}	Clock frequency†				22	MHz
t_w	Pulse duration	Clock high or low	20			ns
		Asynchronous reset high or low	30			
t_{su}	Setup time before clock↑	Input	25			ns
		Feedback	25			
		Synchronous set	25			
		Asynchronous reset low (inactive)	30			
t_h	Hold time, input, set, or feedback after clock↑		0			ns
T_A	Operating free-air temperature		–55		125	°C

† f_{clock} (with feedback) $= \frac{1}{t_{su} + t_{pd}(\text{CLK to Q})}$, f_{clock} (without feedback) $= \frac{1}{t_{w(low)} + t_{w(high)}}$

electrical characteristics over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = –18 mA				–1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = –2 mA		2.4	3.5		V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA			0.25	0.5	V
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V				0.1	mA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V				–100	μA
I_I	V_{CC} = 5.5 V,	V_I = 5.5 V				1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V				25	μA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V				–0.25	mA
I_{OS}‡	V_{CC} = 5.5 V,	V_O = 0.5 V		–30		–90	mA
I_{CC}	V_{CC} = 5.5 V,	V_I = GND,	Outputs open		120	180	mA

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP†	MAX	UNIT
f_{max}¶	With feedback		R1 = 390 Ω, R2 = 750 Ω, See Figure 4	22			MHz
t_{pd}	I, I/O	I/O			15	30	ns
t_{pd}	I, I/O (reset)	Q			15	35	ns
t_{pd}	CLK	Q			10	20	ns
t_{en}	I, I/O	I/O, Q			15	30	ns
t_{dis}	I, I/O	I/O, Q			15	30	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second. V_O is set at 0.5 V to avoid test problems caused by test equipment ground degradation.

¶ f_{max} (with feedback) = $\frac{1}{t_{su} + t_{pd}(\text{CLK to Q})}$, f_{max} (without feedback) = $\frac{1}{t_{w}(\text{low}) + t_{w}(\text{high})}$

preload procedure for registered outputs (see Notes 2 and 3)

The output registers can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below:

Step 1. With V_{CC} at 5 V and pin 1 at V_{IL}, raise pin 13 to V_{IHH}.
Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.
Step 3. Pulse pin 1, clocking in preload data.
Step 4. Remove output voltage, then lower pin 13 to V_{IL}. Preload can be verified by observing the voltage level at the output pin.

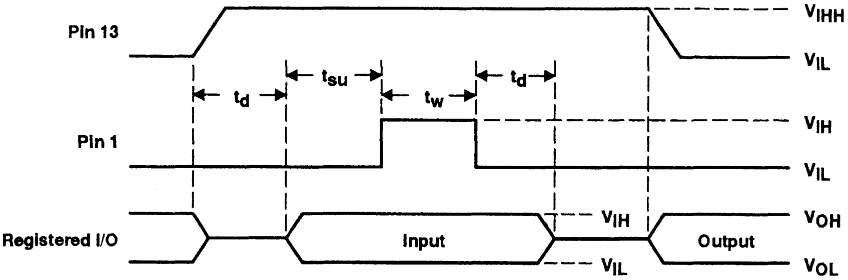
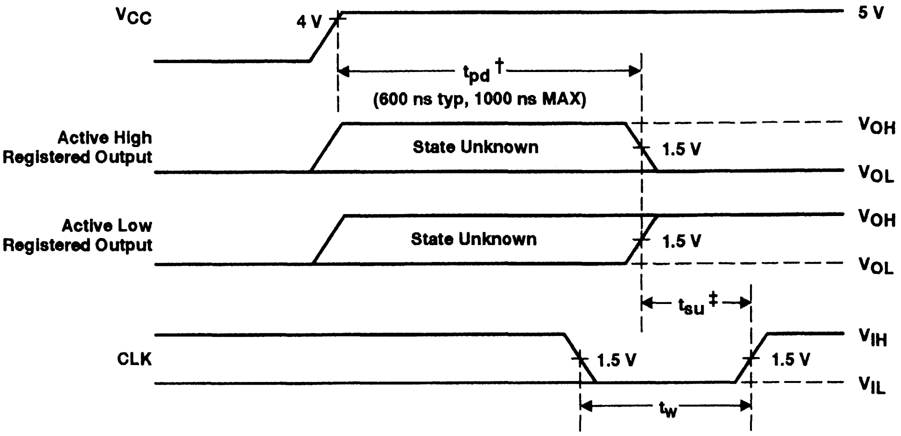


Figure 2. Preload Waveforms

NOTES: 2. Pin numbers shown are for JT and NT packages only. If chip-carrier socket adapter is not used, pin numbers must be changed accordingly.
3. $t_d = t_{su} = t_w$ = 100 ns to 1000 ns. V_{IHH} = 10.25 V to 10.75 V.

power-up reset

Following power up, all registers are reset to zero. The output level depends on the polarity selected during programming. This feature provides extra flexibility to the system designer and is especially valuable in simplifying state-machine initialization. To ensure a valid power-up reset, it is important that the rise of V_{CC} be monotonic. Following power-up reset, a low-to-high clock transition must not occur until all applicable input and feedback setup times are met.



† This is the power-up reset time and applies to registered outputs only. The values shown are from characterization data.
‡ This is the setup time for input or feedback.

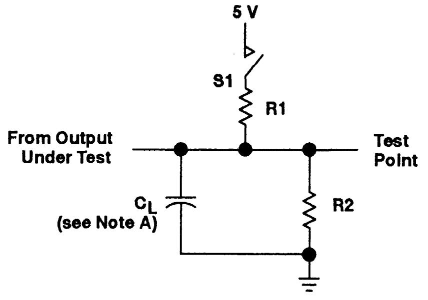
Figure 3. Power-Up Reset Waveforms

programming information

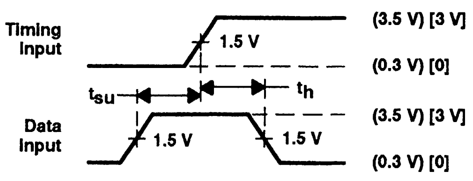
Texas Instruments programmable logic devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments programmable logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

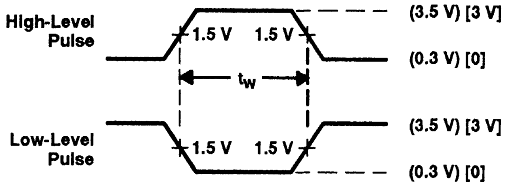
PARAMETER MEASUREMENT INFORMATION



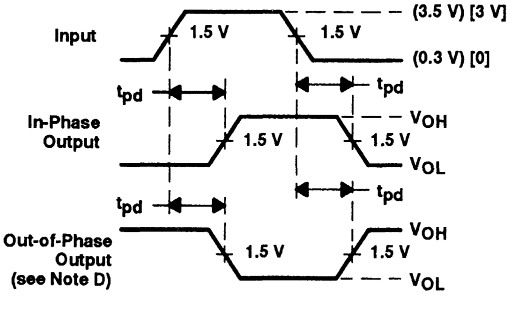
LOAD CIRCUIT FOR
3-STATE OUTPUTS



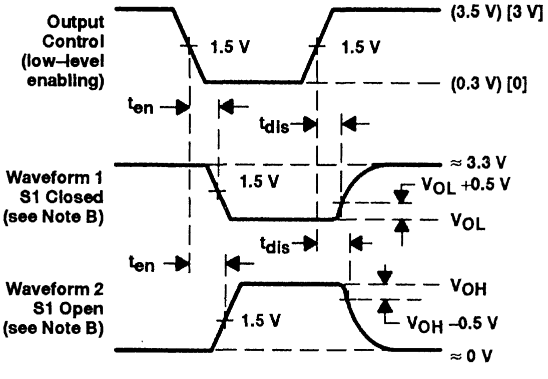
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES:
- A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses have the following characteristics: For C suffix, use the voltage levels indicated in parentheses ( ). PRR $\leq$ 1 MHz, $t_r = t_f \leq 2$ ns, duty cycle = 50%. For M suffix, use the voltage levels indicated in brackets [ ]. PRR $\leq$ 10 MHz, t_r and $t_f \leq 2$ ns, duty cycle = 50%.
- D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.
- E. Equivalent loads may be used for testing.

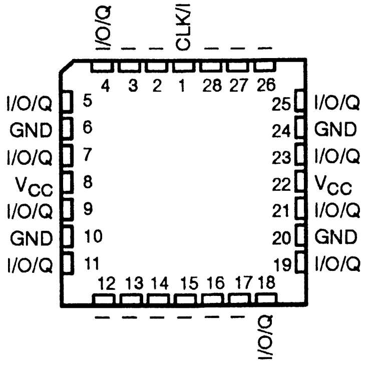
Figure 4. Load Circuit and Voltage Waveforms

TIBPAL22V10-5C
HIGH-PERFORMANCE *IMPACT-XL*™ PROGRAMMABLE ARRAY LOGIC CIRCUIT

SRPS028 – MAY 1992

- **High-Performance Operation:**
  f_{max} (External Feedback) . . . 111 MHz
  Propagation Delay . . . 5 ns Max
- **Increased Logic Power – Up to 22 Inputs and 10 Outputs**
- **Increased Product Terms – Average of 12 Per Output**
- **Variable Product Term Distribution Allows More Complex Functions to Be Implemented**
- **Each Output Is User Programmable for Registered or Combinational Operation, Polarity, and Output Enable Control**
- **Power-Up Clear on Registered Outputs**
- **TTL-Level Preload for Improved Testability**
- **Extra Terms Provide Logical Synchronous Set and Asynchronous Reset Capability**
- **Fast Programming, High Programming Yield, and Unsurpassed Reliability Ensured Using Ti-W Fuses**
- **AC and DC Testing Done at the Factory Utilizing Special Designed-In Test Features**
- **JEDEC Approved Revolutionary Power and Ground Pinout for 28-Pin Chip Carrier Reduces Cross Talk and Ground Bounce**
- **JEDEC File Compatibility Allows Previous '22V10 Designs to be Programmed Into the TIBPAL22V10-5C Without Modifications**

FN PACKAGE
(TOP VIEW)



PRODUCT PREVIEW

description

The TIBPAL22V10-5C is a programmable array logic device featuring high speed and functional equivalency when compared to presently available devices. The TIBPAL22V10-5C is implemented with the familiar sum-of-products (AND-OR) logic structure featuring programmable output logic macrocells. These IMPACT-XL™ circuits combine the latest Advanced Low-Power Schottky technology with proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional TTL logic.

This device contains up to 22 inputs and 10 outputs. It incorporates the unique capability of defining and programming the architecture of each output on an individual basis. Outputs may be registered or nonregistered and inverting or noninverting as shown in the output logic macrocell diagram. The ten potential outputs are enabled through the use of individual product terms.

Further advantages can be seen in the introduction of variable product term distribution. This technique allocates from 8 to 16 logical product terms to each output for an average of 12 product terms per output. This variable allocation of terms allows far more complex functions to be implemented than in previously available devices.

This device is covered by U.S. Patent 4,410,987.
IMPACT-XL is a trademark of Texas Instruments Incorporated.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

Copyright © 1992, Texas Instruments Incorporated

description (continued)

Circuit design is enhanced by the addition of a synchronous set and an asynchronous reset product term. These functions are common to all registers. When the synchronous set product term is a logic 1, the output registers are loaded with a logic 1 on the next low-to-high clock transition. When the asynchronous reset product term is a logic 1, the output registers are loaded with a logic 0. The output logic level after set or reset depends on the polarity selected during programming. Output registers can be preloaded to any desired state during testing. Preloading permits full logical verification during product testing.

With features such as programmable output logic macrocells and variable product term distribution, the TIBPAL22V10-5C offers quick design and development of custom LSI functions with complexities of 500 to 800 equivalent gates. Since each of the ten output pins may be individually configured as inputs on either a temporary or permanent basis, functions requiring up to 21 inputs and a single output or down to 12 inputs and 10 outputs are possible.

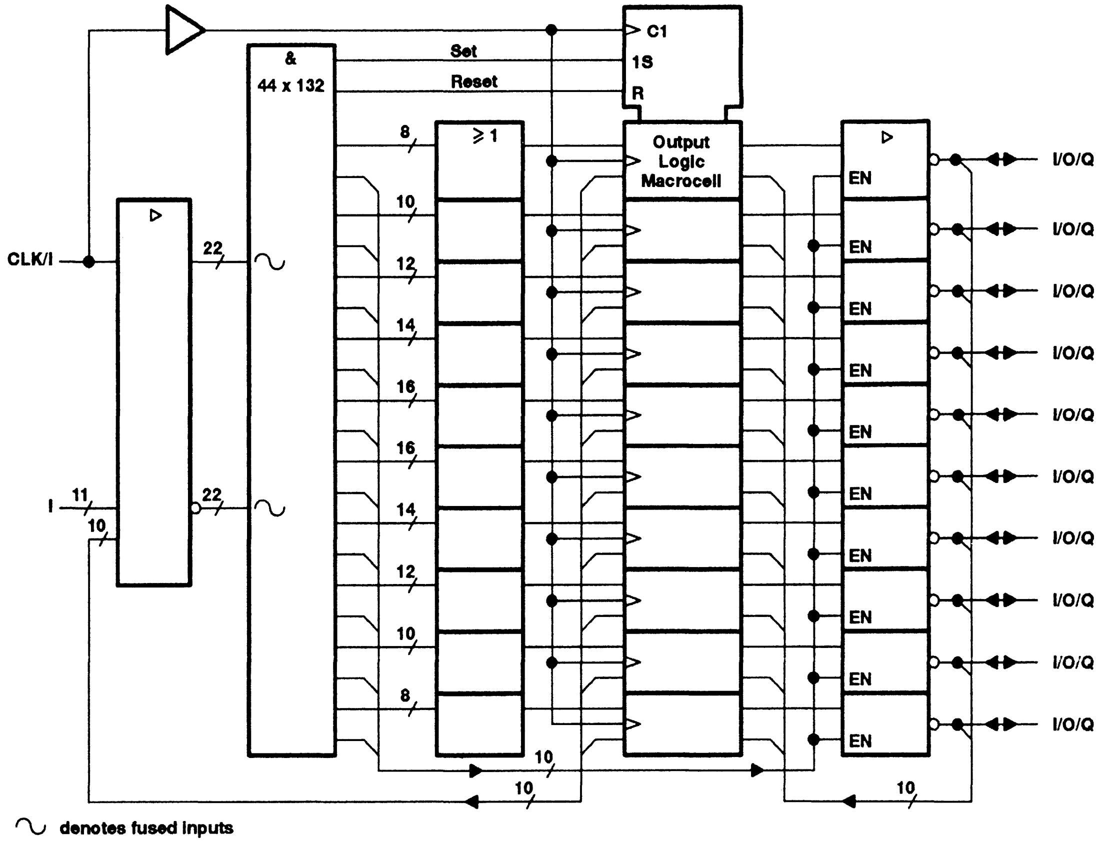
A power-up clear function is supplied that forces all registered outputs to a predetermined state after power is applied to the device. Registered outputs selected as active-low power up with their outputs high. Registered outputs selected as active-high power up with their outputs low.

A single security fuse is provided on each device to discourage unauthorized copying of fuse patterns. Once blown, the verification circuitry is disabled and all other fuses will verify as open.

The TIBPAL22V10-5C is characterized for operation from 0°C to 75°C.

PRODUCT PREVIEW

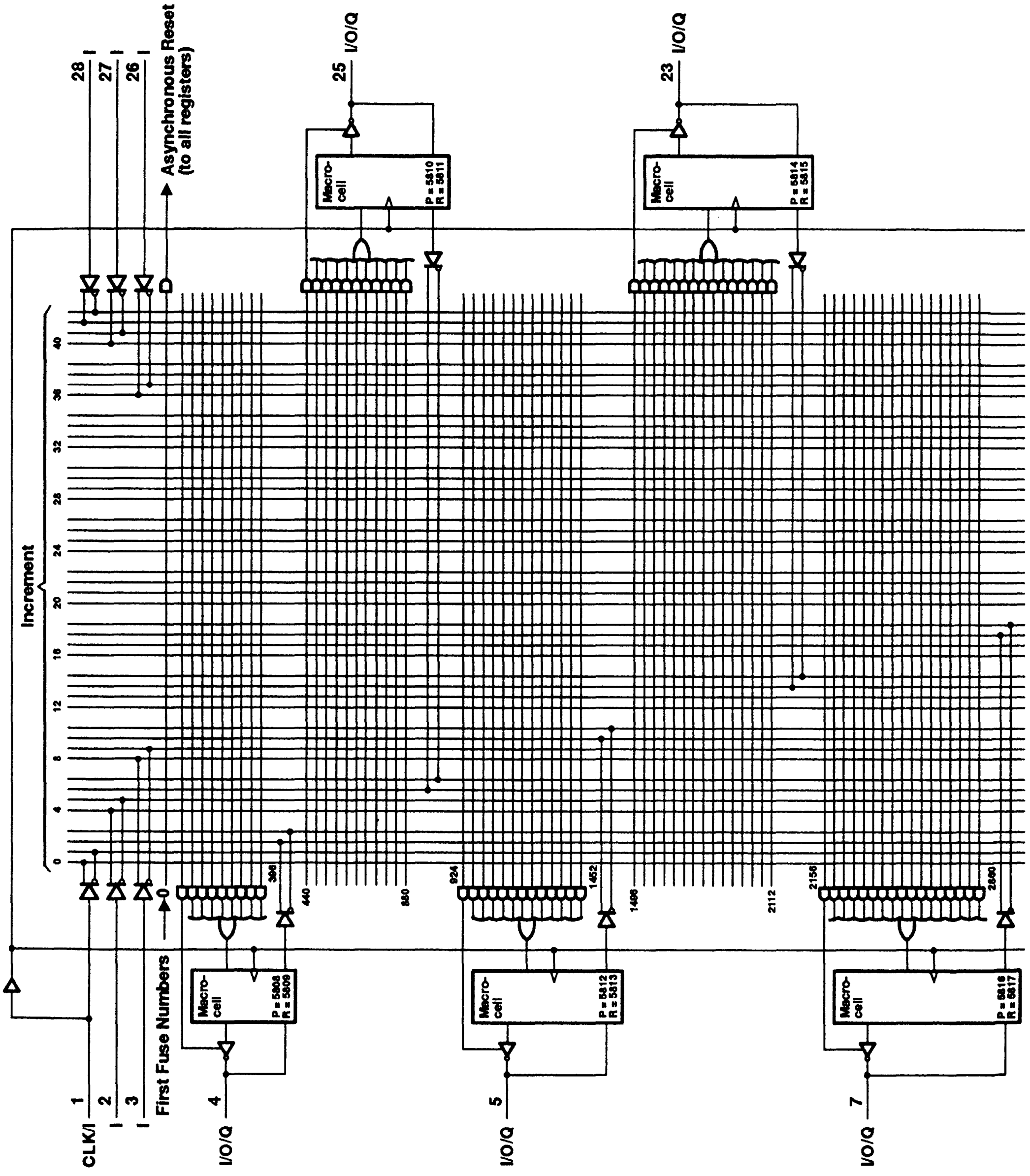
functional block diagram (positive logic)

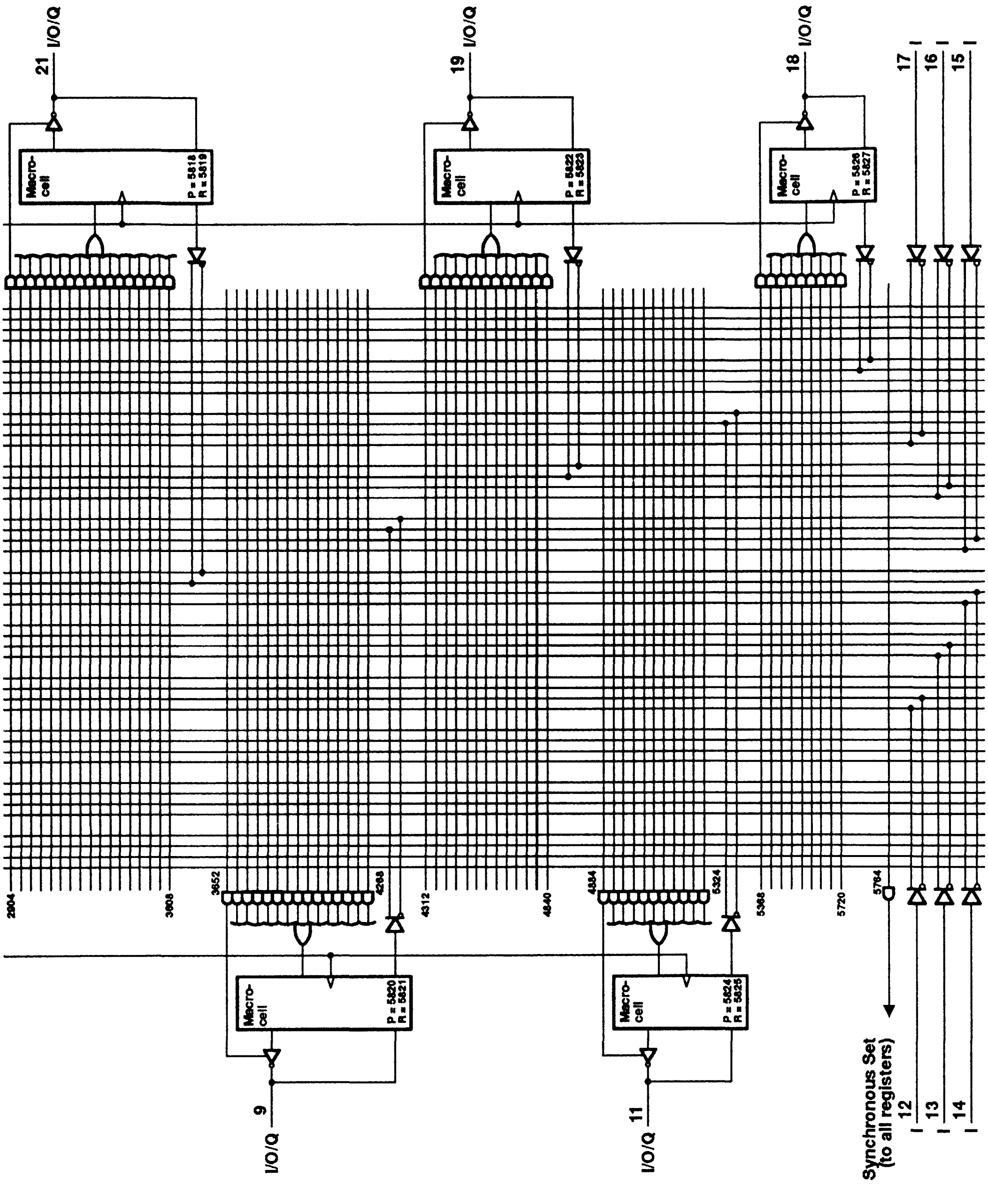


PRODUCT PREVIEW

PRODUCT PREVIEW

logic diagram (positive logic)

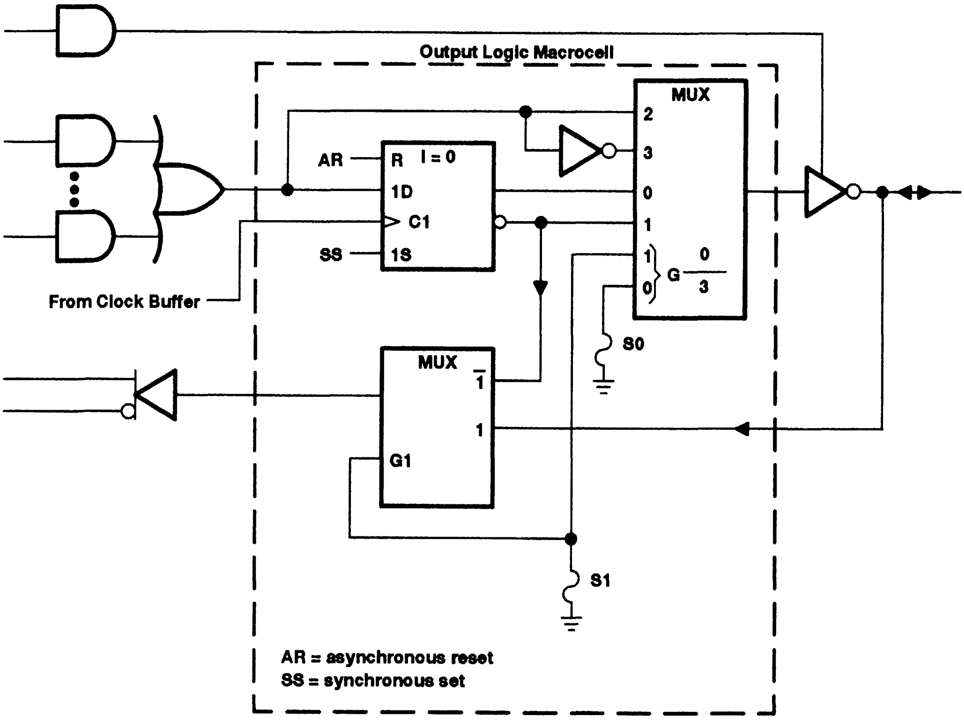




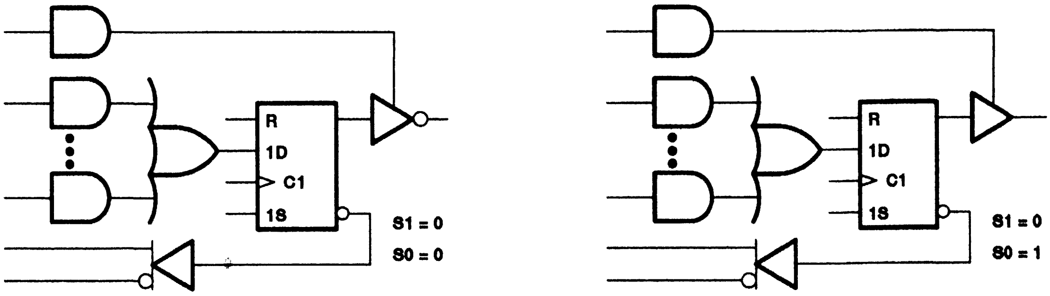
Fuse number = First fuse number + Increment
Inside each MACROCELL the "P" fuse is the polarity fuse and the "R" fuse is the register fuse.

PRODUCT PREVIEW

output logic macrocell diagram

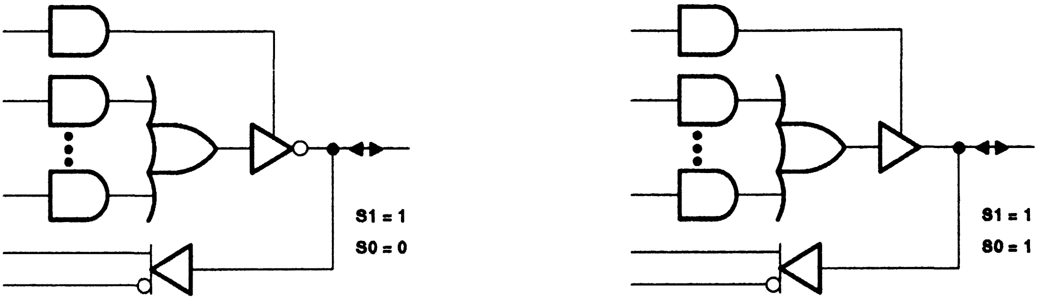


PRODUCT PREVIEW



REGISTER FEEDBACK, REGISTERED, ACTIVE-LOW OUTPUT

REGISTER FEEDBACK, REGISTERED, ACTIVE-HIGH OUTPUT



I/O FEEDBACK, COMBINATIONAL, ACTIVE-LOW OUTPUT

I/O FEEDBACK, COMBINATIONAL, ACTIVE-HIGH OUTPUT

MACROCELL FEEDBACK AND OUTPUT FUNCTION TABLE

FUSE SELECT		FEEDBACK AND OUTPUT CONFIGURATION		
S1	S0			
0	0	Register feedback	Registered	Active low
0	1	Register feedback	Registered	Active high
1	0	I/O feedback	Combinational	Active low
1	1	I/O feedback	Combinational	Active high

0 = unblown fuse, 1 = blown fuse

S1 and S0 are select-function fuses as shown in the output logic macrocell diagram.

Figure 1. Resultant Macrocell Feedback and Output Logic After Programming

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage range (see Note 1)	–1.2 V to V_{CC} +0.5 V
Voltage range applied to disabled output (see Note 1)	–0.5 V to V_{CC} +0.5 V
Operating free-air temperature range	0°C to 75°C
Storage temperature range	–65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle or during a preload cycle.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage (see Note 2)		2		5.5	V
V_{IL}	Low-level input voltage (see Note 2)				0.8	V
I_{OH}	High-level output current				–3.2	mA
I_{OL}	Low-level output current				16	mA
t_w	Pulse duration	Clock high or low	3.5			ns
		Asynchronous reset high or low	7			
t_{su}	Setup time before clock↑	Input	4.5			ns
		Feedback	4.5			
		Synchronous preset (active)	6			
		Synchronous preset (inactive)	6			
		Asynchronous reset (inactive)	6			
t_h	Hold time, input, set, or feedback after clock↑		0			ns
T_A	Operating free-air temperature		0		75	°C

NOTE 2: These are absolute voltage levels with respect to the ground pin of the device and includes all overshoots due to system and/or tester noise. Testing these parameters should not be attempted without suitable equipment.

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.75 V,	I_I = −18 mA				−1.2	V
V_{OH}		V_{CC} = 4.75 V,	I_{OH} = −3.2 mA		2.4			V
V_{OL}		V_{CC} = 4.75 V,	I_{OL} = 16 mA			0.35	0.5	V
I_{OZH}‡		V_{CC} = 5.25 V,	V_O = 2.7 V				0.1	mA
I_{OZL}‡		V_{CC} = 5.25 V,	V_O = 0.4 V				−0.1	mA
I_I		V_{CC} = 5.25 V,	V_I = 5.5 V				1	mA
I_{IH}‡		V_{CC} = 5.25 V,	V_I = 2.7 V				25	µA
I_{IL}	CLK	V_{CC} = 5.25 V,	V_I = 0.4 V				−0.25	mA
	All others						−0.1	
I_{OS}§		V_{CC} = 5.25 V,	V_O = 0.5 V		−30		−130	mA
I_{CC}		V_{CC} = 5.25 V,	V_I = GND,	Outputs open			210	mA
C_i	I	f = 1 MHz,	V_I = 2 V			5.5		pF
	CLK					9		
C_o		f = 1 MHz,	V_O = 2 V			5		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ I/O leakage is the worst case of I_{OZL} and I_{IL} or I_{OZH} and I_{IH}, respectively.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second. V_O is set at 0.5 V to avoid test problems caused by test equipment ground degradation.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	MAX	UNIT
f_{max}¶	Without feedback		R1 = 300 Ω, R2 = 300 Ω, See Figure 4	143		MHz
	With internal feedback (counter configuration)			133		
	With external feedback			111		
t_{pd}	I, I/O	I/O		1	5	ns
t_{pd}	I, I/O (reset)	Q			10	ns
t_{pd}	CLK	Q		1	4.5	ns
t_{pd}#	CLK	Feedback			3	ns
t_{en}	I, I/O	I/O, Q			6.5	ns
t_{dis}	I, I/O	I/O, Q			6	ns

¶ $$f_{max}\text{ (without feedback)} = \frac{1}{t_{w(low)} + t_{w(high)}}$$

$$f_{max}\text{ (with internal feedback)} = \frac{1}{t_{su} + t_{pd}\text{(CLK to feedback)}}$$

$$f_{max}\text{ (with external feedback)} = \frac{1}{t_{su} + t_{pd}\text{(CLK to Q)}}$$

This parameter is calculated from the measured f_{max} with internal feedback in the counter configuration.

PRODUCT PREVIEW

preload procedure for registered outputs (see Note 3)

The output registers can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below:

Step 1. With V_{CC} at 5 V and pin 1 at V_{IL}, raise pin 14 to V_{IHH}.
Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.
Step 3. Pulse pin 1, clocking in preload data.
Step 4. Remove output voltage, then lower pin 14 to V_{IL}. Preload can be verified by observing the voltage level at the output pin.

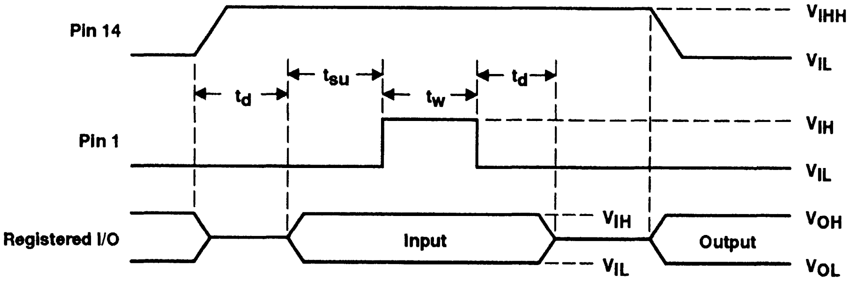
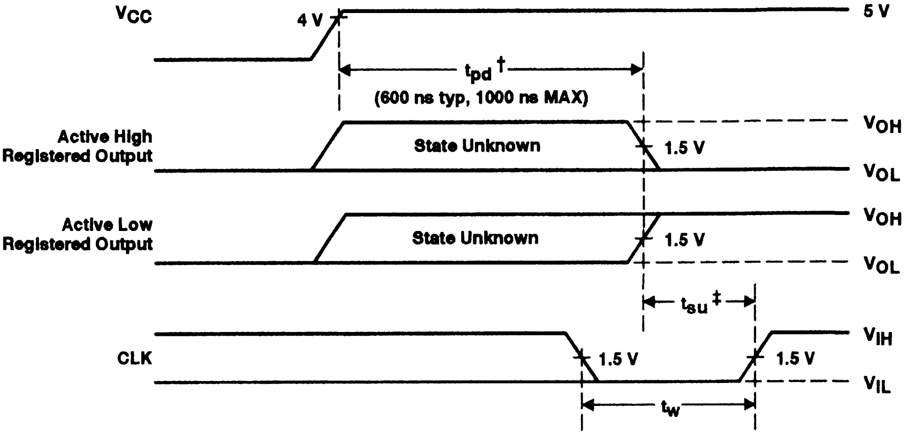


Figure 2. Preload Waveforms

NOTE 3: $t_d = t_{su} = t_w$ = 100 ns to 1000 ns. V_{IHH} = 10.25 V to 10.75 V.

power-up reset

Following power up, all registers are reset to zero. The output level depends on the polarity selected during programming. This feature provides extra flexibility to the system designer and is especially valuable in simplifying state-machine initialization. To ensure a valid power-up reset, it is important that the rise of V_{CC} be monotonic. Following power-up reset, a low-to-high clock transition must not occur until all applicable input and feedback setup times are met.



† This is the power-up reset time and applies to registered outputs only. The values shown are from characterization data.
‡ This is the setup time for input or feedback.

Figure 3. Power-Up Reset Waveforms

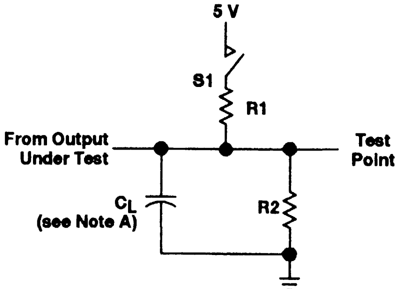
programming information

Texas Instruments programmable logic devices can be programmed using widely available software and inexpensive device programmers.

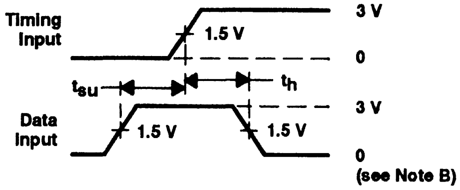
Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments programmable logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

PARAMETER MEASUREMENT INFORMATION

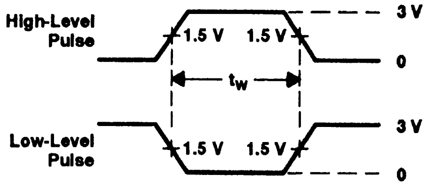
PRODUCT PREVIEW



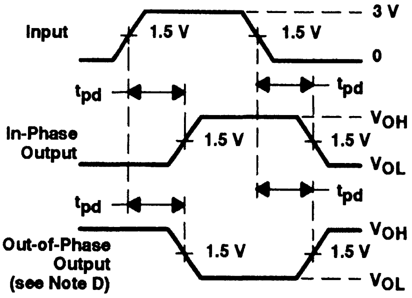
LOAD CIRCUIT FOR 3-STATE OUTPUTS



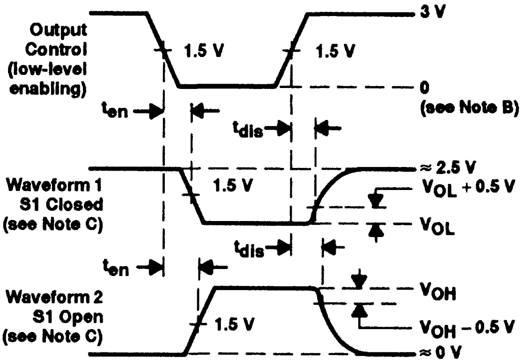
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATIONS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES:
A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
B. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.
E. Equivalent loads may be used for testing.

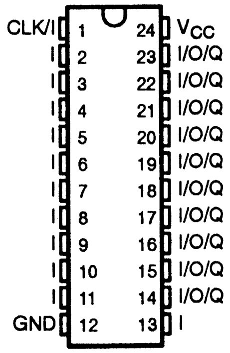
Figure 4. Load Circuit and Voltage Waveforms

TIBPAL22V10-7C, TIBPAL22V10-10M
HIGH-PERFORMANCE *IMPACT-X*™ PROGRAMMABLE ARRAY LOGIC CIRCUITS

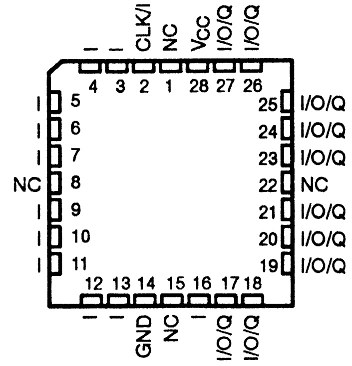
SRPS014B – D3520, AUGUST 1990 – REVISED SEPTEMBER 1992

- **Second-Generation PLD Architecture**
- **High-Performance Operation:**
  f_{max} (External Feedback)
    TIBPAL22V10-7C . . . 80 MHz Min
    TIBPAL22V10-10M . . . 71 MHz Min
  Propagation Delay
    TIBPAL22V10-7C . . . 7.5 ns Max
    TIBPAL22V10-10M . . . 10 ns Max
- **Increased Logic Power – Up to 22 Inputs and 10 Outputs**
- **Increased Product Terms – Average of 12 Per Output**
- **Variable Product Term Distribution Allows More Complex Functions to Be Implemented**
- **Each Output Is User Programmable for Registered or Combinational Operation, Polarity, and Output Enable Control**
- **Power-Up Clear on Registered Outputs**
- **TTL-Level Preload for Improved Testability**
- **Extra Terms Provide Logical Synchronous Set and Asynchronous Reset Capability**
- **Fast Programming, High Programming Yield, and Unsurpassed Reliability Ensured Using Ti-W Fuses**
- **AC and DC Testing Done at the Factory Utilizing Special Designed-In Test Features**
- **Package Options Include Both Plastic and Ceramic Chip Carriers in Addition to Plastic and Ceramic DIPs**

C SUFFIX . . . NT PACKAGE
M SUFFIX . . . JT PACKAGE
(TOP VIEW)



C SUFFIX . . . FN PACKAGE
M SUFFIX . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection
Pin assignments in operating mode

description

The TIBPAL22V10-7C and TIBPAL22V10-10M are programmable array logic devices featuring high speed and functional equivalency when compared to presently available devices. They are implemented with the familiar sum-of-products (AND-OR) logic structure featuring programmable output logic macrocells. These IMPACT-X™ circuits combine the latest Advanced Low-Power Schottky technology with proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional TTL logic.

These devices contain up to 22 inputs and 10 outputs. They incorporate the unique capability of defining and programming the architecture of each output on an individual basis. Outputs may be registered or nonregistered and inverting or noninverting as shown in the output logic macrocell diagram. The ten potential outputs are enabled through the use of individual product terms.

These devices are covered by U.S. Patent 4,410,987.
IMPACT-X is a trademark of Texas Instruments Incorporated.

UNLESS OTHERWISE NOTED this document contains PRODUCTION DATA information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 1992, Texas Instruments Incorporated

description (continued)

Further advantages can be seen in the introduction of variable product term distribution. This technique allocates from 8 to 16 logical product terms to each output for an average of 12 product terms per output. This variable allocation of terms allows far more complex functions to be implemented than in previously available devices.

Circuit design is enhanced by the addition of a synchronous set and an asynchronous reset product term. These functions are common to all registers. When the synchronous set product term is a logic 1, the output registers are loaded with a logic 1 on the next low-to-high clock transition. When the asynchronous reset product term is a logic 1, the output registers are loaded with a logic 0. The output logic level after set or reset depends on the polarity selected during programming. Output registers can be preloaded to any desired state during testing. Preloading permits full logical verification during product testing.

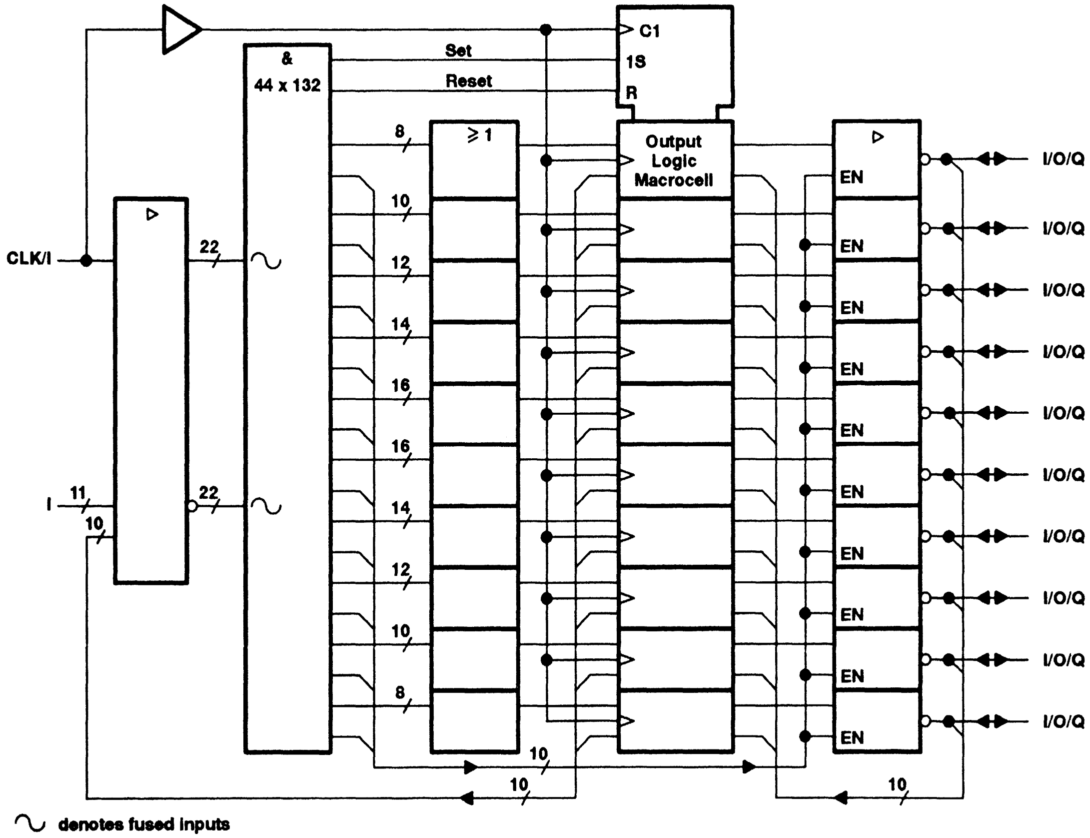
With features such as programmable output logic macrocells and variable product term distribution, the TIBPAL22V10' offers quick design and development of custom LSI functions with complexities of 500 to 800 equivalent gates. Since each of the ten output pins may be individually configured as inputs on either a temporary or permanent basis, functions requiring up to 21 inputs and a single output or down to 12 inputs and 10 outputs are possible.

A power-up clear function is supplied that forces all registered outputs to a predetermined state after power is applied to the device. Registered outputs selected as active-low power up with their outputs high. Registered outputs selected as active-high power up with their outputs low.

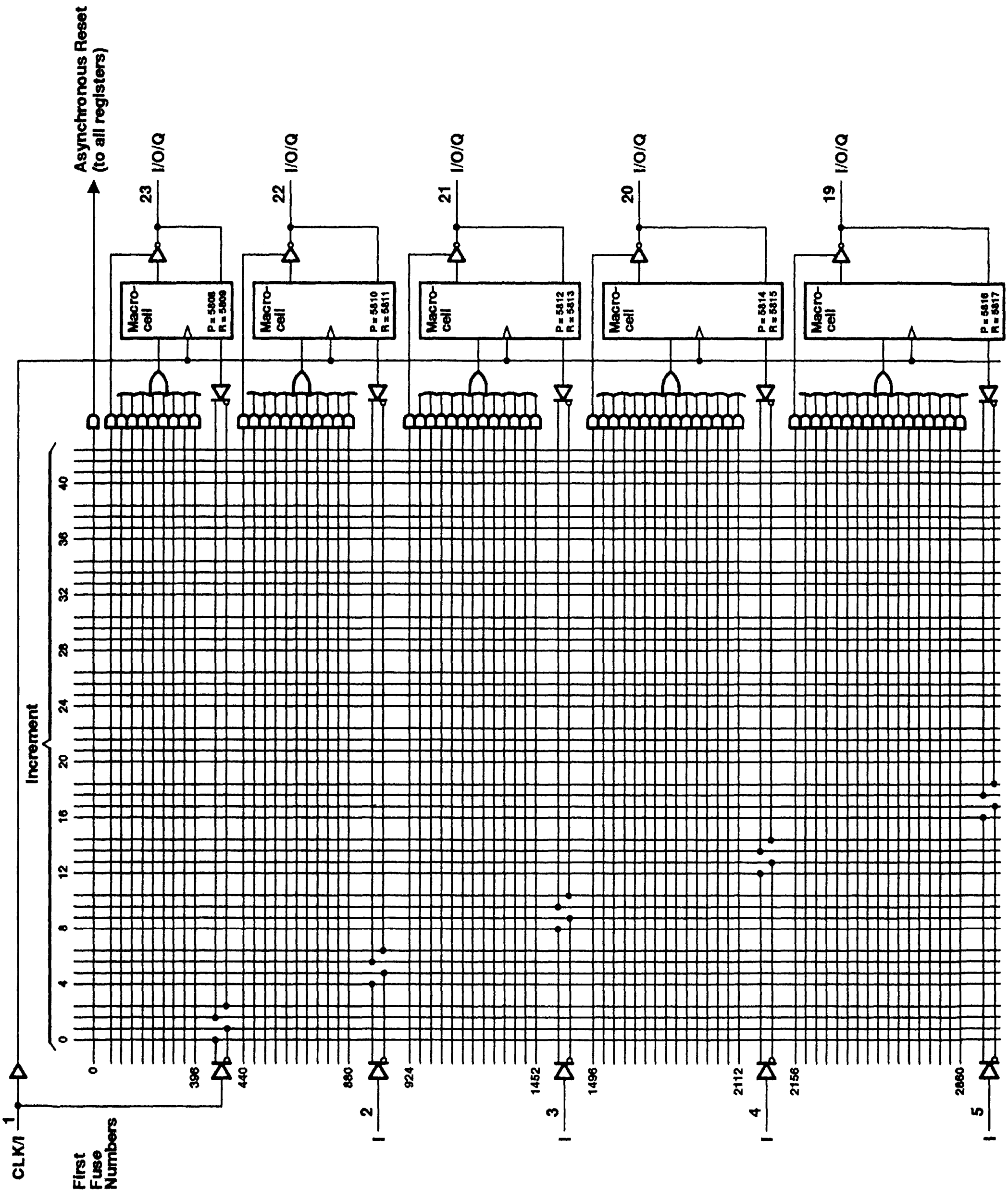
A single security fuse is provided on each device to discourage unauthorized copying of fuse patterns. Once blown, the verification circuitry is disabled and all other fuses will appear to be open.

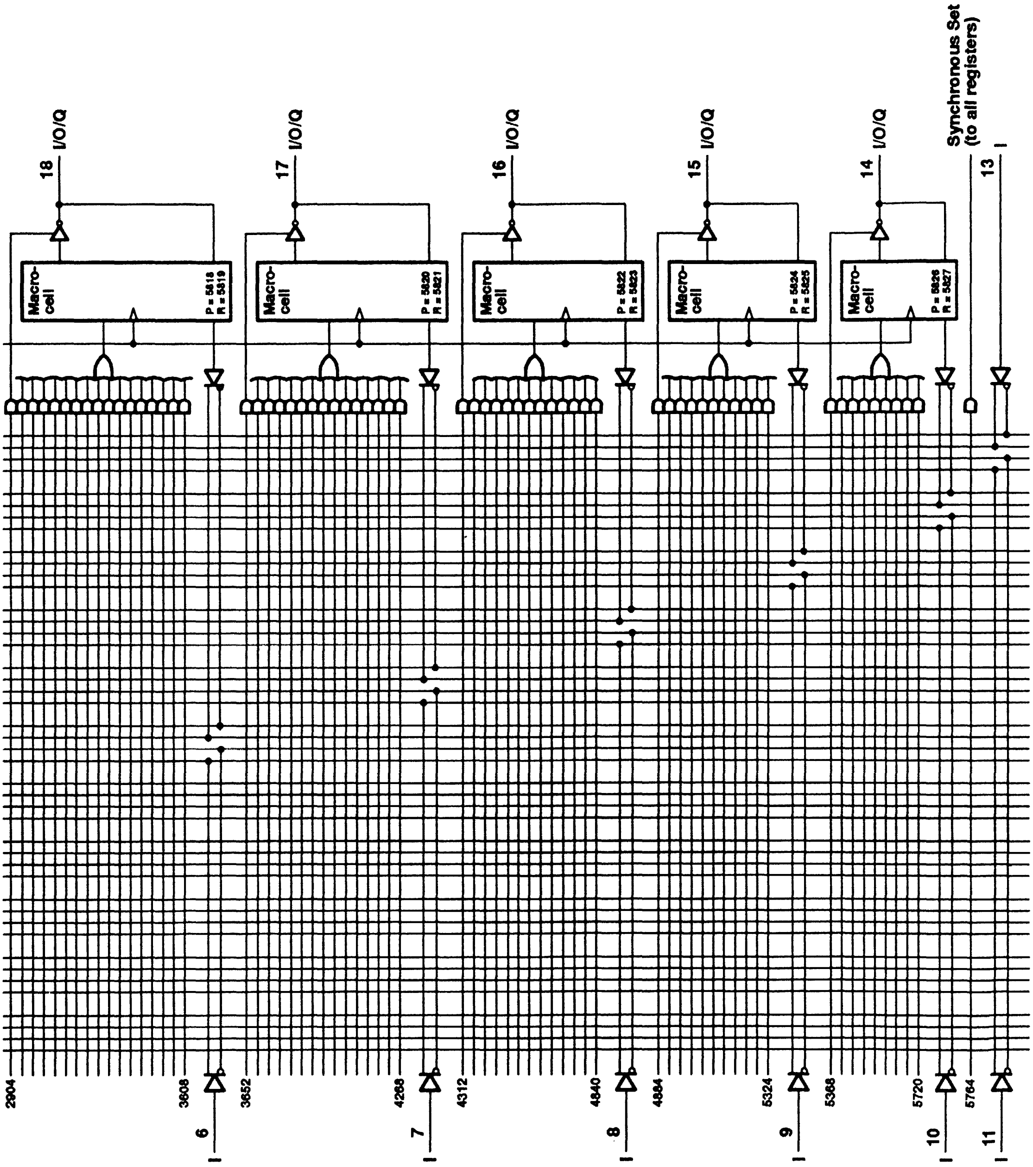
The TIBPAL22V10-7C is characterized for operation from 0°C to 75°C. The TIBPAL22V10-10M is characterized for operation over the full military temperature range of –55°C to 125°C.

functional block diagram (positive logic)



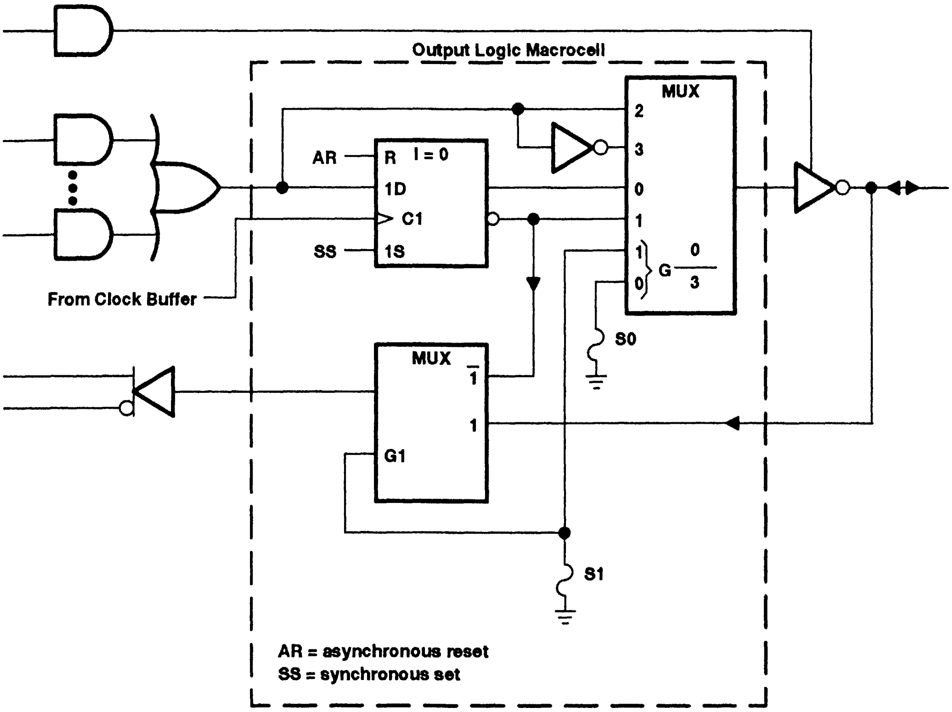
logic diagram (positive logic)

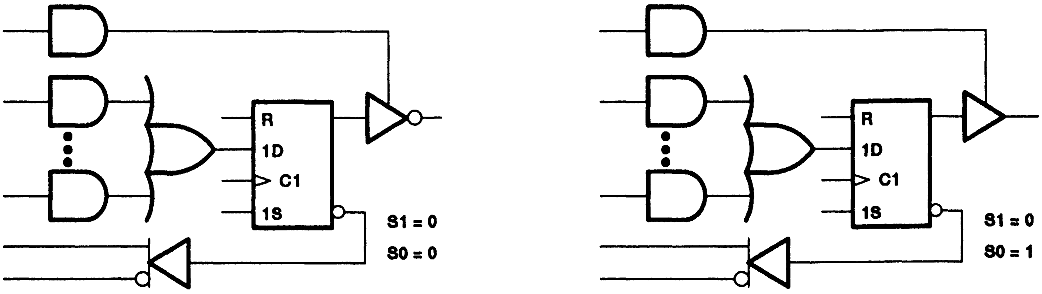




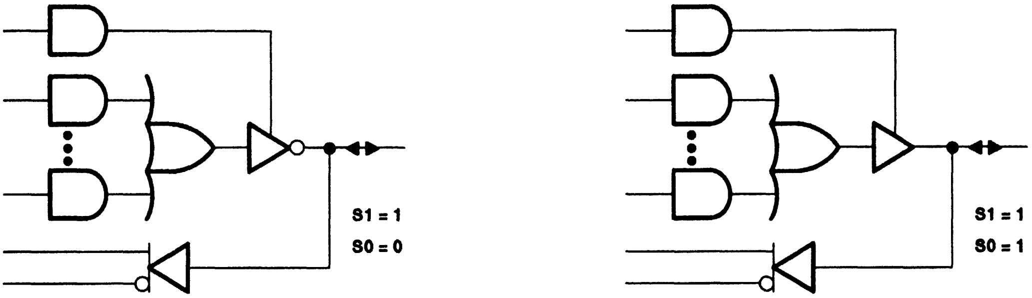
Fuse number = First fuse number + Increment
Inside each MACROCELL the "P" fuse is the polarity fuse and the "R" fuse is the register fuse.

output logic macrocell diagram





REGISTER FEEDBACK, REGISTERED, ACTIVE-LOW OUTPUT **REGISTER FEEDBACK, REGISTERED, ACTIVE-HIGH OUTPUT**



I/O FEEDBACK, COMBINATIONAL, ACTIVE-LOW OUTPUT **I/O FEEDBACK, COMBINATIONAL, ACTIVE-HIGH OUTPUT**

MACROCELL FEEDBACK AND OUTPUT FUNCTION TABLE

FUSE SELECT		FEEDBACK AND OUTPUT CONFIGURATION		
S1	**S0**			
0	0	Register feedback	Registered	Active low
0	1	Register feedback	Registered	Active high
1	0	I/O feedback	Combinational	Active low
1	1	I/O feedback	Combinational	Active high

0 = unblown fuse, 1 = blown fuse
S1 and S0 are select-function fuses as shown in the output logic macrocell diagram.

Figure 1. Resultant Macrocell Feedback and Output Logic After Programming

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage range (see Note 1)	–1.2 V to V_{CC} +0.5 V
Voltage range applied to disabled output (see Note 1)	–0.5 V to V_{CC} +0.5 V
Operating free-air temperature range	0°C to 75°C
Storage temperature range	–65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle or during a preload cycle.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage (see Note 2)		2		5.5	V
V_{IL}	Low-level input voltage (see Note 2)				0.8	V
I_{OH}	High-level output current				–3.2	mA
I_{OL}	Low-level output current				16	mA
t_w	Pulse duration	Clock high or low	4			ns
		Asynchronous reset high or low	6			
t_{su}	Setup time before clock↑	Input	5.5			ns
		Feedback	5.5			
		Synchronous preset (active)	8			
		Synchronous preset (inactive)	8			
		Asynchronous reset (inactive)	6			
t_h	Hold time, input, set, or feedback after clock↑		0			ns
T_A	Operating free-air temperature		0		75	°C

NOTE 2: These are absolute voltage levels with respect to the ground pin of the device and includes all overshoots due to system and/or tester noise. Testing these parameters should not be attempted without suitable equipment.

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS	MIN	TYP[†]	MAX	UNIT
V_{IK}		V_{CC} = 4.75 V, I_I = −18 mA			−1.2	V
V_{OH}		V_{CC} = 4.75 V, I_{OH} = −3.2 mA	2.4			V
V_{OL}		V_{CC} = 4.75 V, I_{OL} = 16 mA		0.35	0.5	V
I_{OZH}[‡]		V_{CC} = 5.25 V, V_O = 2.7 V			0.1	mA
I_{OZL}[‡]		V_{CC} = 5.25 V, V_O = 0.4 V			−0.1	mA
I_I		V_{CC} = 5.25 V, V_I = 5.5 V			1	mA
I_{IH}[‡]		V_{CC} = 5.25 V, V_I = 2.7 V			25	µA
I_{IL}	CLK	V_{CC} = 5.25 V, V_I = 0.4 V			−0.25	mA
	All others				−0.1	
I_{OS}[§]		V_{CC} = 5.25 V, V_O = 0.5 V	−30		−130	mA
I_{CC}		V_{CC} = 5.25 V, V_I = GND, Outputs open			210	mA
C_i		f = 1 MHz, V_I = 2 V		6		pF
C_o		f = 1 MHz, V_O = 2 V		8		pF

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[‡] I/O leakage is the worst case of I_{OZL} and I_{IL} or I_{OZH} and I_{IH}, respectively.

[§] Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second. V_O is set at 0.5 V to avoid test problems caused by test equipment ground degradation.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	TIBPAL22V10-7CFN		TIBPAL22V10-7CNT		UNIT
				MIN	MAX	MIN	MAX	
f_{max}[¶]	Without feedback		R1 = 300 Ω, R2 = 300 Ω, See Figure 6	125		125		MHz
	With internal feedback (counter configuration)			100		100		
	With external feedback			87		80		
t_{pd}	I, I/O	I/O		3	7.5	3	7.5	ns
t_{pd}	I, I/O (reset)	Q			12		12	ns
t_{pd}	CLK	Q		1.5	6	1.5	7	ns
t_{pd}[#]	CLK	Feedback			4.5		4.5	ns
t_{en}	I, I/O	I/O, Q			8		8	ns
t_{dis}	I, I/O	I/O, Q			7.5		7.5	ns

PRODUCT PREVIEW

[¶] f_{max} (without feedback) = $\dfrac{1}{t_{w(low)} + t_{w(high)}}$

f_{max} (with internal feedback) = $\dfrac{1}{t_{su} + t_{pd}(\text{CLK to feedback})}$

f_{max} (with external feedback) = $\dfrac{1}{t_{su} + t_{pd}(\text{CLK to Q})}$

[#] This parameter is calculated from the measured f_{max} with internal feedback in the counter configuration.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage range (see Note 1)	−1.2 V to V_{CC} +0.5 V
Voltage range applied to disabled output (see Note 1)	−0.5 V to V_{CC} +0.5 V
Operating free-air temperature range	−55°C to 125°C
Storage temperature range	−65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle or during a preload cycle.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage (see Note 2)		2		5.5	V
V_{IL}	Low-level input voltage (see Note 2)				0.8	V
I_{OH}	High-level output current				−2	mA
I_{OL}	Low-level output current				12	mA
t_w	Pulse duration	Clock high or low	5			ns
		Asynchronous reset high or low	10			
t_{su}	Setup time before clock↑	Input	7			ns
		Feedback	7			
		Synchronous preset (active)	9			
		Synchronous preset (inactive)	8			
		Asynchronous reset (inactive)	8			
t_h	Hold time, input, set, or feedback after clock↑		0			ns
T_A	Operating free-air temperature		−55		125	°C

NOTE 2: These are absolute voltage levels with respect to the ground pin of the device and includes all overshoots due to system and/or tester noise. Testing these parameters should not be attempted without suitable equipment.

PRODUCT PREVIEW

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = –18 mA				–1.2	V
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = –2 mA		2.4			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 12 mA			0.35	0.5	V
I_{OZH}‡		V_{CC} = 5.5 V,	V_O = 2.7 V				0.1	mA
I_{OZL}‡		V_{CC} = 5.5 V,	V_O = 0.4 V				–0.1	mA
I_I		V_{CC} = 5.5 V,	V_I = 5.5 V				1	mA
I_{IH}‡		V_{CC} = 5.5 V,	V_I = 2.7 V				25	µA
I_{IL}	CLK	V_{CC} = 5.5 V,	V_I = 0.4 V				–0.25	mA
	All others						–0.1	
I_{OS}§		V_{CC} = 5.5 V,	V_O = 0.5 V		–30		–130	mA
I_{CC}		V_{CC} = 5.5 V,	V_I = GND,	Outputs open			220	mA
C_i		f = 1 MHz,	V_I = 2 V			6		pF
C_o		f = 1 MHz,	V_O = 2 V			8		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ I/O leakage is the worst case of I_{OZL} and I_{IL} or I_{OZH} and I_{IH}, respectively.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second. V_O is set at 0.5 V to avoid test problems caused by test equipment ground degradation.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	MAX	UNIT
f_{max}¶	Without feedback		R1 = 390 Ω, R2 = 750 Ω, See Figure 6	100		MHz
	With internal feedback (counter configuration)			80		
	With external feedback			71		
t_{pd}	I, I/O	I/O		1	10	ns
t_{pd}	I, I/O (reset)	Q			15	ns
t_{pd}	CLK	Q		1	7	ns
t_{pd}#	CLK	Feedback			5.5	ns
t_{en}	I, I/O	I/O, Q			11	ns
t_{dis}	I, I/O	I/O, Q			9	ns

¶ f_{max} (without feedback) = $\dfrac{1}{t_{w(low)} + t_{w(high)}}$

f_{max} (with internal feedback) = $\dfrac{1}{t_{su} + t_{pd}(\text{CLK to feedback})}$

f_{max} with external feedback is not production tested and is calculated using the equation, f_{max} (with external feedback) = $\dfrac{1}{t_{su} + t_{pd}(\text{CLK to Q})}$

This parameter is calculated from the measured f_{max} with internal feedback in the counter configuration.

PRODUCT PREVIEW

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.

TEXAS INSTRUMENTS

preload procedure for registered outputs (see Notes 3 and 4)

The output registers can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below:

Step 1. With V_{CC} at 5 V and pin 1 at V_{IL}, raise pin 13 to V_{IHH}.
Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.
Step 3. Pulse pin 1, clocking in preload data.
Step 4. Remove output voltage, then lower pin 13 to V_{IL}. Preload can be verified by observing the voltage level at the output pin.

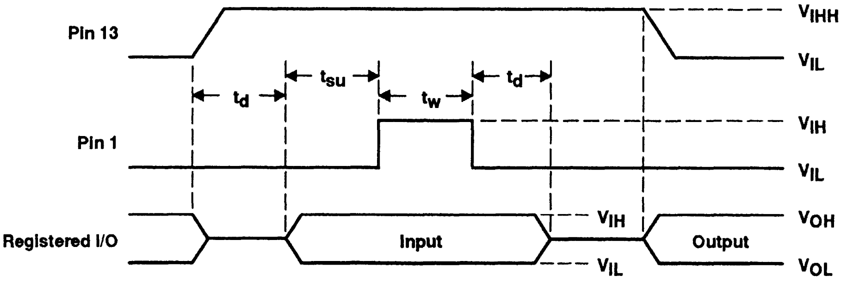
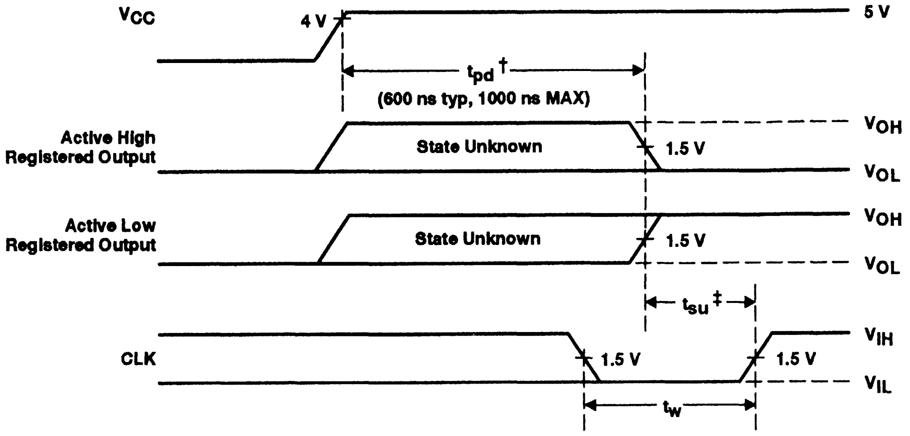


Figure 2. Preload Waveforms

NOTES: 3. Pin numbers shown are for the JT and NT packages only. If chip-carrier socket adapter is not used, pin numbers must be changed accordingly.
4. $t_d = t_{su} = t_w$ = 100 ns to 1000 ns. V_{IHH} = 10.25 V to 10.75 V.

power-up reset

Following power up, all registers are reset to zero. The output level depends on the polarity selected during programming. This feature provides extra flexibility to the system designer and is especially valuable in simplifying state-machine initialization. To ensure a valid power-up reset, it is important that the rise of V_{CC} be monotonic. Following power-up reset, a low-to-high clock transition must not occur until all applicable input and feedback setup times are met.



---

† This is the power-up reset time and applies to registered outputs only. The values shown are from characterization data.
‡ This is the setup time for input or feedback.

Figure 3. Power-Up Reset Waveforms

programming information

Texas Instruments programmable logic devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments programmable logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

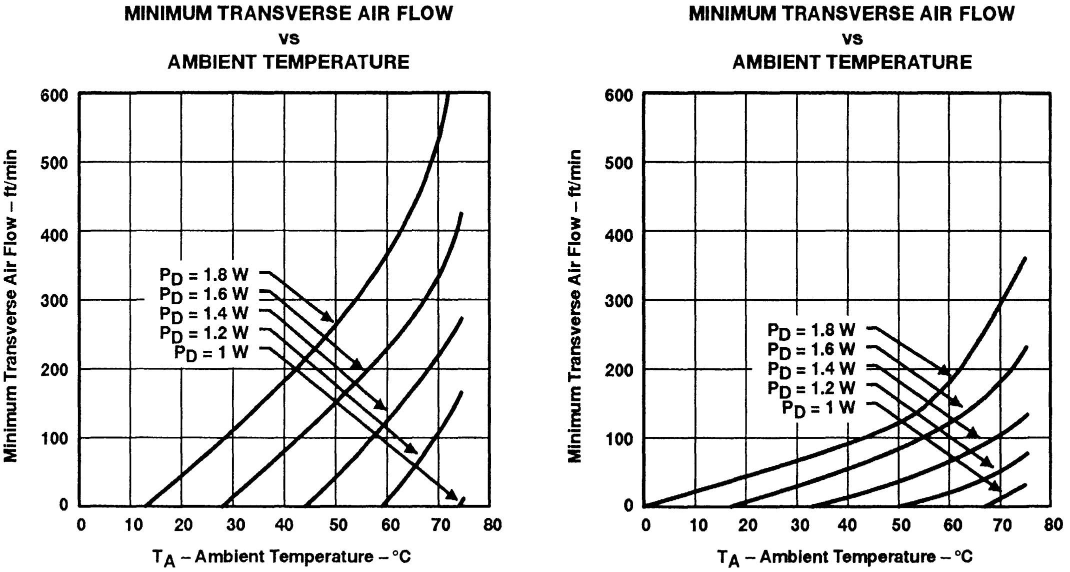
THERMAL INFORMATION

thermal management of the TIBPAL22V10-7C

Thermal management of the TIBPAL22V10-7CNT and TIBPAL22V10-7CFN is necessary when operating at certain conditions of frequency, output loading, and outputs switching simultaneously. The device and system application will determine the appropriate level of management.

Determining the level of thermal management is based on factors such as power dissipation (P_D), ambient temperature (T_A), and transverse airflow (FPM). Figures 4 (a) and 4 (b) show the relationship between ambient temperature and transverse airflow at given power dissipation levels. The required transverse airflow can be determined at a particular ambient temperature and device power dissipation level in order to ensure the device specifications.

Figure 5 illustrates how power dissipation varies as a function of frequency and the number of outputs switching simultaneously. It should be noted that all outputs are fully loaded (C_L = 50 pF). Since the condition of ten fully loaded outputs represents the worst-case condition, each application must be evaluated accordingly.



(a) TIBPAL22V10-7CNT

(b) TIBPAL22V10-7CFN

Figure 4

THERMAL INFORMATION

POWER DISSIPATION vs FREQUENCY

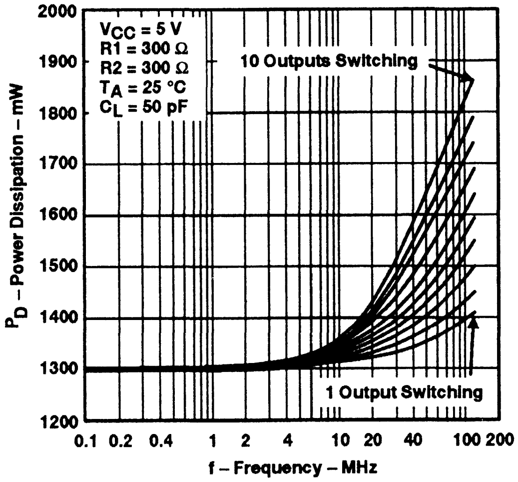
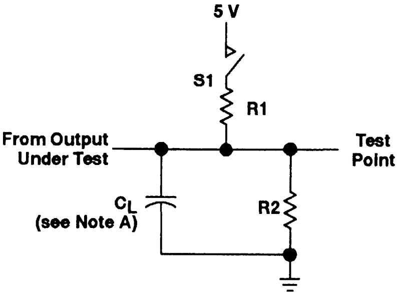
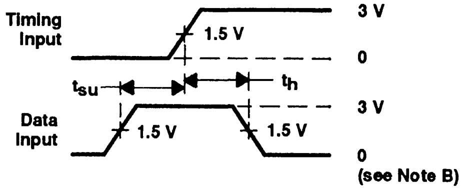


Figure 5

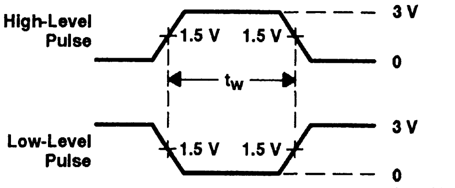
PARAMETER MEASUREMENT INFORMATION



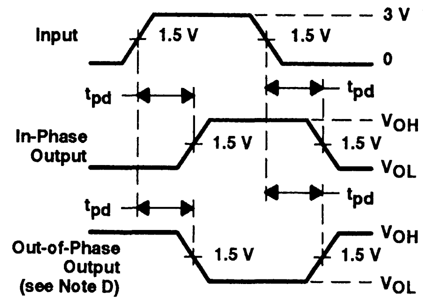
LOAD CIRCUIT FOR
3-STATE OUTPUTS



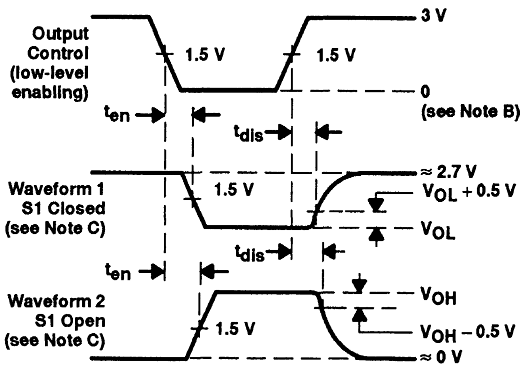
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
B. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.
E. Equivalent loads may be used for testing.

Figure 6. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

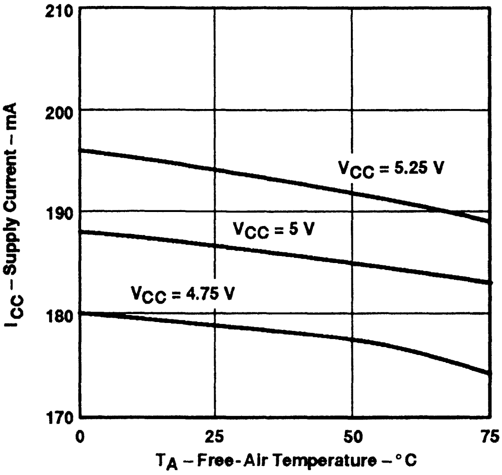


Figure 7

PROPAGATION DELAY TIME
vs
SUPPLY VOLTAGE

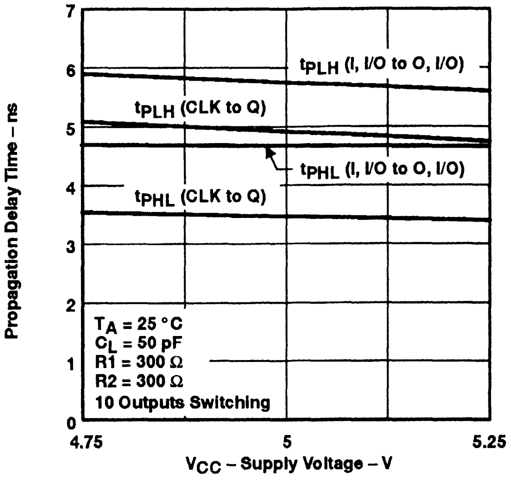


Figure 8

PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

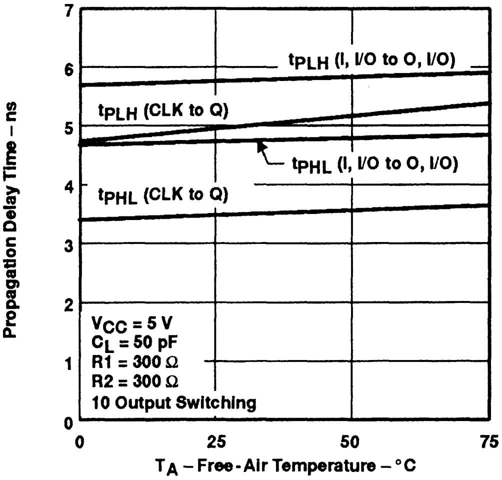


Figure 9

PROPAGATION DELAY TIME
vs
LOAD CAPACITANCE

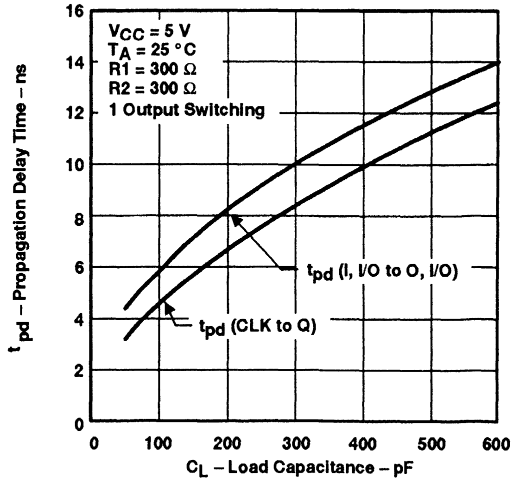


Figure 10

TYPICAL CHARACTERISTICS

WORST-CASE PROPAGATION DELAY TIME vs NUMBER OF OUTPUTS SWITCHING FK AND FN PACKAGES

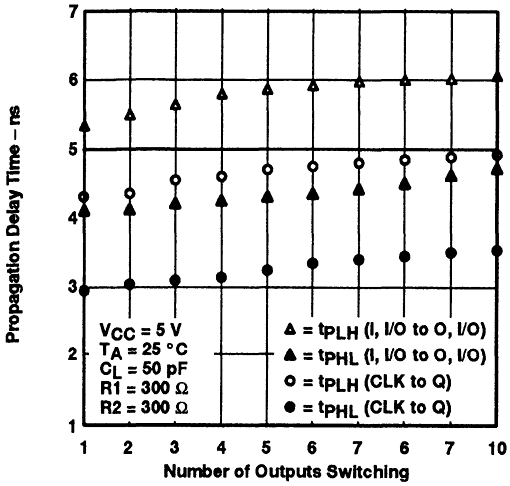


Figure 11

WORST-CASE PROPAGATION DELAY TIME vs NUMBER OF OUTPUTS SWITCHING JT AND NT PACKAGES

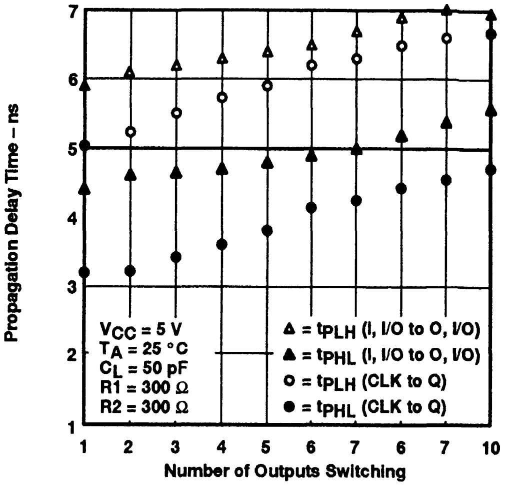


Figure 12

POWER DISSIPATION vs FREQUENCY 10-BIT COUNTER MODE

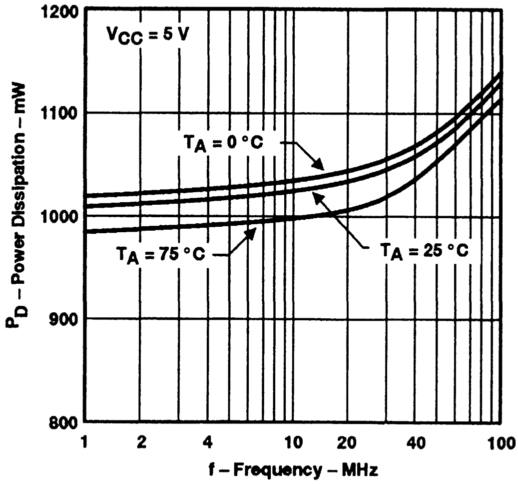


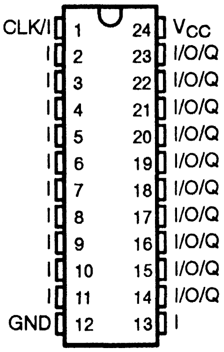
Figure 13

TIBPAL22V10-10C
HIGH-PERFORMANCE *IMPACT-X*™ PROGRAMMABLE ARRAY LOGIC CIRCUITS

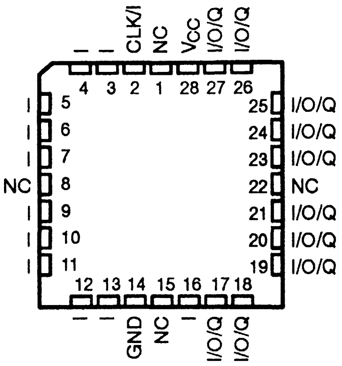
SRPS015 – D3972, FEBRUARY 1992

- **Second-Generation PLD Architecture**
- **High-Performance Operation:**
  f_{max} (External Feedback) . . . 71 MHz
  Propagation Delay . . . 10 ns Max
- **Increased Logic Power – Up to 22 Inputs and 10 Outputs**
- **Increased Product Terms – Average of 12 Per Output**
- **Variable Product Term Distribution Allows More Complex Functions to Be Implemented**
- **Each Output Is User Programmable for Registered or Combinational Operation, Polarity, and Output Enable Control**
- **Power-Up Clear on Registered Outputs**
- **TTL-Level Preload for Improved Testability**
- **Extra Terms Provide Logical Synchronous Set and Asynchronous Reset Capability**
- **Fast Programming, High Programming Yield, and Unsurpassed Reliability Ensured Using Ti-W Fuses**
- **AC and DC Testing Done at the Factory Utilizing Special Designed-In Test Features**
- **Dependable Texas Instruments Quality and Reliability**
- **Package Options Include Plastic Dual-In-Line and Chip Carrier Packages**

NT PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



NC — No internal connection
Pin assignments in operating mode

description

The TIBPAL22V10-10C is a programmable array logic device featuring high speed and functional equivalency when compared to presently available devices. They are implemented with the familiar sum-of-products (AND-OR) logic structure featuring the new concept "Programmable Output Logic Macrocell". These IMPACT-X™ circuits combine the latest Advanced Low-Power Schottky technology with proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional TTL logic.

These devices contain up to 22 inputs and 10 outputs. They incorporate the unique capability of defining and programming the architecture of each output on an individual basis. Outputs may be registered or nonregistered and inverting or noninverting as shown in the output logic macrocell diagram. The ten potential outputs are enabled through the use of individual product terms.

Further advantages can be seen in the introduction of variable product term distribution. This technique allocates from 8 to 16 logical product terms to each output for an average of 12 product terms per output. This variable allocation of terms allows far more complex functions to be implemented than in previously available devices.

This device is covered by U.S. Patent 4,410,987.
IMPACT-X is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 1992, Texas Instruments Incorporated

description (continued)

Circuit design is enhanced by the addition of a synchronous set and an asynchronous reset product term. These functions are common to all registers. When the synchronous set product term is a logic 1, the output registers are loaded with a logic 1 on the next low-to-high clock transition. When the asynchronous reset product term is a logic 1, the output registers are loaded with a logic 0. The output logic level after set or reset depends on the polarity selected during programming. Output registers can be preloaded to any desired state during testing. Preloading permits full logical verification during product testing.

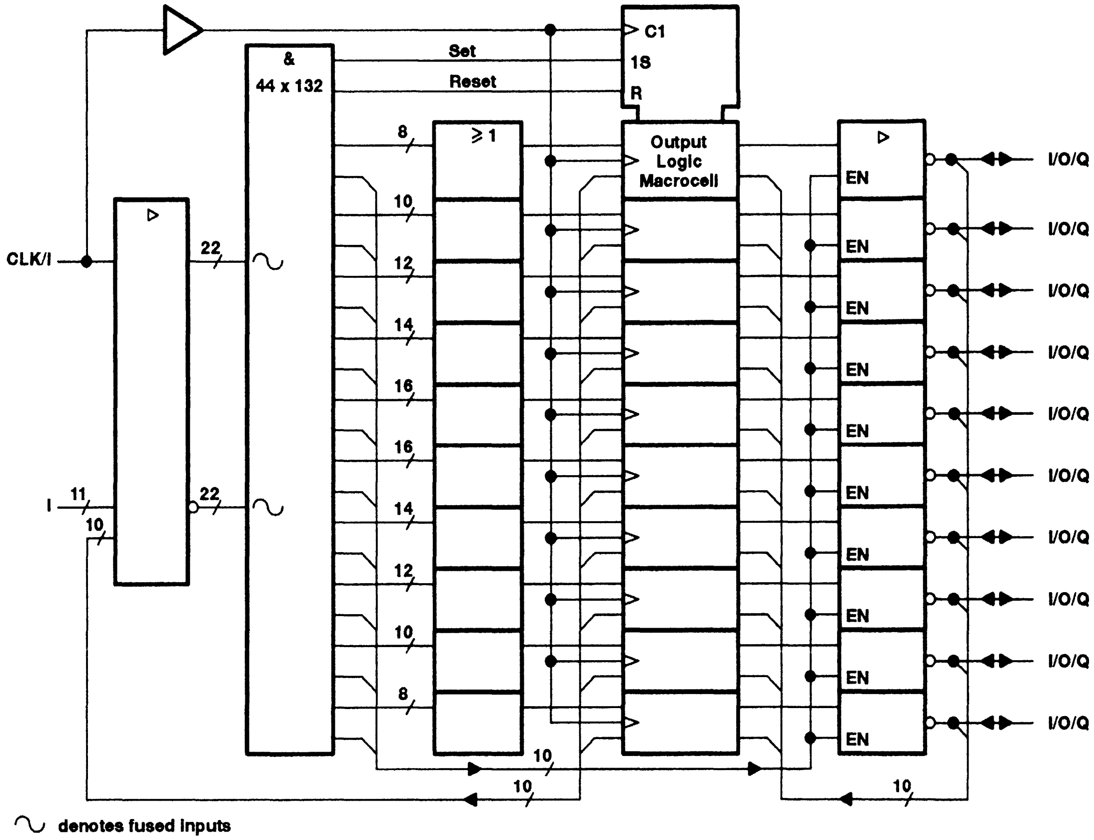
With features such as programmable output logic macrocells and variable product term distribution, the TIBPAL22V10-10C offers quick design and development of custom LSI functions with complexities of 500 to 800 equivalent gates. Since each of the ten output pins may be individually configured as inputs on either a temporary or permanent basis, functions requiring up to 21 inputs and a single output or down to 12 inputs and 10 outputs are possible.

A power-up clear function is supplied that forces all registered outputs to a predetermined state after power is applied to the device. Registered outputs selected as active-low power up with their outputs high. Registered outputs selected as active-high power up with their outputs low.

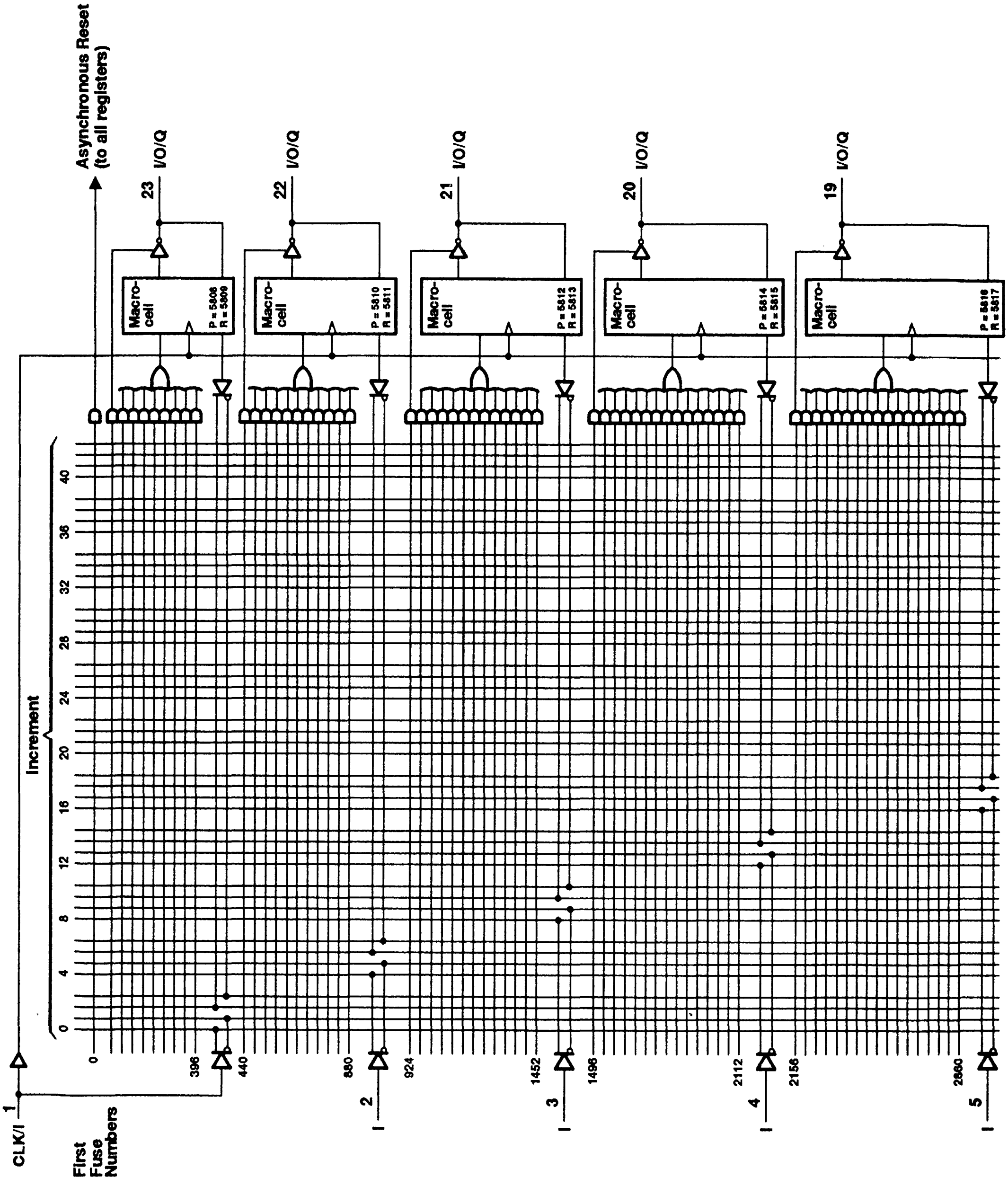
A single security fuse is provided on each device to discourage unauthorized copying of fuse patterns. Once blown, the verification circuitry is disabled and all other fuses will appear to be open.

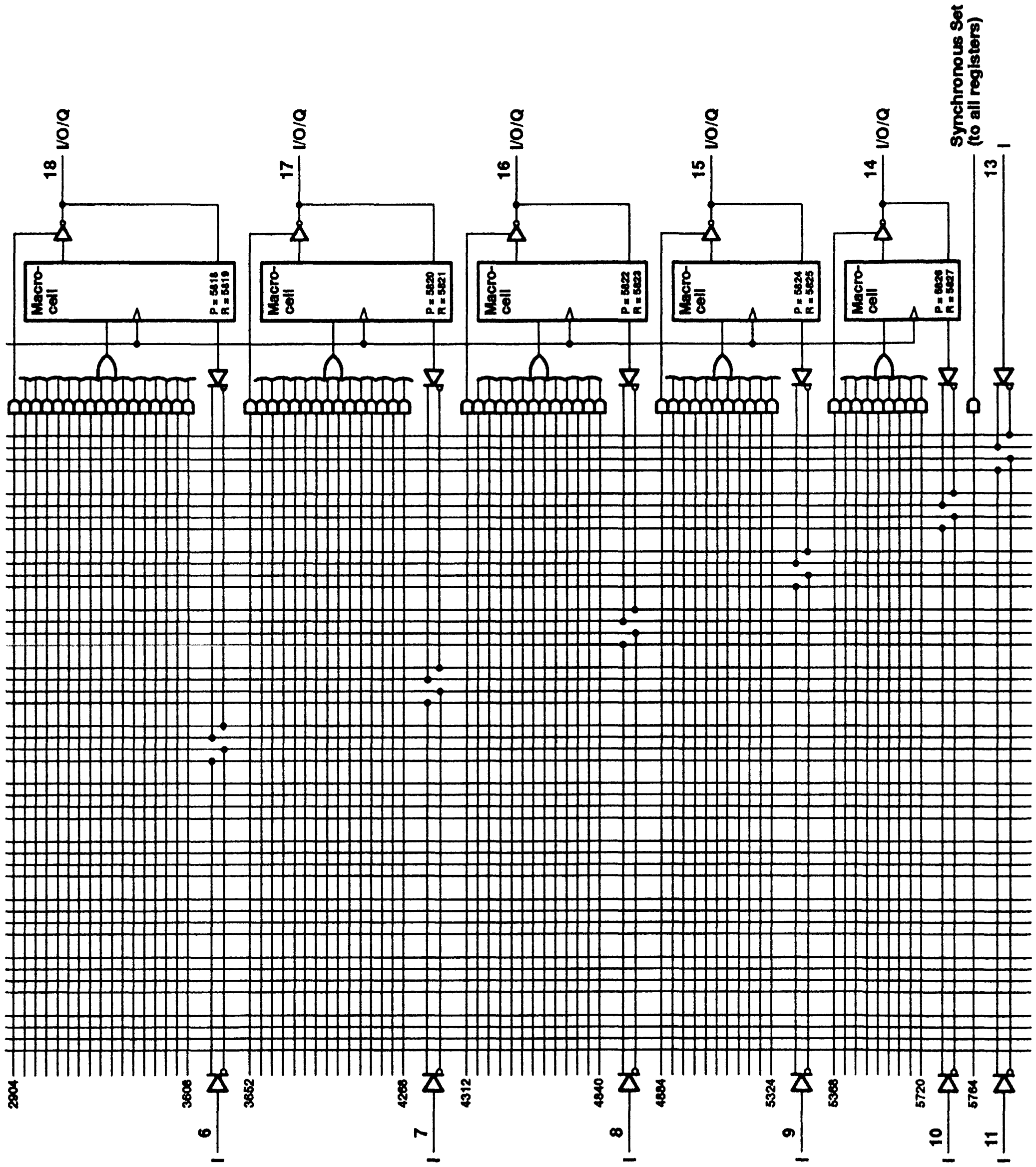
The TIBPAL22V10-10C is characterized for operation from 0°C to 75°C.

functional block diagram (positive logic)



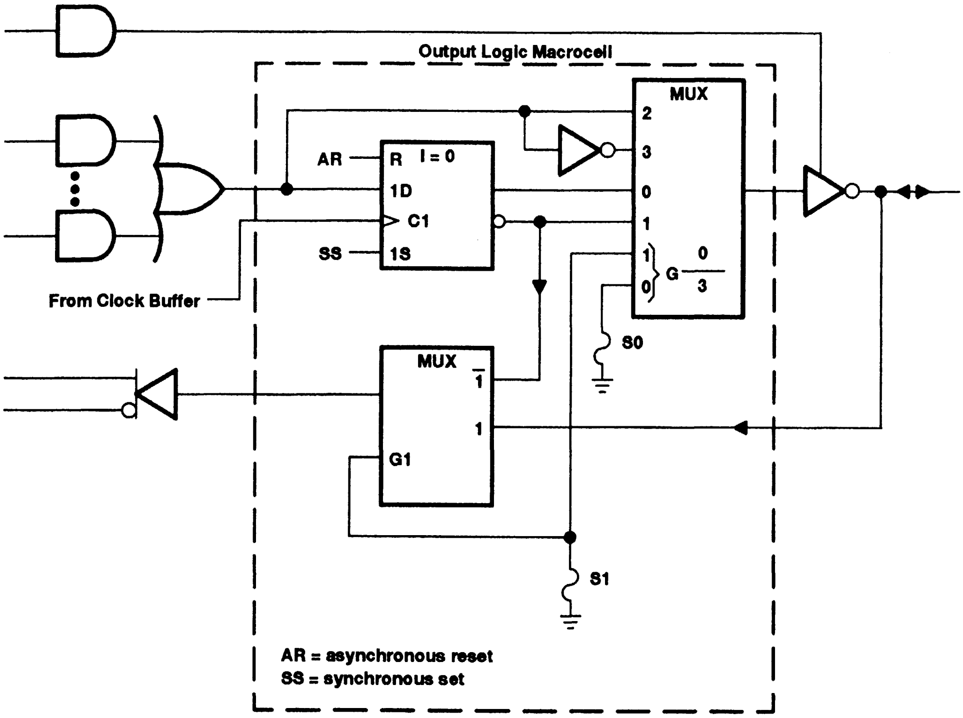
logic diagram (positive logic)

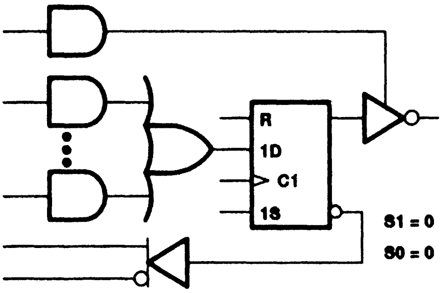




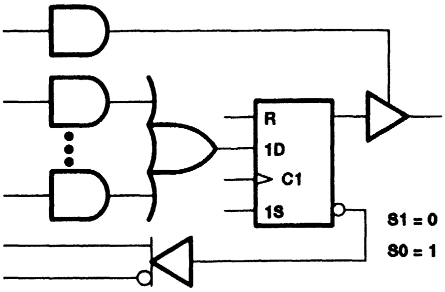
Fuse number = First Fuse number + Increment
Inside each MACROCELL the "P" fuse is the polarity fuse and the "R" fuse is the register fuse.

output logic macrocell diagram

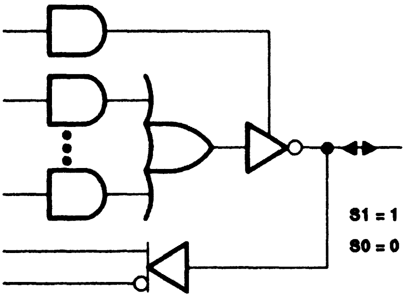




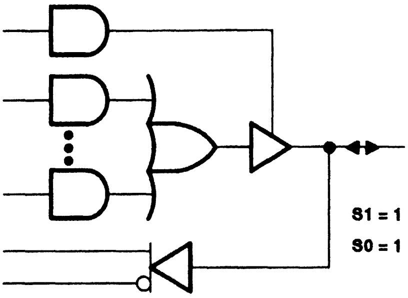
REGISTER FEEDBACK, REGISTERED, ACTIVE-LOW OUTPUT



REGISTER FEEDBACK, REGISTERED, ACTIVE-HIGH OUTPUT



I/O FEEDBACK, COMBINATIONAL, ACTIVE-LOW OUTPUT



I/O FEEDBACK, COMBINATIONAL, ACTIVE-HIGH OUTPUT

MACROCELL FEEDBACK AND OUTPUT FUNCTION TABLE

FUSE SELECT		FEEDBACK AND OUTPUT CONFIGURATION		
S1	S0			
0	0	Register feedback	Registered	Active low
0	1	Register feedback	Registered	Active high
1	0	I/O feedback	Combinational	Active low
1	1	I/O feedback	Combinational	Active high

0 = unblown fuse, 1 = blown fuse
S1 and S0 are select-function fuses as shown in the output logic macrocell diagram.

Figure 1. Resultant Macrocell Feedback and Output Logic After Programming

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) .... 7 V
Input voltage (see Note 1) .... −1.2 V to V_{CC} +0.5 V
Voltage range applied to disabled output (see Note 1) .... −0.5 V to V_{CC} +0.5 V
Operating free-air temperature range .... 0°C to 75°C
Storage temperature range .... −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle or during a preload cycle.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage (see Note 2)		2		5.5	V
V_{IL}	Low-level input voltage (see Note 2)				0.8	V
I_{OH}	High-level output current				−3.2	mA
I_{OL}	Low-level output current				16	mA
t_w	Pulse duration	Clock high or low	5			ns
		Asynchronous reset high or low	10			
t_{su}	Setup time before clock↑	Input	7			ns
		Feedback	7			
		Synchronous preset (active)	9			
		Synchronous preset (inactive)	8			
		Asynchronous reset (inactive)	8			
t_h	Hold time, input, set, or feedback after clock↑		0			ns
T_A	Operating free-air temperature		0		75	°C

NOTE 2: These are absolute voltage levels with respect to the ground pin of the device and includes all overshoots due to system and/or tester noise. Testing these parameters should not be attempted without suitable equipment.

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.75 V,	I_I = –18 mA				–1.2	V
V_{OH}		V_{CC} = 4.75 V,	I_{OH} = –3.2 mA		2.4			V
V_{OL}		V_{CC} = 4.75 V,	I_{OL} = 16 mA			0.35	0.5	V
I_{OZH}‡		V_{CC} = 5.25 V,	V_O = 2.7 V				0.1	mA
I_{OZL}‡		V_{CC} = 5.25 V,	V_O = 0.4 V				–0.1	mA
I_I		V_{CC} = 5.25 V,	V_I = 5.5 V				1	mA
I_{IH}‡		V_{CC} = 5.25 V,	V_I = 2.7 V				25	µA
I_{IL}	CLK	V_{CC} = 5.25 V,	V_I = 0.4 V				–0.25	mA
	All others						–0.1	
I_{OS}§		V_{CC} = 5.25 V,	V_O = 0.5 V		–30		–130	mA
I_{CC}		V_{CC} = 5.25 V,	V_I = GND,	Outputs open			210	mA
C_i	I	f = 1 MHz,	V_I = 2 V			6		pF
	CLK					6		
C_o		f = 1 MHz,	V_O = 2 V			8		pF

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ I/O leakage is the worst case of I_{OZL} and I_{IL} or I_{OZH} and I_{IH}, respectively.

§ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second. V_O is set at 0.5 V to avoid test problems caused by test equipment ground degradation.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	MAX	UNIT
f_{max}¶	Without feedback		R1 = 300 Ω, R2 = 300 Ω, See Figure 6	100		MHz
	With internal feedback (counter configuration)			80		
	With external feedback			71		
t_{pd}	I, I/O	I/O		1	10	ns
t_{pd}	I, I/O (reset)	Q			15	ns
t_{pd}	CLK	Q		1	7	ns
t_{pd}#	CLK	Feedback			5.5	ns
t_{en}	I, I/O	I/O, Q			11	ns
t_{dis}	I, I/O	I/O, Q			9	ns

¶ $$f_{max}\text{ (without feedback)} = \frac{1}{t_{w(low)} + t_{w(high)}}$$

$$f_{max}\text{ (with internal feedback)} = \frac{1}{t_{su} + t_{pd}\text{(CLK to feedback)}}$$

$$f_{max}\text{ (with external feedback)} = \frac{1}{t_{su} + t_{pd}\text{(CLK to Q)}}$$

This parameter is calculated from the measured f_{max} with internal feedback in the counter configuration.

preload procedure for registered outputs (see Notes 3 and 4)

The output registers can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below:

Step 1. With V_{CC} at 5 V and pin 1 at V_{IL}, raise pin 13 to V_{IHH}.
Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.
Step 3. Pulse pin 1, clocking in preload data.
Step 4. Remove output voltage, then lower pin 13 to V_{IL}. Preload can be verified by observing the voltage level at the output pin.

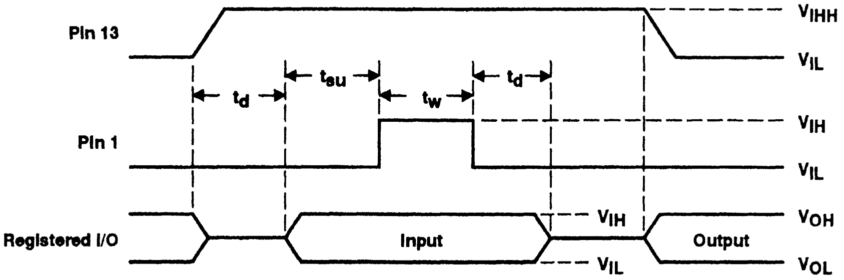
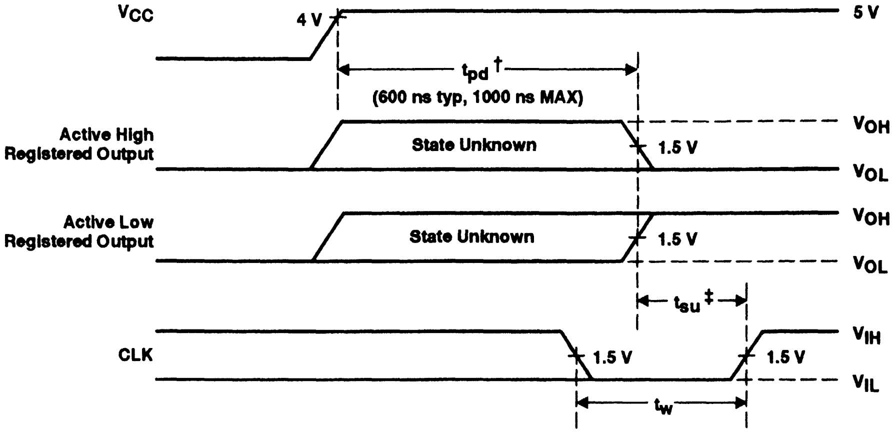


Figure 2. Preload Waveforms

NOTES: 3. Pin numbers shown are for the NT package only. If chip-carrier socket adapter is not used, pin numbers must be changed accordingly.
4. $t_d = t_{su} = t_w$ = 100 ns to 1000 ns. V_{IHH} = 10.25 V to 10.75 V.

power-up reset

Following power up, all registers are reset to zero. The output level depends on the polarity selected during programming. This feature provides extra flexibility to the system designer and is especially valuable in simplifying state-machine initialization. To ensure a valid power-up reset, it is important that the rise of V_{CC} be monotonic. Following power-up reset, a low-to-high clock transition must not occur until all applicable input and feedback setup times are met.



† This is the power-up reset time and applies to registered outputs only. The values shown are from characterization data.
‡ This is the setup time for input or feedback.

Figure 3. Power-Up Reset Waveforms

programming information

Texas Instruments programmable logic devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments programmable logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

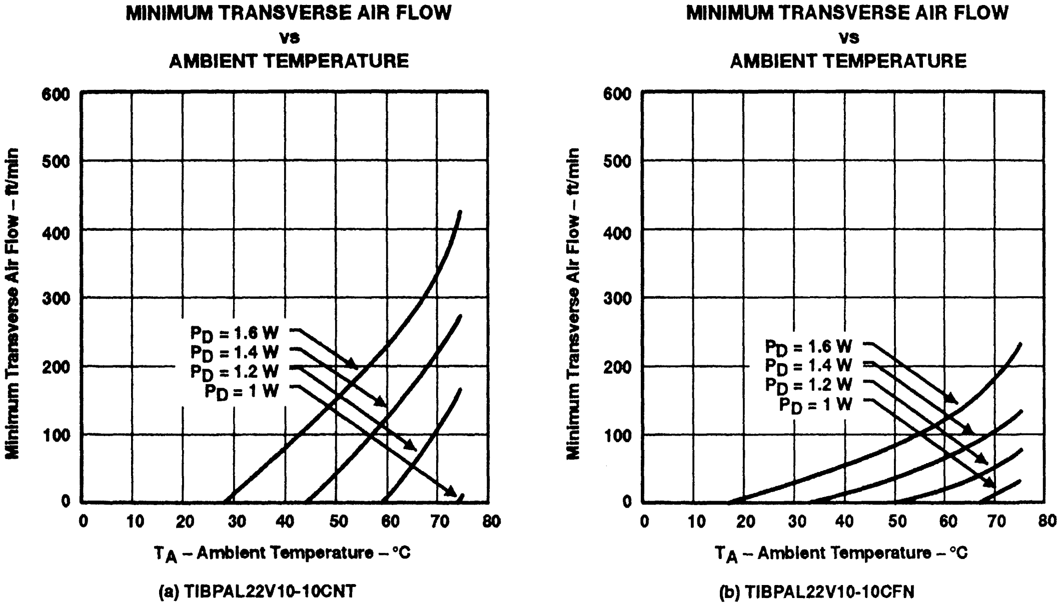
THERMAL INFORMATION

thermal management of the TIBPAL22V10-10C

Thermal management of the TIBPAL22V10-10CNT and TIBPAL22V10-10CFN is necessary when operating at certain conditions of frequency, output loading, and outputs switching simultaneously. The device and system application will determine the appropriate level of management.

Determining the level of thermal management is based on factors such as power dissipation (P_D), ambient temperature (T_A), and transverse airflow (FPM). Figures 4 (a) and 4 (b) show the relationship between ambient temperature and transverse airflow at given power dissipation levels. The required transverse airflow can be determined at a particular ambient temperature and device power dissipation level in order to ensure the device specifications.

Figure 5 illustrates how power dissipation varies as a function of frequency and the number of outputs switching simultaneously. It should be noted that all outputs are fully loaded (C_L = 50 pF). Since the condition of eight fully loaded outputs represents the worst-case condition, each application must be evaluated accordingly.



(a) TIBPAL22V10-10CNT

(b) TIBPAL22V10-10CFN

Figure 4

THERMAL INFORMATION

POWER DISSIPATION vs FREQUENCY

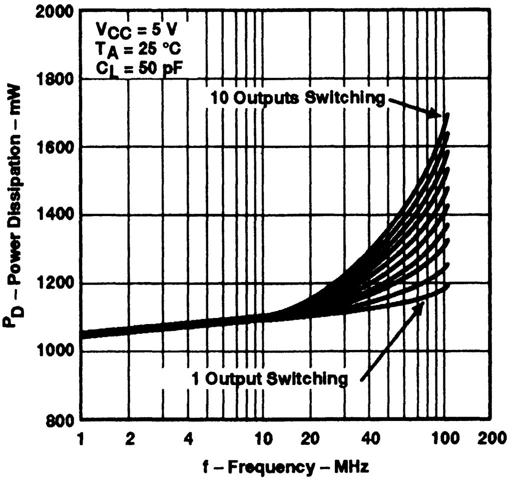
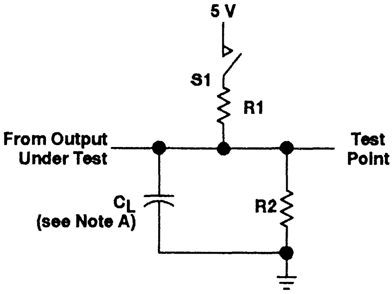
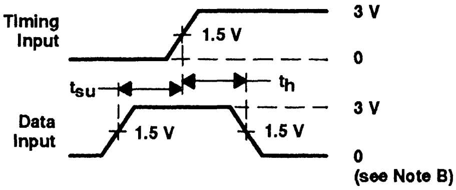


Figure 5

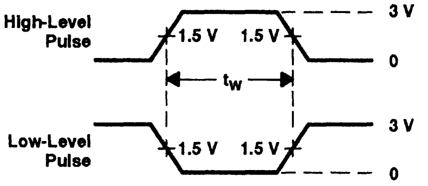
PARAMETER MEASUREMENT INFORMATION



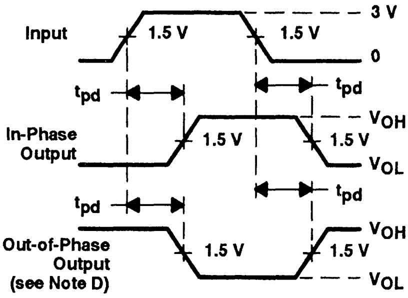
LOAD CIRCUIT FOR
3-STATE OUTPUTS



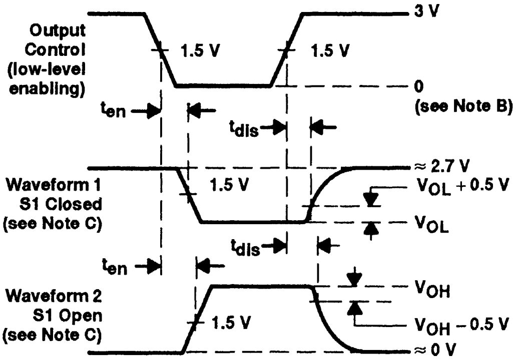
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
B. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.
E. Equivalent loads may be used for testing.

Figure 6. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

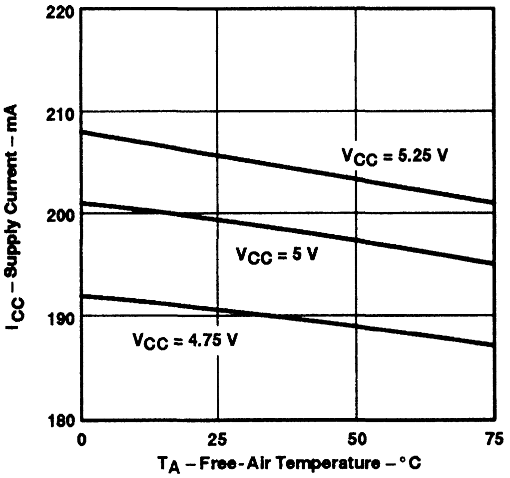


Figure 7

PROPAGATION DELAY TIME
vs
SUPPLY VOLTAGE

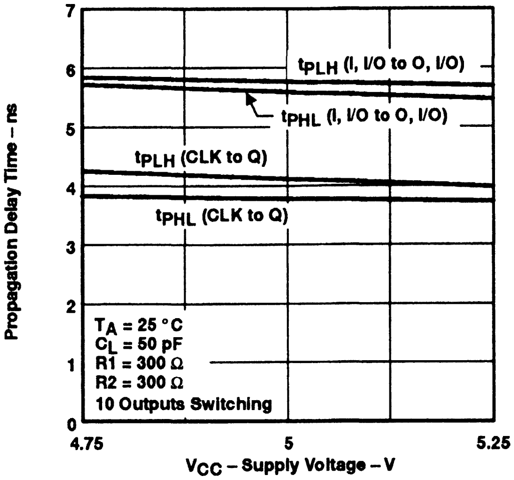


Figure 8

PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

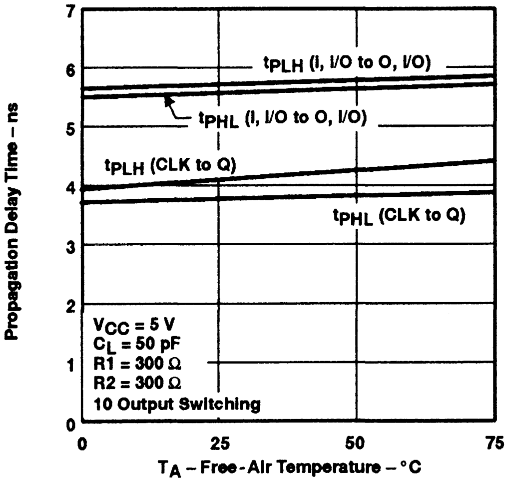


Figure 9

PROPAGATION DELAY TIME
vs
LOAD CAPACITANCE

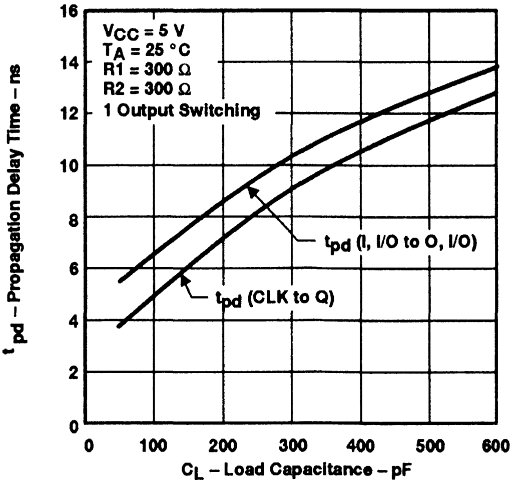


Figure 10

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME
vs
NUMBER OF OUTPUTS SWITCHING

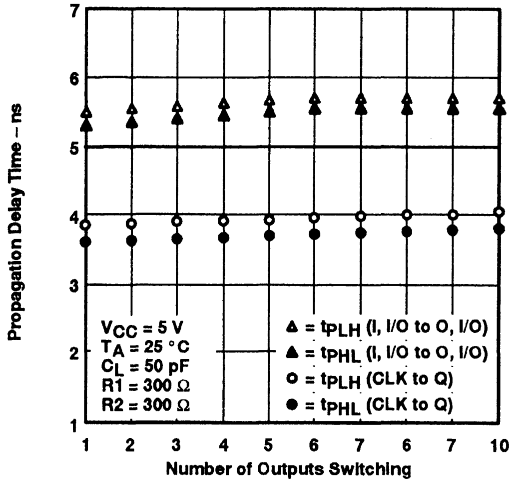


Figure 11

POWER DISSIPATION
vs
FREQUENCY
10-BIT COUNTER MODE

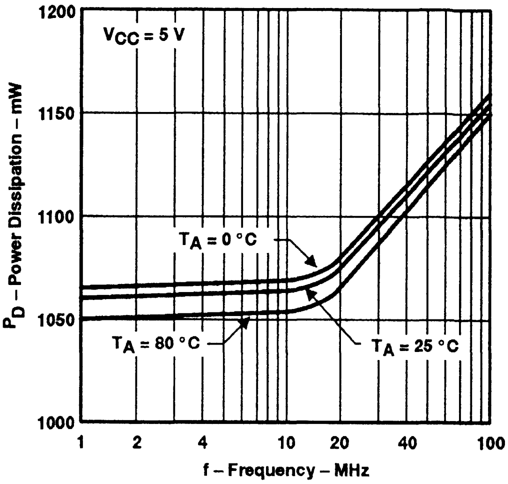


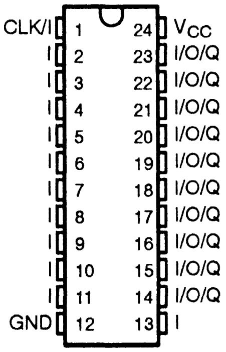
Figure 12

TIBPAL22V10-15BC
HIGH-PERFORMANCE *IMPACT-X*™ PROGRAMMABLE ARRAY LOGIC CIRCUITS

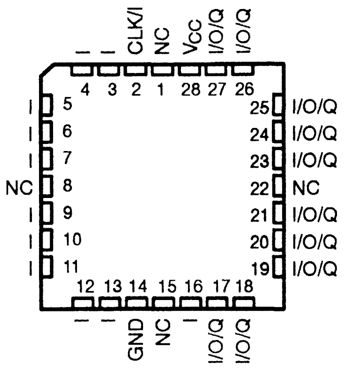
SRPS009A – D3356, OCTOBER 1989 – REVISED JUNE 1990

- **Second-Generation PLD Architecture**
- **High-Performance Operation:**
  f_{max} (External Feedback) . . . 40 MHz
  Propagation Delay . . . 15 ns Max
- **Increased Logic Power – Up to 22 Inputs and 10 Outputs**
- **Increased Product Terms – Average of 12 per Output**
- **Variable Product Term Distribution Allows More Complex Functions to Be Implemented**
- **Each Output Is User Programmable for Registered or Combinational Operation, Polarity, and Output Enable Control**
- **Power-Up Clear on Registered Outputs**
- **TTL-Level Preload for Improved Testability**
- **Extra Terms Provide Logical Synchronous Set and Asynchronous Reset Capability**
- **Fast Programming, High Programming Yield, and Unsurpassed Reliability Ensured Using Ti-W Fuses**
- **AC and DC Testing Done at the Factory Utilizing Special Designed-In Test Features**
- **Dependable Texas Instruments Quality and Reliability**
- **Package Options Include Plastic Dual-In-Line and Chip Carrier Packages**

NT PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



NC – No internal connection
Pin assignments in operating mode

description

The TIBPAL22V10-15BC is a programmable array logic device featuring high speed and functional equivalency when compared to presently available devices. They are implemented with the familiar sum-of-products (AND-OR) logic structure featuring the new concept "Programmable Output Logic Macrocell". These IMPACT-X™ circuits combine the latest Advanced Low-Power Schottky technology with proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional TTL logic.

These devices contain up to 22 inputs and 10 outputs. They incorporate the unique capability of defining and programming the architecture of each output on an individual basis. Outputs may be registered or nonregistered and inverting or noninverting as shown in the output logic macrocell diagram. The ten potential outputs are enabled through the use of individual product terms.

Further advantages can be seen in the introduction of variable product term distribution. This technique allocates from 8 to 16 logical product terms to each output for an average of 12 product terms per output. This variable allocation of terms allows far more complex functions to be implemented than in previously available devices.

This device is covered by U.S. Patent 4,410,987.
IMPACT-X is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 1990, Texas Instruments Incorporated

TEXAS INSTRUMENTS

description (continued)

Circuit design is enhanced by the addition of a synchronous set and an asynchronous reset product term. These functions are common to all registers. When the synchronous set product term is a logic 1, the output registers are loaded with a logic 1 on the next low-to-high clock transition. When the asynchronous reset product term is a logic 1, the output registers are loaded with a logic 0. The output logic level after set or reset depends on the polarity selected during programming. Output registers can be preloaded to any desired state during testing. Preloading permits full logical verification during product testing.

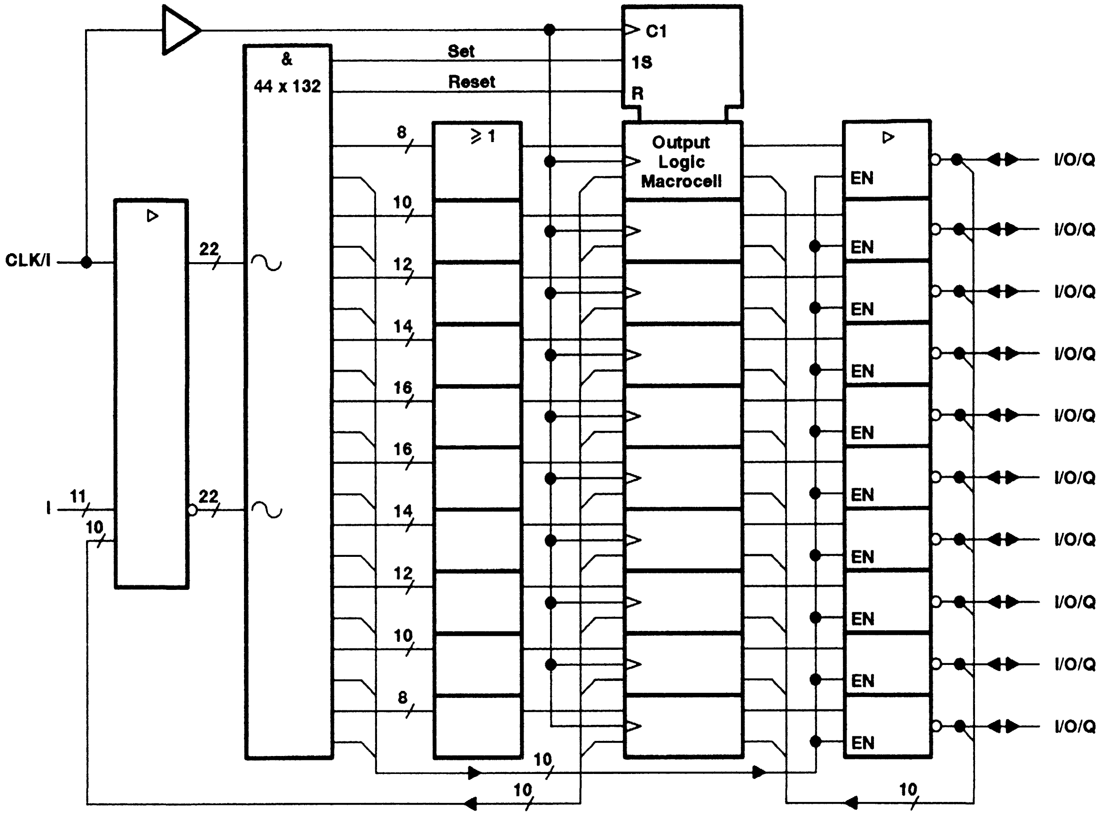
With features such as programmable output logic macrocells and variable product term distribution, the TIBPAL22V10-15BC offers quick design and development of custom LSI functions with complexities of 500 to 800 equivalent gates. Since each of the ten output pins may be individually configured as inputs on either a temporary or permanent basis, functions requiring up to 21 inputs and a single output or down to 12 inputs and 10 outputs are possible.

A power-up clear function is supplied that forces all registered outputs to a predetermined state after power is applied to the device. Registered outputs selected as active-low power up with their outputs high. Registered outputs selected as active-high power up with their outputs low.

A single security fuse is provided on each device to discourage unauthorized copying of fuse patterns. Once blown, the verification circuitry is disabled and all other fuses will appear to be open.

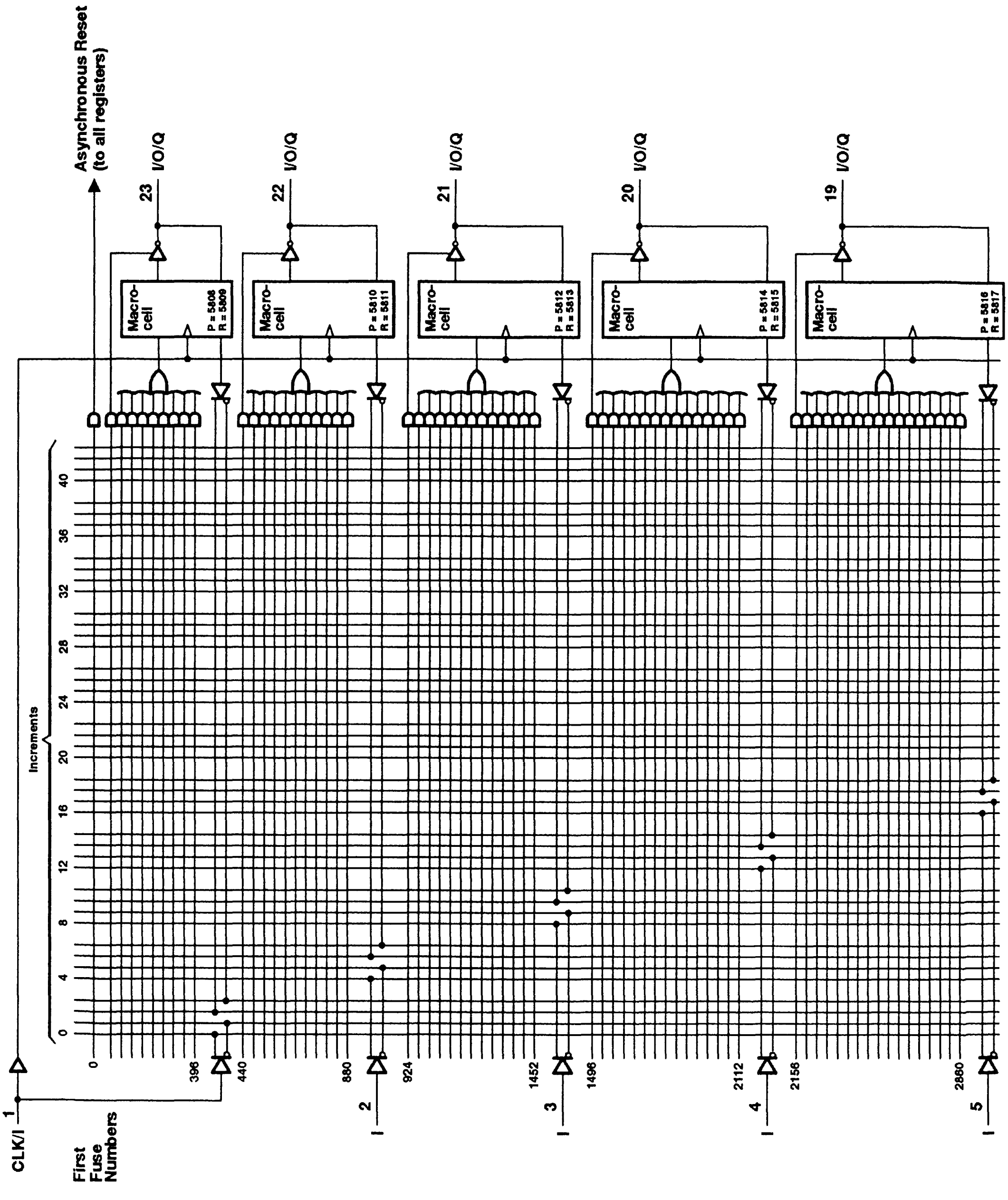
The TIBPAL22V10-15BC is characterized for operation from 0°C to 75°C.

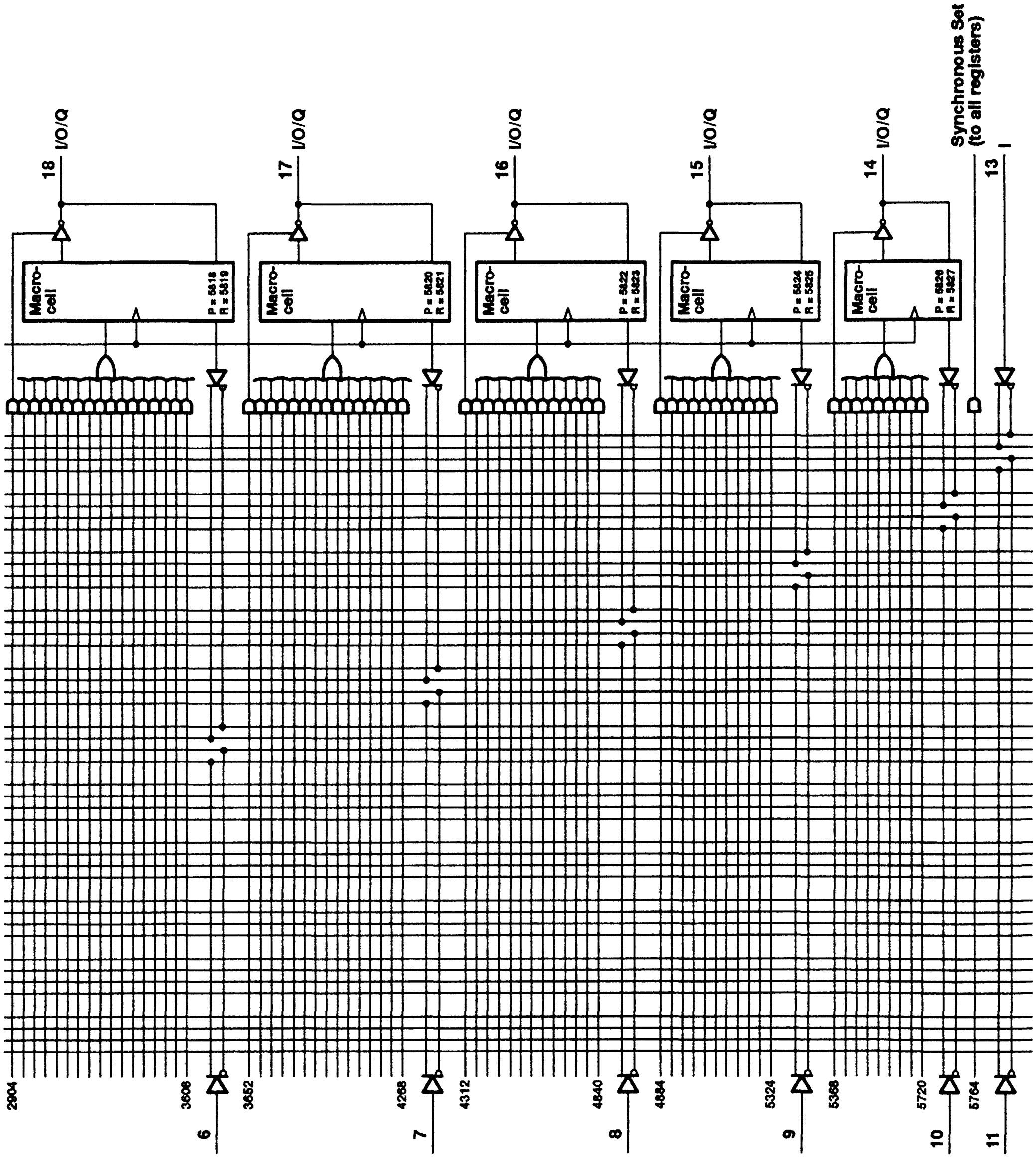
functional block diagram (positive logic)



∿ denotes fused inputs

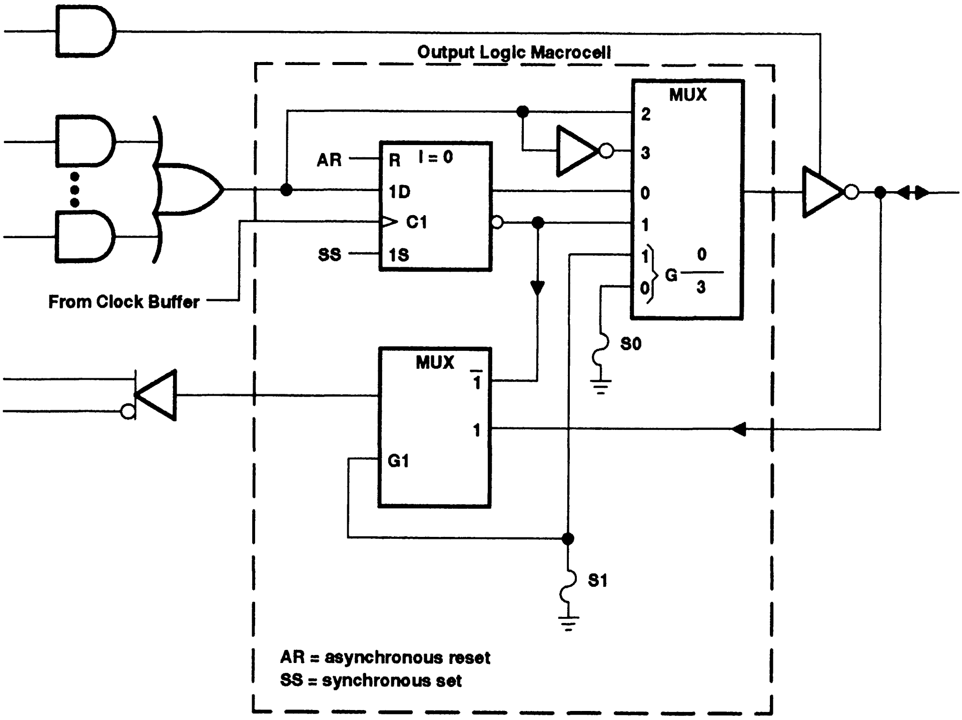
logic symbol (positive logic)

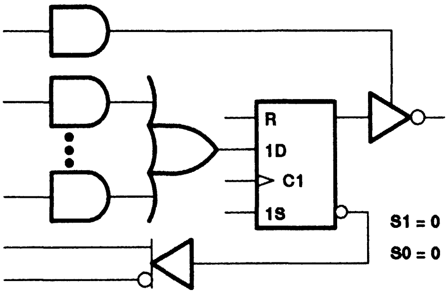




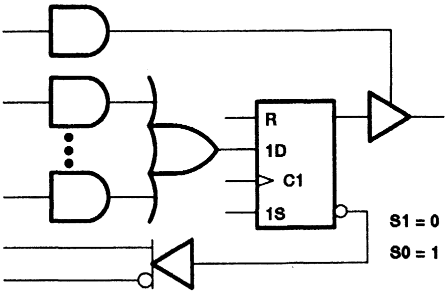
Fuse number = First fuse number + Increment
Inside each MACROCELL the "P" fuse is the polarity fuse and the "R" fuse is the register fuse.

output logic macrocell diagram

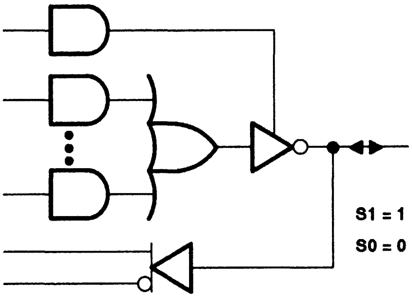




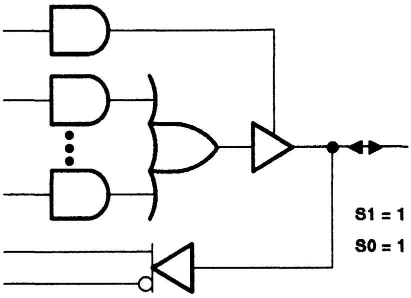
REGISTER FEEDBACK, REGISTERED, ACTIVE-LOW OUTPUT



REGISTER FEEDBACK, REGISTERED, ACTIVE-HIGH OUTPUT



I/O FEEDBACK, COMBINATIONAL, ACTIVE-LOW OUTPUT



I/O FEEDBACK, COMBINATIONAL, ACTIVE-HIGH OUTPUT

MACROCELL FEEDBACK AND OUTPUT FUNCTION TABLE

FUSE SELECT		FEEDBACK AND OUTPUT CONFIGURATION		
S1	S0			
0	0	Register feedback	Registered	Active low
0	1	Register feedback	Registered	Active high
1	0	I/O feedback	Combinational	Active low
1	1	I/O feedback	Combinational	Active high

0 = unblown fuse, 1 = blown fuse

S1 and S0 are select-function fuses as shown in the output logic macrocell diagram.

Figure 1. Resultant Macrocell Feedback and Output Logic After Programming

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) .... 7 V
Input voltage (see Note 1) .... 5.5 V
Voltage applied to disabled output (see Note 1) .... 5.5 V
Operating free-air temperature range .... 0°C to 75°C
Storage temperature range .... −65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle or during a preload cycle.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−3.2	mA
I_{OL}	Low-level output current				16	mA
t_w	Pulse duration	Clock high or low	10			ns
		Asynchronous Reset high or low	15			
t_{su}	Setup time before clock↑	Input	13			ns
		Feedback	13			
		Synchronous Preset (active)	13			
		Asynchronous Reset (inactive)	15			
t_h	Hold time, input, set, or feedback after clock↑		0			ns
T_A	Operating free-air temperature		0		75	°C

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		$V_{CC} = 4.75$ V,	$I_I = -18$ mA				−1.2	V
V_{OH}		$V_{CC} = 4.75$ V,	$I_{OH} = -3.2$ mA		2.4	3.5		V
V_{OL}		$V_{CC} = 4.75$ V,	$I_{OL} = 16$ mA			0.35	0.5	V
I_{OZH}		$V_{CC} = 5.25$ V,	$V_O = 2.7$ V				0.1	mA
I_{OZL}		$V_{CC} = 5.25$ V,	$V_O = 0.4$ V				−0.1	mA
I_I		$V_{CC} = 5.25$ V,	$V_I = 5.5$ V				1	mA
I_{IH}		$V_{CC} = 5.25$ V,	$V_I = 2.7$ V				25	μA
I_{IL}	CLK	$V_{CC} = 5.25$ V,	$V_I = 0.4$ V				−0.15	mA
	All others						−0.1	
I_{OS}‡		$V_{CC} = 5.25$ V,	$V_O = 0.5$ V		−30		−90	mA
I_{CC}		$V_{CC} = 5.25$ V,	$V_I = \text{GND}$,	Outputs open		155	180	mA
C_i		f = 1 MHz,	$V_I = 2$ V			5.5		pF
C_o		f = 1 MHz,	$V_O = 2$ V			8		pF
C_{clk}		f = 1 MHz,	$V_{CLK} = 2$ V			7		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	TYP†	MAX	UNIT
f_{max}§	External feedback		R1 = 300 Ω, R2 = 390 Ω, See Figure 4	40	60		MHz
t_{pd}	I, I/O	I/O			11	15	ns
t_{pd}	I, I/O (reset)	Q			13	20	ns
t_{pd}	CLK	Q			7	12	ns
t_{pd}	CLK	I/O			15	22	ns
t_{en}	I, I/O	I/O, Q			11	15	ns
t_{dis}	I, I/O	I/O, Q			11	15	ns

† All typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second. V_O is set at 0.5 V to avoid test problems caused by test equipment ground degradation.

§ f_{max} (with feedback) $= \dfrac{1}{t_{su} + t_{pd}(\text{CLK to Q})}$.

preload procedure for registered outputs (see Notes 2 and 3)

The output registers can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below:

Step 1. With V_{CC} at 5 V and pin 1 at V_{IL}, raise pin 13 to V_{IHH}.
Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.
Step 3. Pulse pin 1, clocking in preload data.
Step 4. Remove output voltage, then lower pin 13 to V_{IL}. Preload can be verified by observing the voltage level at the output pin.

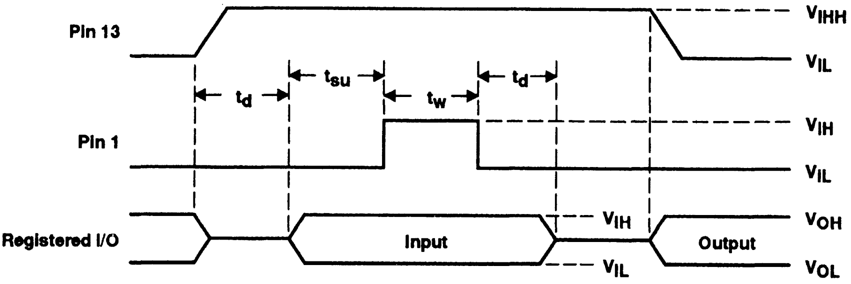
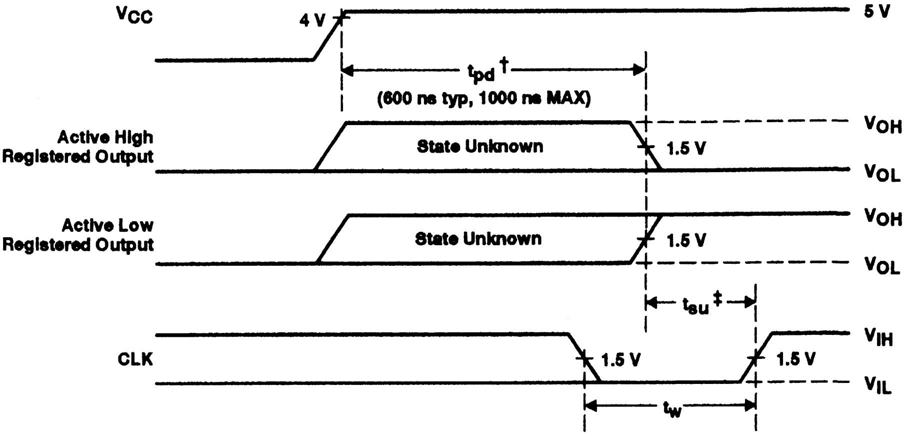


Figure 2. Preload Waveforms

NOTES: 2. Pin numbers shown are for the NT package only. If chip-carrier socket adapter is not used, pin numbers must be changed accordingly.
3. $t_d = t_{su} = t_w$ = 100 ns to 1000 ns. V_{IHH} = 10.25 V to 10.75 V.

power-up reset

Following power up, all registers are reset to zero. The output level depends on the polarity selected during programming. This feature provides extra flexibility to the system designer and is especially valuable in simplifying state-machine initialization. To ensure a valid power-up reset, it is important that the rise of V_{CC} be monotonic. Following power-up reset, a low-to-high clock transition must not occur until all applicable input and feedback setup times are met.



† This is the power-up reset time and applies to registered outputs only. The values shown are from characterization data.
‡ This is the setup time for input or feedback.

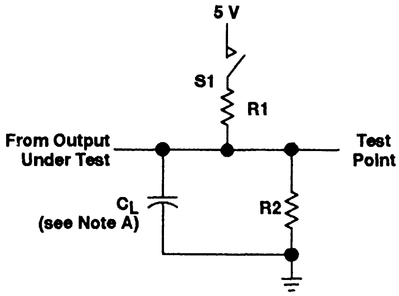
Figure 3. Power-Up Reset Waveforms

programming information

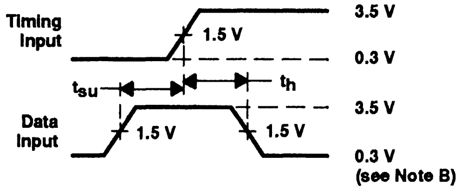
Texas Instruments programmable logic devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments programmable logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

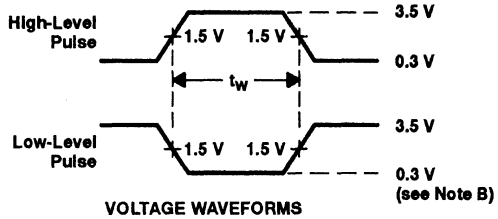
PARAMETER MEASUREMENT INFORMATION



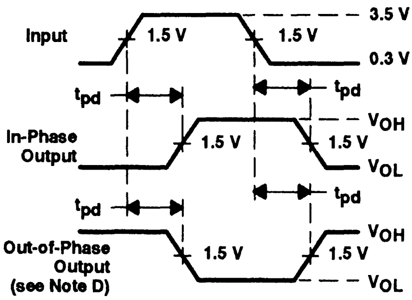
LOAD CIRCUIT FOR
3-STATE OUTPUTS



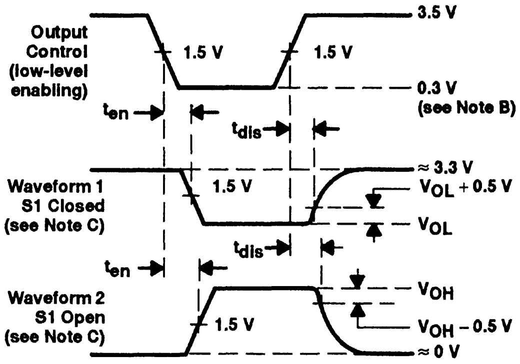
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.

B. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.

E. Equivalent loads may be used for testing.

Figure 4. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

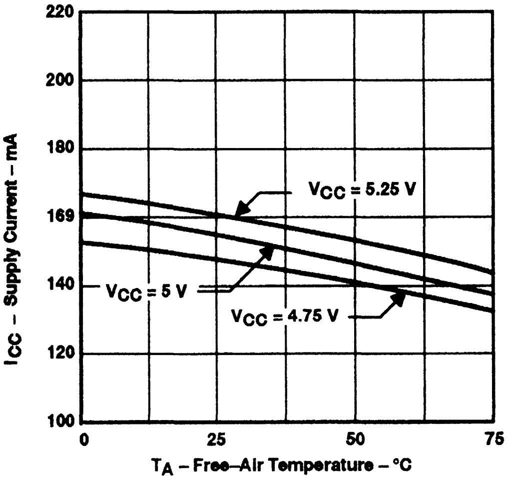

SUPPLY CURRENT vs FREE–AIR TEMPERATURE

Figure 5

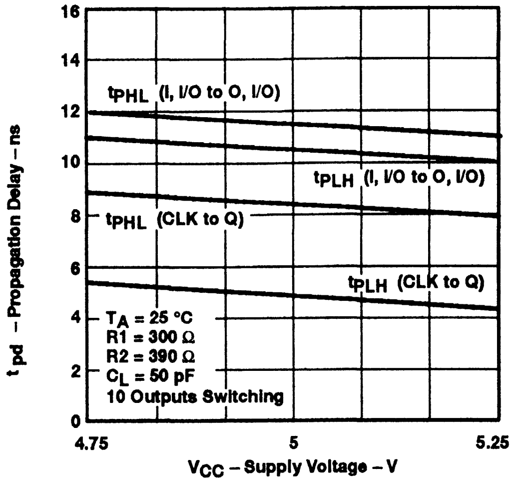

PROPAGATION DELAY TIME vs SUPPLY VOLTAGE

Figure 6

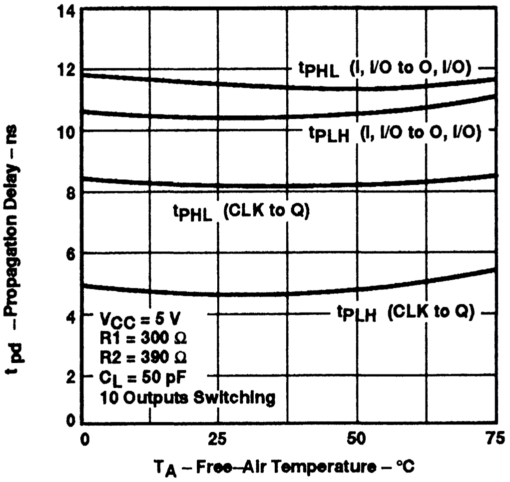

PROPAGATION DELAY TIME vs FREE–AIR TEMPERATURE

Figure 7

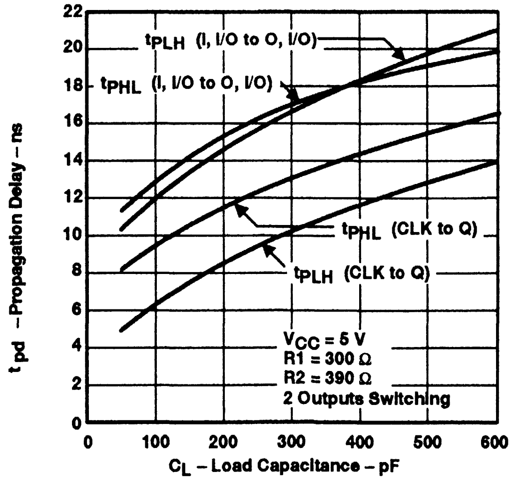

PROPAGATION DELAY TIME vs LOAD CAPACITANCE

Figure 8

TYPICAL CHARACTERISTICS

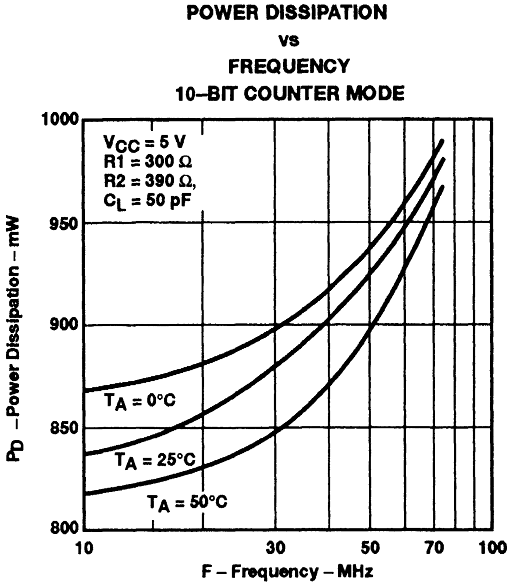


Figure 9

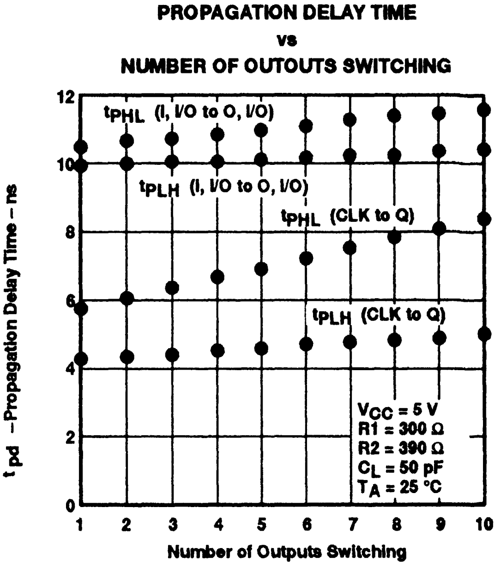


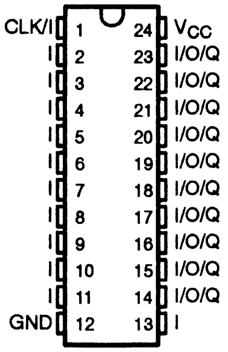
Figure 10

TIBPAL22V10-20M
HIGH-PERFORMANCE *IMPACT-X*™ PROGRAMMABLE ARRAY LOGIC CIRCUITS

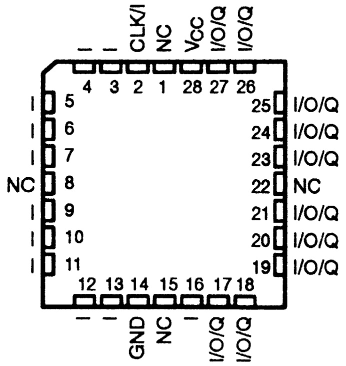
SRPS012A – D3523, JUNE 1990 – REVISED MARCH 1992

- **Second-Generation PLD Architecture**
- **High-Performance Operation:**
  f_{max} (External Feedback) . . . 33.3 MHz
  Propagation Delay . . . 20 ns Max
- **Increased Logic Power – Up to 22 Inputs and 10 Outputs**
- **Increased Product Terms – Average of 12 per Output**
- **Variable Product Term Distribution Allows More Complex Functions to Be Implemented**
- **Each Output Is User Programmable for Registered or Combinational Operation, Polarity, and Output Enable Control**
- **Power-Up Clear on Registered Outputs**
- **TTL-Level Preload for Improved Testability**
- **Extra Terms Provide Logical Synchronous Set and Asynchronous Reset Capability**
- **Fast Programming, High Programming Yield, and Unsurpassed Reliability Ensured Using Ti-W Fuses**
- **AC and DC Testing Done at the Factory Utilizing Special Designed-In Test Features**
- **Dependable Texas Instruments Quality and Reliability**
- **Package Options Include Plastic Dual-In-Line and Chip Carrier Packages**

JT PACKAGE
(TOP VIEW)



FK PACKAGE
(TOP VIEW)



NC – No internal connection
Pin assignments in operating mode

description

The TIBPAL22V10-20M is a programmable array logic device featuring high speed and functional equivalency when compared to presently available devices. They are implemented with the familiar sum-of-products (AND-OR) logic structure featuring the new concept "Programmable Output Logic Macrocell". These IMPACT-X™ circuits combine the latest Advanced Low-Power Schottky technology with proven titanium-tungsten fuses to provide reliable, high-performance substitutes for conventional TTL logic.

These devices contain up to 22 inputs and 10 outputs. They incorporate the unique capability of defining and programming the architecture of each output on an individual basis. Outputs may be registered or nonregistered and inverting or noninverting as shown in the output logic macrocell diagram. The ten potential outputs are enabled through the use of individual product terms.

Further advantages can be seen in the introduction of variable product term distribution. This technique allocates from 8 to 16 logical product terms to each output for an average of 12 product terms per output. This variable allocation of terms allows far more complex functions to be implemented than in previously available devices.

This device is covered by U.S. Patent 4,410,987.
IMPACT-X is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 1992, Texas Instruments Incorporated

TEXAS
INSTRUMENTS

description (continued)

Circuit design is enhanced by the addition of a synchronous set and an asynchronous reset product term. These functions are common to all registers. When the synchronous set product term is a logic 1, the output registers are loaded with a logic 1 on the next low-to-high clock transition. When the asynchronous reset product term is a logic 1, the output registers are loaded with a logic 0. The output logic level after set or reset depends on the polarity selected during programming. Output registers can be preloaded to any desired state during testing. Preloading permits full logical verification during product testing.

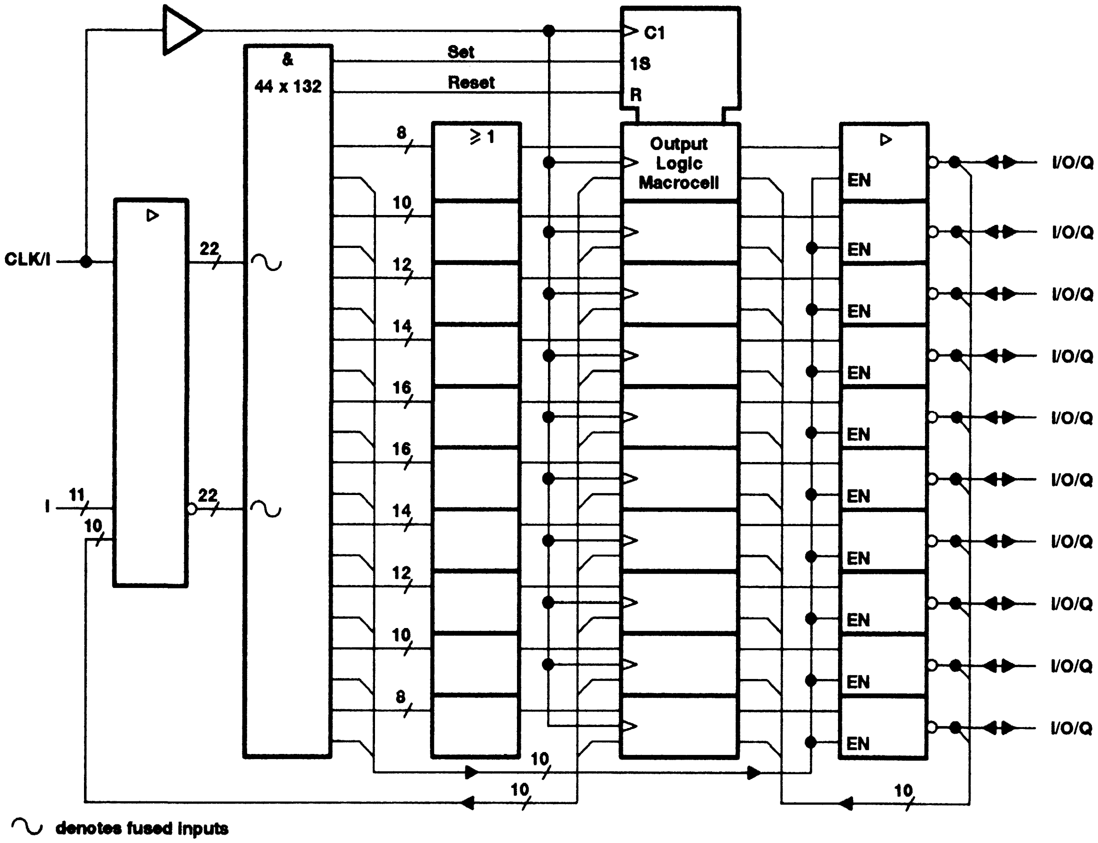
With features such as programmable output logic macrocells and variable product term distribution, the TIBPAL22V10-20M offers quick design and development of custom LSI functions with complexities of 500 to 800 equivalent gates. Since each of the ten output pins may be individually configured as inputs on either a temporary or permanent basis, functions requiring up to 21 inputs and a single output or down to 12 inputs and 10 outputs are possible.

A power-up clear function is supplied that forces all registered outputs to a predetermined state after power is applied to the device. Registered outputs selected as active-low power up with their outputs high. Registered outputs selected as active-high power up with their outputs low.

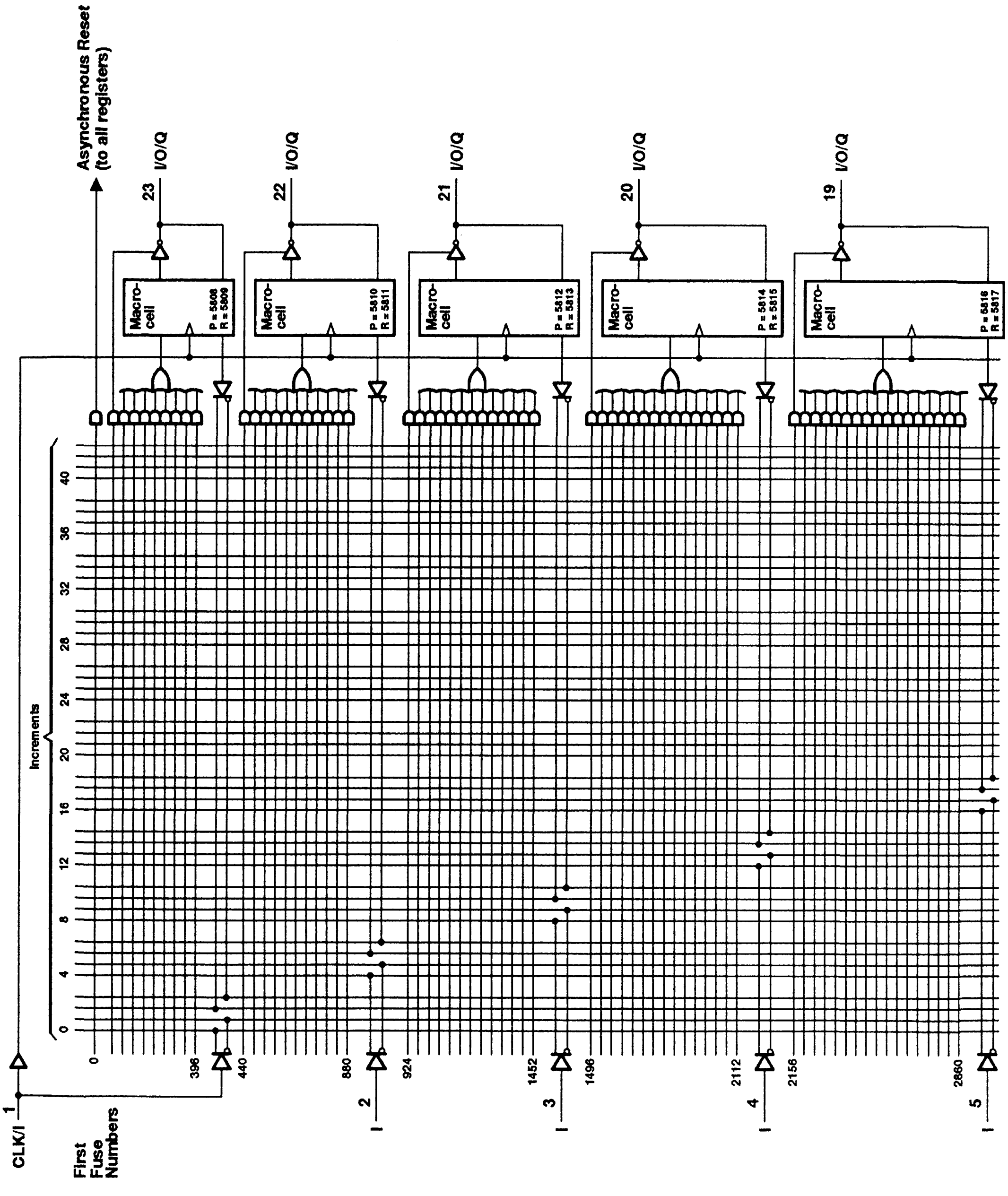
A single security fuse is provided on each device to discourage unauthorized copying of fuse patterns. Once blown, the verification circuitry is disabled and all other fuses will appear to be open.

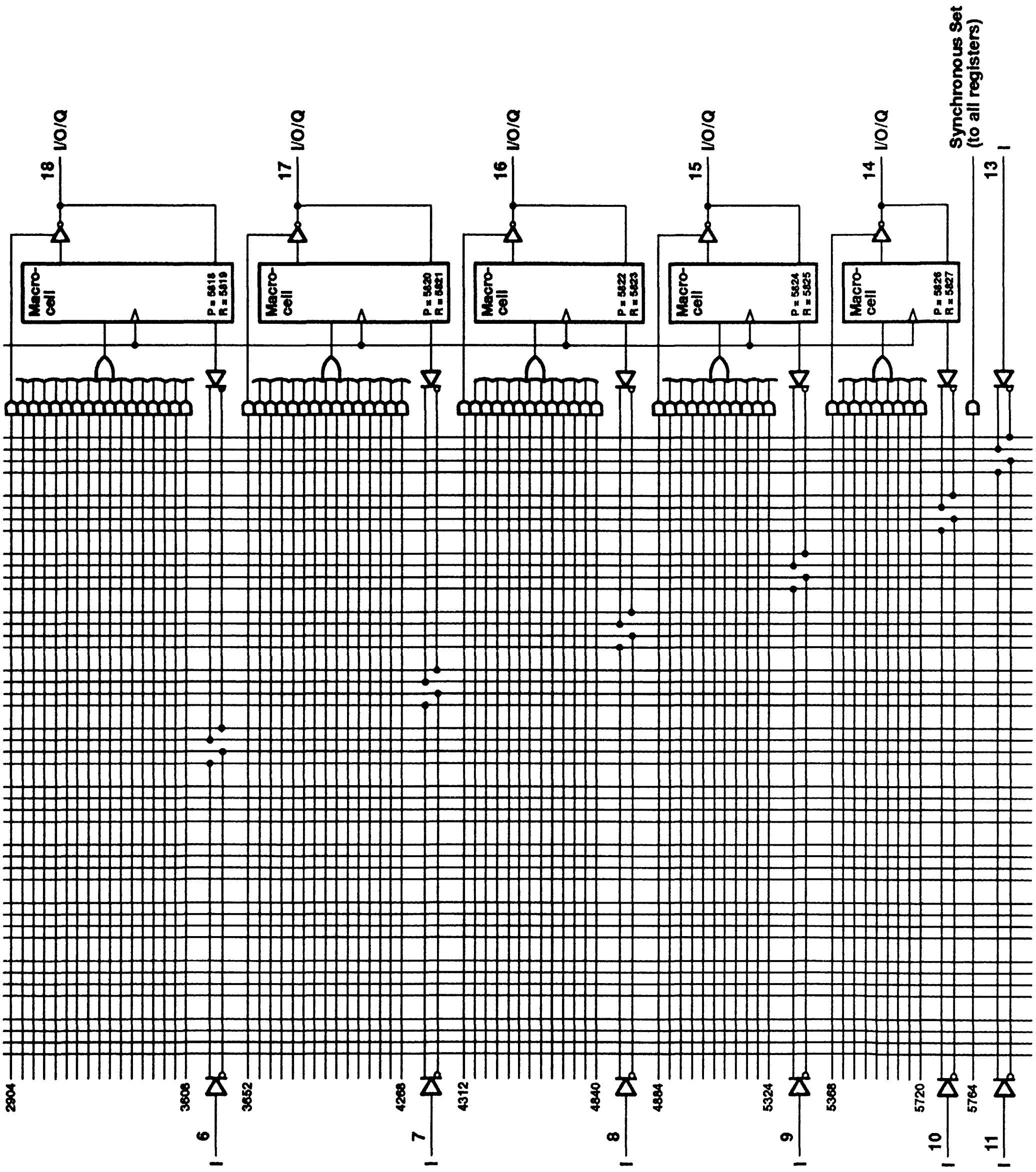
The TIBPAL22V10-20M is characterized for operation over the full military temperature range of –55°C to 125°C.

functional block diagram (positive logic)



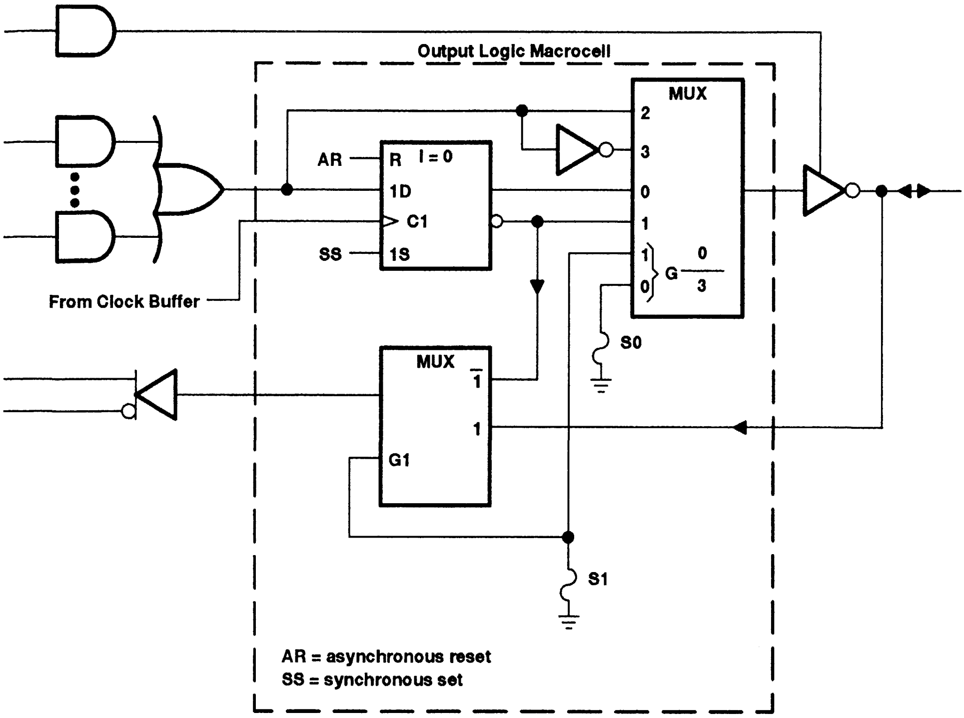
logic symbol (positive logic)



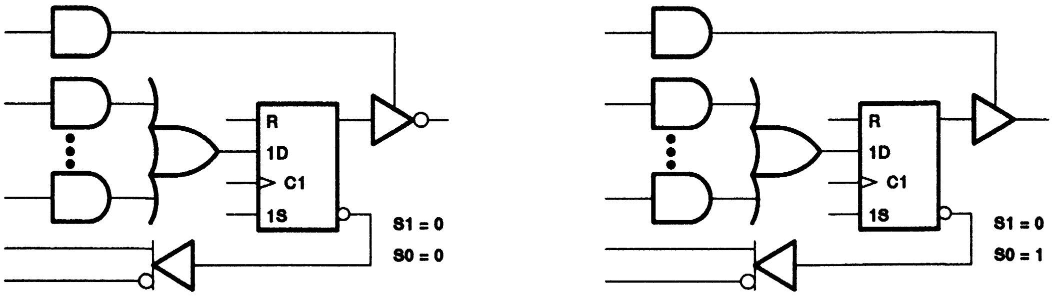


Fuse number = First fuse number + Increment
Inside each MACROCELL the "P" fuse is the polarity fuse and the "R" fuse is the register fuse.

output logic macrocell diagram

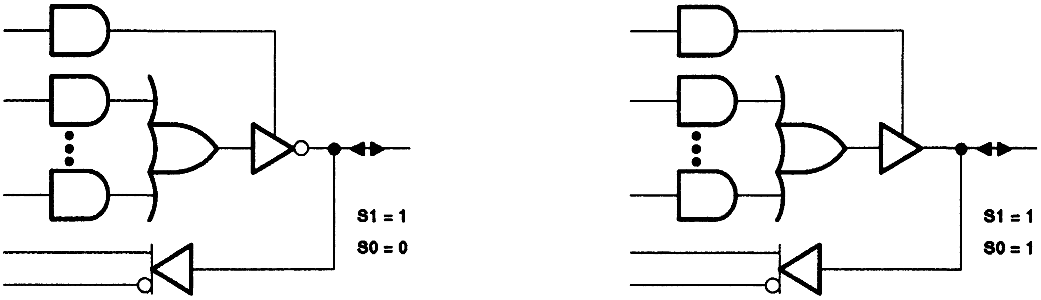


AR = asynchronous reset
SS = synchronous set



REGISTER FEEDBACK, REGISTERED, ACTIVE-LOW OUTPUT

REGISTER FEEDBACK, REGISTERED, ACTIVE-HIGH OUTPUT



I/O FEEDBACK, COMBINATIONAL, ACTIVE-LOW OUTPUT

I/O FEEDBACK, COMBINATIONAL, ACTIVE-HIGH OUTPUT

MACROCELL FEEDBACK AND OUTPUT FUNCTION TABLE

FUSE SELECT		FEEDBACK AND OUTPUT CONFIGURATION		
S1	**S0**			
0	0	Register feedback	Registered	Active low
0	1	Register feedback	Registered	Active high
1	0	I/O feedback	Combinational	Active low
1	1	I/O feedback	Combinational	Active high

0 = unblown fuse, 1 = blown fuse

S1 and S0 are select-function fuses as shown in the output logic macrocell diagram.

Figure 1. Resultant Macrocell Feedback and Output Logic After Programming

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage (see Note 1)	5.5 V
Voltage applied to disabled output (see Note 1)	5.5 V
Operating free-air temperature range	−55°C to 125°C
Storage temperature range	−65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle or during a preload cycle.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−2	mA
I_{OL}	Low-level output current				12	mA
t_w	Pulse duration	Clock high or low	15			ns
		Asynchronous Reset high or low	20			
t_{su}	Setup time before clock↑	Input	17			ns
		Feedback	17			
		Synchronous Preset (active)	17			
		Asynchronous Reset (inactive)	20			
t_h	Hold time, input, set, or feedback after clock↑		0			ns
T_A	Operating free-air temperature		−55		125	°C

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		$V_{CC} = 4.5$ V,	$I_I = -18$ mA				−1.2	V
V_{OH}		$V_{CC} = 4.5$ V,	$I_{OH} = -2$ mA		2.4	3.5		V
V_{OL}		$V_{CC} = 4.5$ V,	$I_{OL} = 12$ mA			0.25	0.5	V
I_{OZH}		$V_{CC} = 5.5$ V,	$V_O = 2.7$ V				0.1	mA
I_{OZL}		$V_{CC} = 5.5$ V,	$V_O = 0.4$ V				−0.1	mA
I_I		$V_{CC} = 5.5$ V,	$V_I = 5.5$ V				1	mA
I_{IH}		$V_{CC} = 5.5$ V,	$V_I = 2.7$ V				25	µA
I_{IL}	CLK	$V_{CC} = 5.5$ V,	$V_I = 0.4$ V				−0.2	mA
	All others						−0.1	
I_{OS}‡		$V_{CC} = 5.5$ V,	$V_O = 0.5$ V		−30		−90	mA
I_{CC}		$V_{CC} = 5.5$ V,	$V_I = \text{GND}$,	Outputs open			200	mA
C_i		f = 1 MHz,	$V_I = 2$ V			5.5		pF
C_o		f = 1 MHz,	$V_O = 2$ V			8		pF
C_{clk}		f = 1 MHz,	$V_{CLK} = 2$ V			7		pF

† All typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second. V_O is set at 0.5 V to avoid test problems caused by test equipment ground degradation.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	MAX	UNIT
f_{max}§	External feedback		R1 = 390 Ω, R2 = 750 Ω, See Figure 4	33.3		MHz
t_{pd}	I, I/O	I/O			20	ns
t_{pd}	I, I/O (reset)	Q			25	ns
t_{pd}	CLK	Q			15	ns
t_{en}	I, I/O	I/O, Q			20	ns
t_{dis}	I, I/O	I/O, Q			20	ns

§ f_{max} (with feedback) $= \dfrac{1}{t_{su} + t_{pd}(\text{CLK to Q})}$. Verification of t_{su} and t_{pd}(CLK to Q) may be used to verify expected performance.

preload procedure for registered outputs (see Notes 2 and 3)

The output registers can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below:

Step 1. With V_{CC} at 5 V and pin 1 at V_{IL}, raise pin 13 to V_{IHH}.
Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.
Step 3. Pulse pin 1, clocking in preload data.
Step 4. Remove output voltage, then lower pin 13 to V_{IL}. Preload can be verified by observing the voltage level at the output pin.

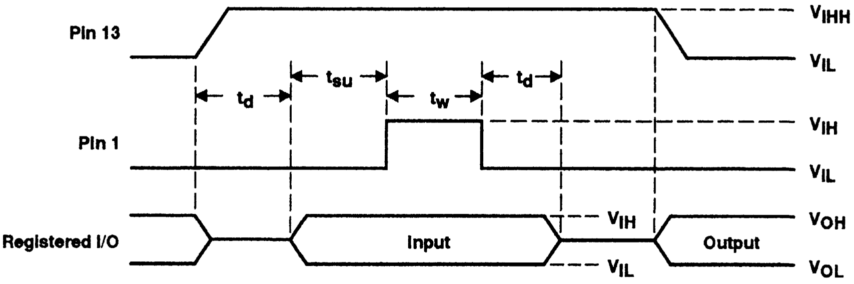
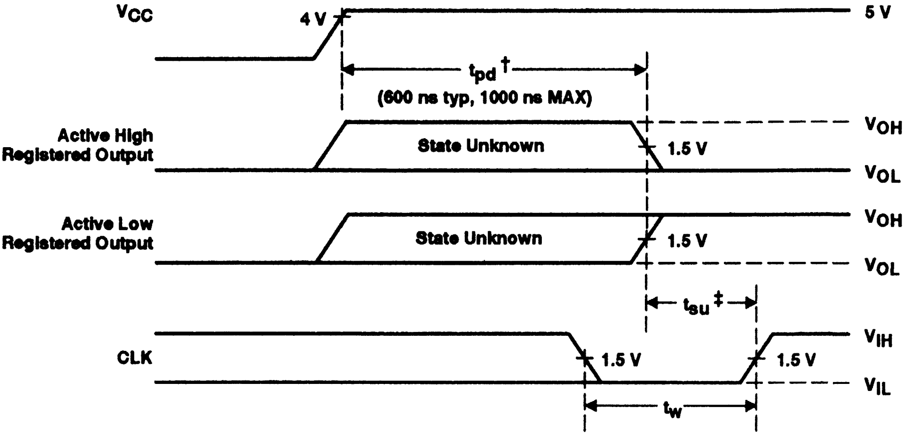


Figure 2. Preload Waveforms

NOTES: 2. Pin numbers shown are for the JT package only. If chip-carrier socket adapter is not used, pin numbers must be changed accordingly.
3. $t_d = t_{su} = t_w$ = 100 ns to 1000 ns. V_{IHH} = 10.25 V to 10.75 V.

power-up reset

Following power up, all registers are reset to zero. The output level depends on the polarity selected during programming. This feature provides extra flexibility to the system designer and is especially valuable in simplifying state-machine initialization. To ensure a valid power-up reset, it is important that the rise of V_{CC} be monotonic. Following power-up reset, a low-to-high clock transition must not occur until all applicable input and feedback setup times are met.



† This is the power-up reset time and applies to registered outputs only. The values shown are from characterization data.
‡ This is the setup time for input or feedback.

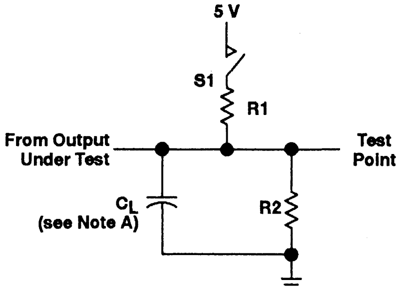
Figure 3. Power-Up Reset Waveforms

programming information

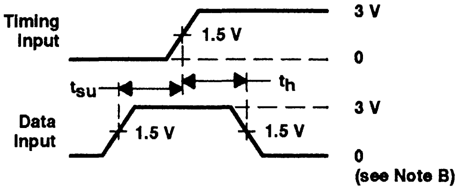
Texas Instruments programmable logic devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments programmable logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

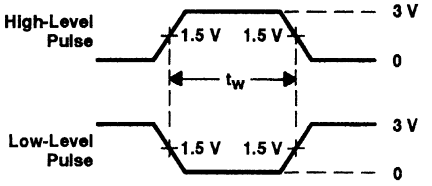
PARAMETER MEASUREMENT INFORMATION



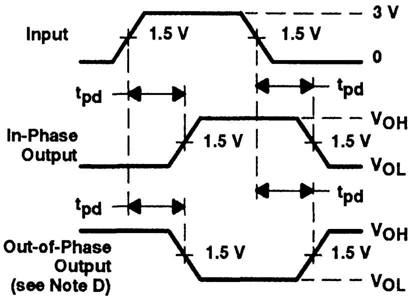
LOAD CIRCUIT FOR
3-STATE OUTPUTS



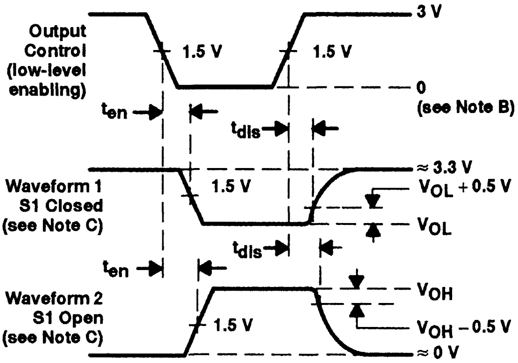
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.

B. All input pulses have the following characteristics: PRR ≤ 10 MHz, t_r and t_f = 2 ns, duty cycle = 50%.

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.

E. Equivalent loads may be used for testing.

Figure 4. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

SUPPLY CURRENT vs FREE–AIR TEMPERATURE

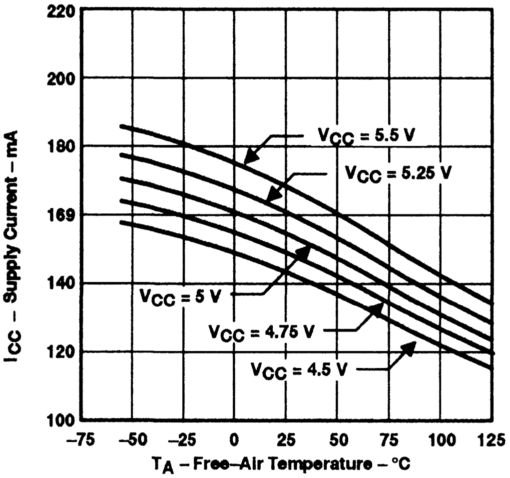


Figure 5

PROPAGATION DELAY TIME vs SUPPLY VOLTAGE

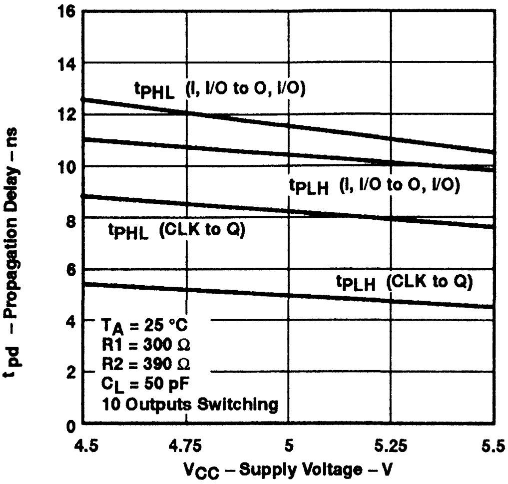


Figure 6

PROPAGATION DELAY TIME vs FREE–AIR TEMPERATURE

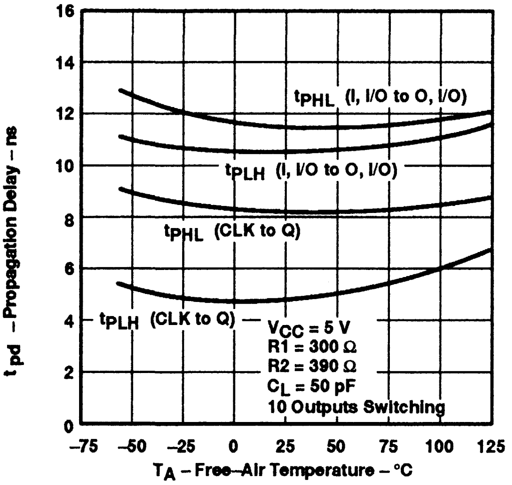


Figure 7

PROPAGATION DELAY TIME vs LOAD CAPACITANCE

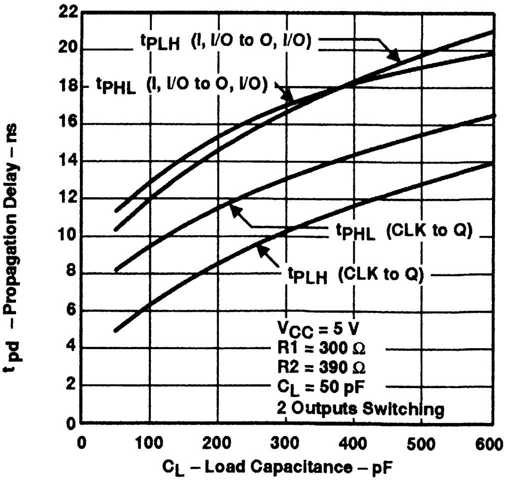


Figure 8

TYPICAL CHARACTERISTICS

POWER DISSIPATION vs FREQUENCY 10–BIT COUNTER MODE

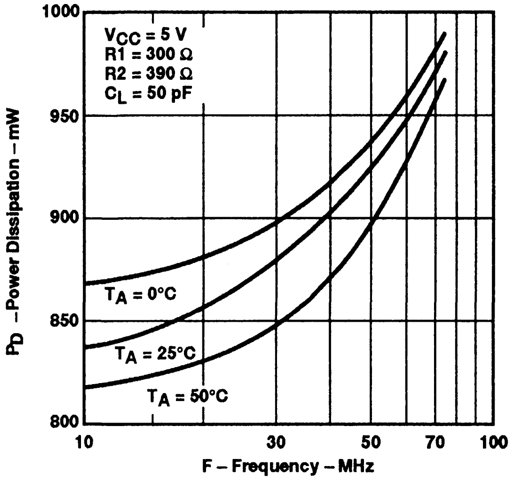


Figure 9

PROPAGATION DELAY TIME vs NUMBER OF OUTOUTS SWITCHING

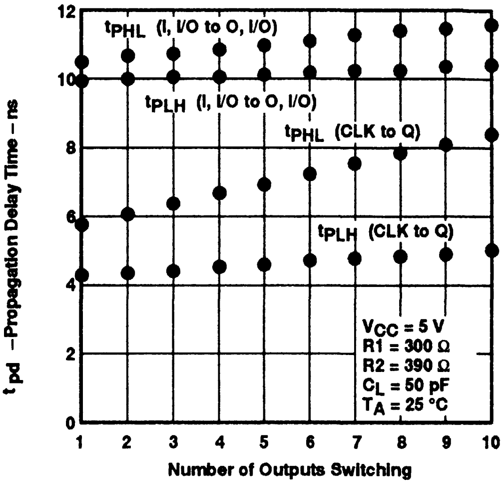


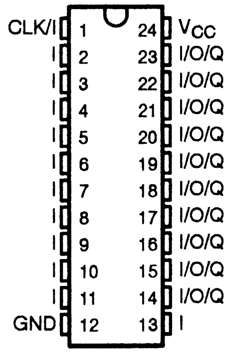
Figure 10

TIBPAL22VP10-20C, TIBPAL22VP10-25M
HIGH-PERFORMANCE *IMPACT-X*™ PROGRAMMABLE ARRAY LOGIC CIRCUITS

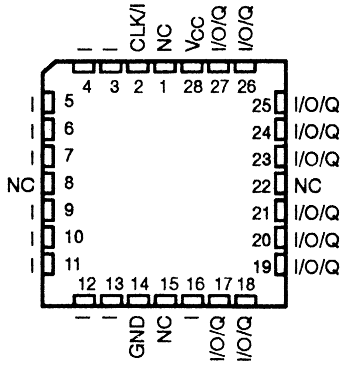
SRPS013 – D2943, FEBRUARY 1987 – REVISED JUNE 1991

- **Functionally Equivalent to the TIBPAL22V10/10A, with Additional Feedback Paths in the Output Logic Macrocell**
- **Choice of Operating Speeds:**
  TIBPAL22VP10-20C . . . 20 ns Max
  TIBPAL22VP10-25M . . . 25 ns Max
- **Variable Product Term Distribution Allows More Complex Functions to Be Implemented**
- **Each Output Is User Programmable for Registered or Combinational Operation, Polarity, and Output Enable Control**
- **TTL-Level Preload for Improved Testability**
- **Extra Terms Provide Logical Synchronous Set and Asynchronous Reset Capability**
- **Fast Programming, High Programming Yield, and Unsurpassed Reliability Ensured Using Ti-W Fuses**
- **AC and DC Testing Done at the Factory Utilizing Special Designed-In Test Features**
- **Dependable Texas Instruments Quality and Reliability**
- **Package Options Include Plastic Dual-In-Line and Chip Carrier Packages**

C SUFFIX . . . NT PACKAGE
M SUFFIX . . . JT PACKAGE
(TOP VIEW)



C SUFFIX . . . FN PACKAGE
M SUFFIX . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection
Pin assignments in operating mode

description

The TIBPAL22VP10' is equivalent to the TIBPAL22V10A but offers additional flexibility in the output structure. The improved output macrocell uses the registered outputs as inputs when in a high-impedance condition. This provides two additional output configurations for a total of six possible macrocell configurations all of which are shown in Figure 1.

These devices contain up to 22 inputs and 10 outputs. They incorporate the unique capability of defining and programming the architecture of each output on an individual basis. Outputs may be registered or nonregistered and inverting or noninverting. In addition, the data may be fed back into the array from either the register or the I/O port. The ten potential outputs are enabled through the use of individual product terms.

Further advantages can be seen in the introduction of variable product term distribution. This technique allocates from 8 to 16 logical product terms to each output for an average of 12 product terms per output. This variable allocation of terms allows far more complex functions to be implemented than in previously available devices.

These devices are covered by U.S. Patent 4,410,987.
IMPACT-X is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 1991, Texas Instruments Incorporated

description (continued)

Circuit design is enhanced by the addition of a synchronous set and an asynchronous reset product term. These functions are common to all registers. When the synchronous set product term is a logic 1, the output registers are loaded with a logic 1 on the next low-to-high clock transition. When the asynchronous reset product term is a logic 1, the output registers are loaded with a logic 0. The output logic level after set or reset depends on the polarity selected during programming. Output registers can be preloaded to any desired state during testing. Preloading permits full logical verification during product testing.

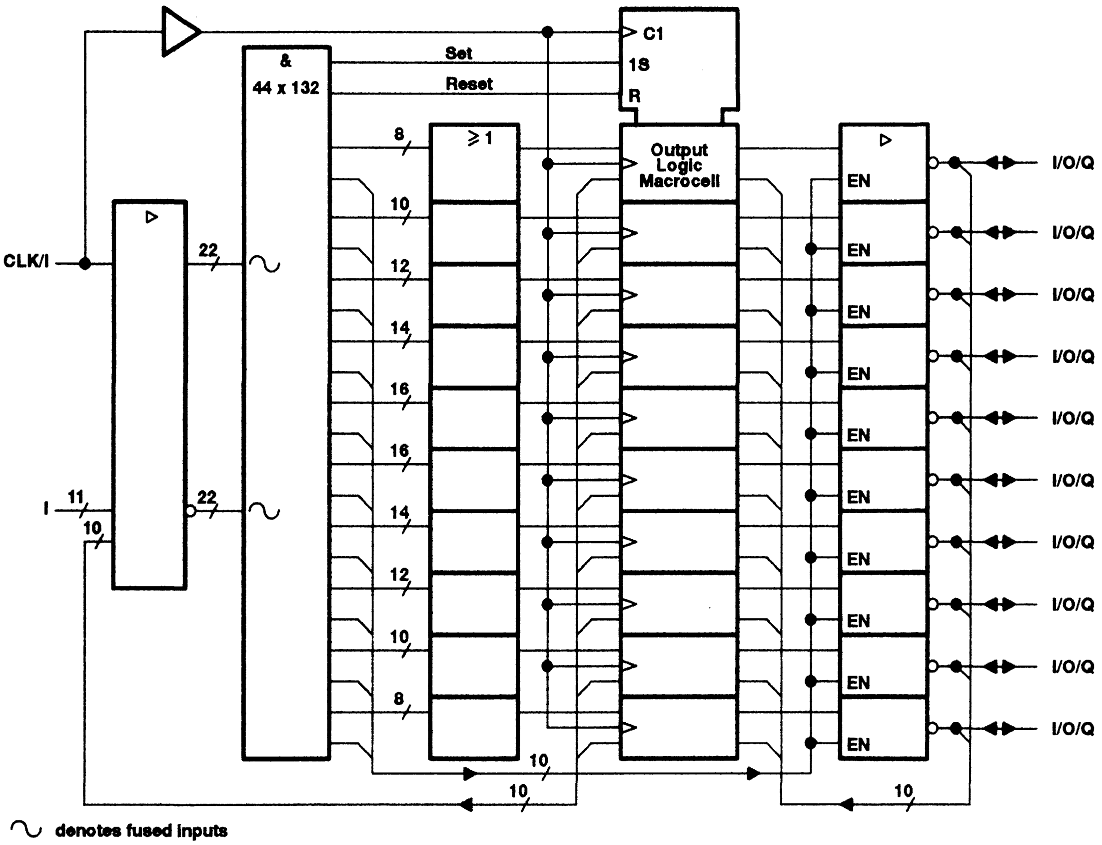
With features such as programmable output logic macrocells and variable product term distribution, the TIBPAL22VP10' offers quick design and development of custom LSI functions with complexities of 500 to 800 equivalent gates. Since each of the ten output pins may be individually configured as inputs on either a temporary or permanent basis, functions requiring up to 21 inputs and a single output or down to 12 inputs and 10 outputs are possible.

A power-up clear function is supplied that forces all registered outputs to a predetermined state after power is applied to the device. Registered outputs selected as active-low power-up with their outputs high. Registered outputs selected as active-high power-up with their outputs low.

A single security fuse is provided on each device to discourage unauthorized copying of fuse patterns. Once blown, the verification circuitry is disabled and all other fuses will appear to be open.

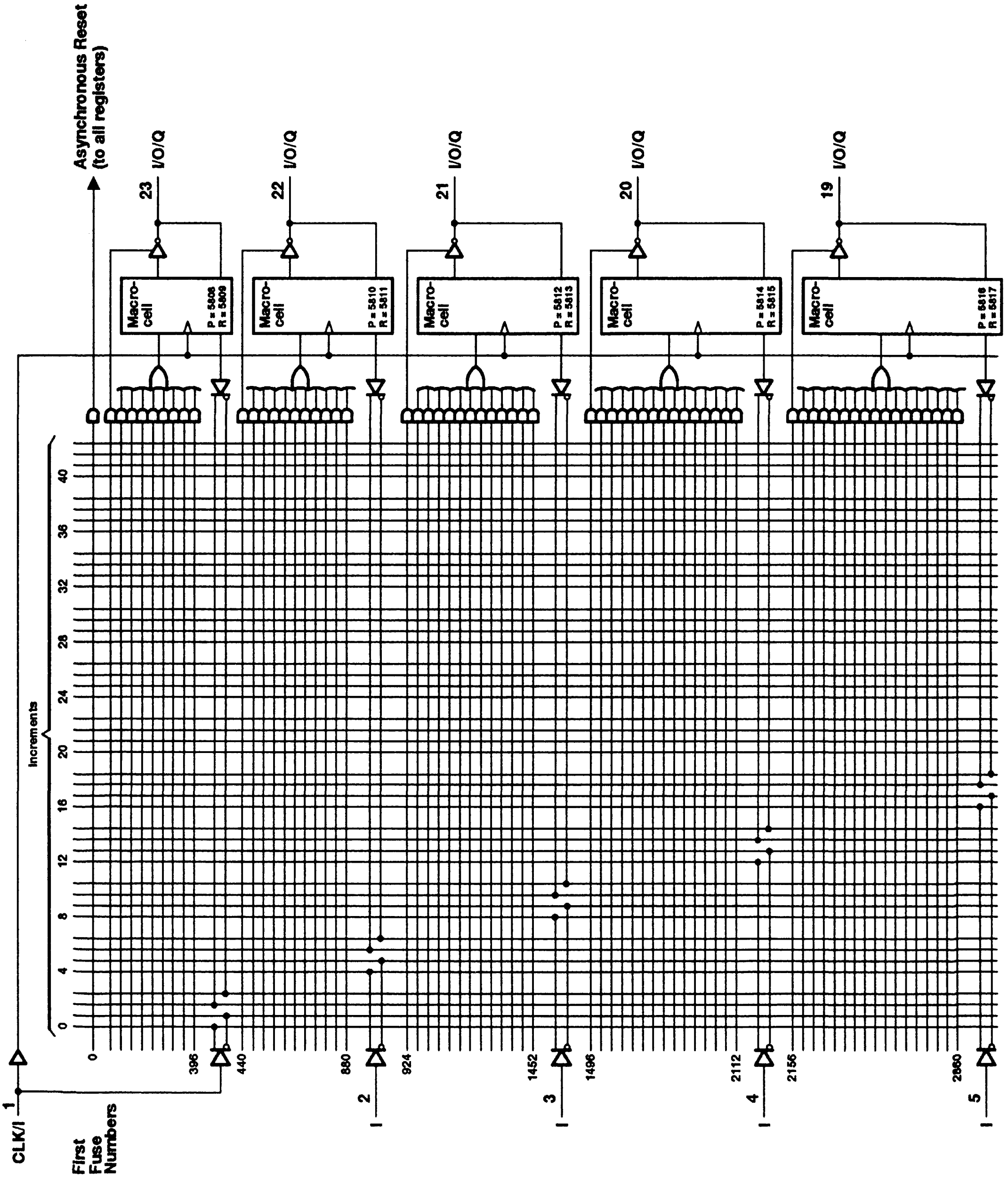
The TIBPAL22V10-20C is characterized for operation from 0°C to 75°C. The TIBPAL22V10-25M is characterized for operation over the full military temperature range of –55°C to 125°C.

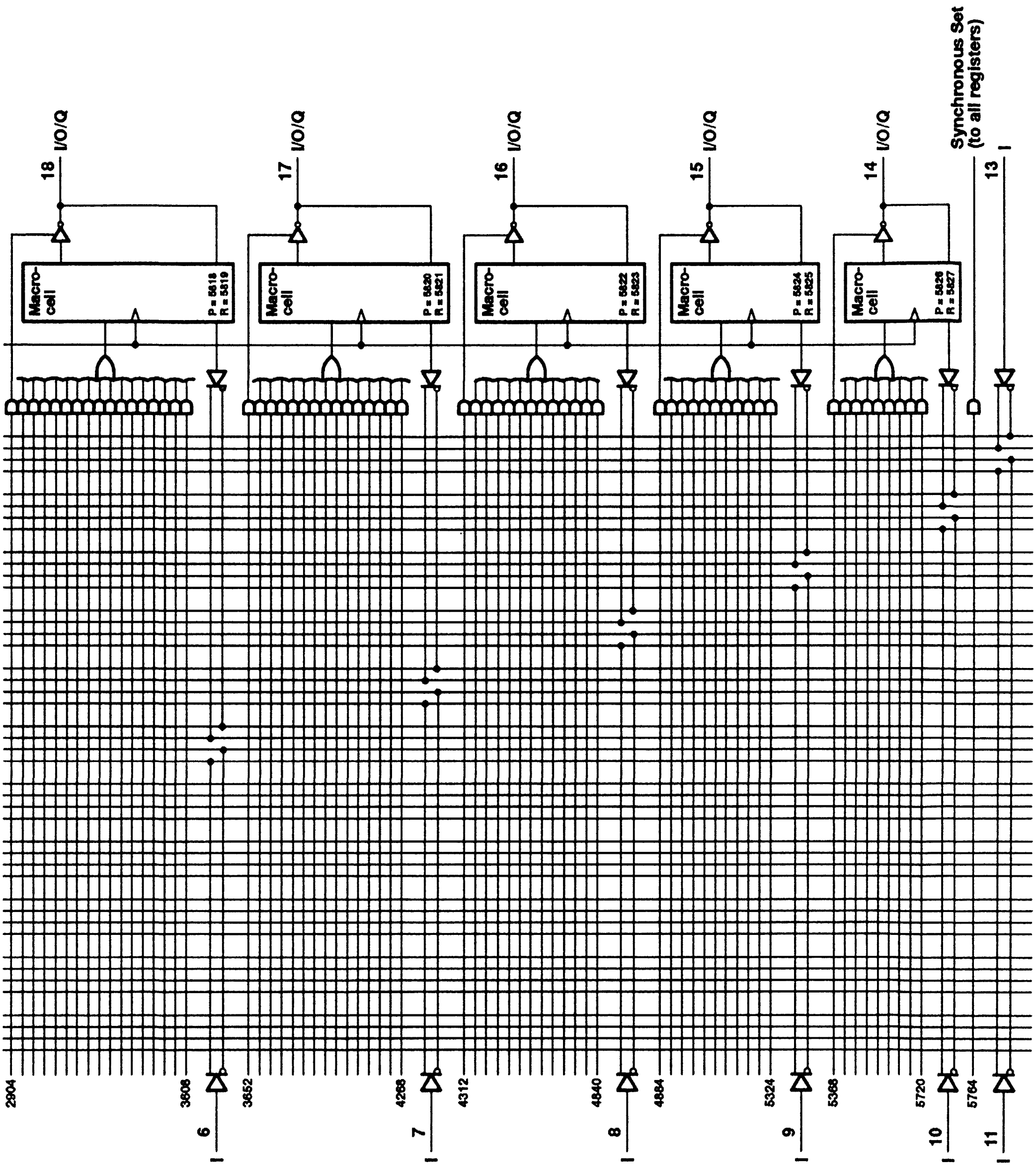
functional block diagram (positive logic)



∿ denotes fused inputs

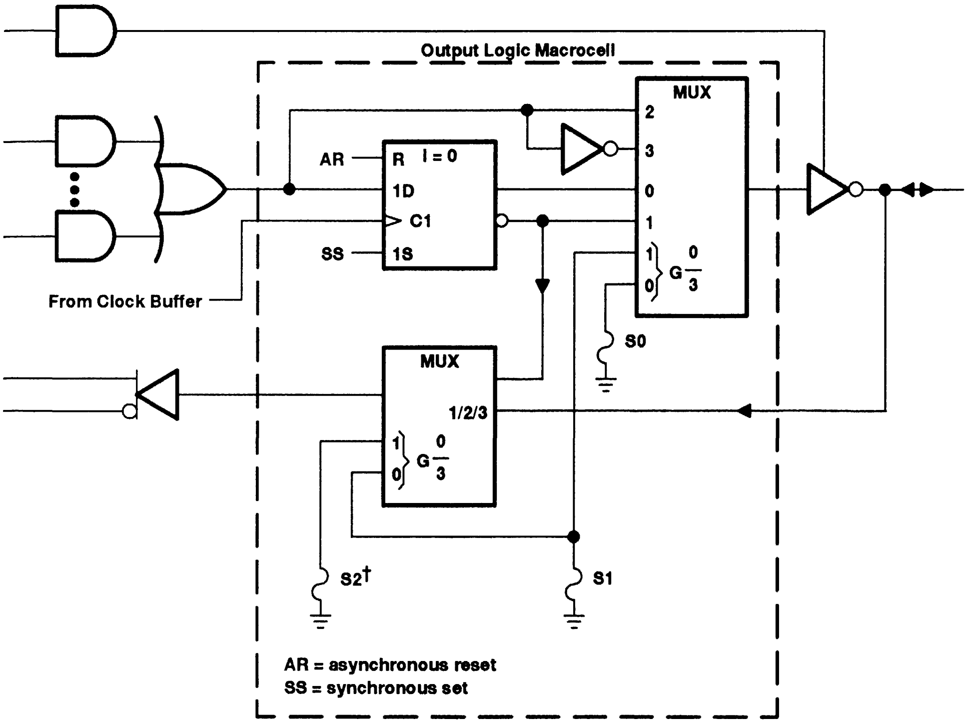
logic symbol (positive logic)





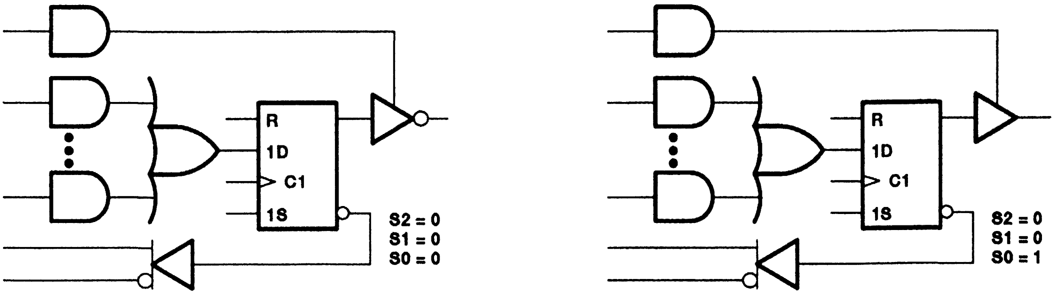
Fuse number = First fuse number + Increment
Inside each MACROCELL the "P" fuse is the polarity fuse and the "R" fuse is the register fuse.

output logic macrocell diagram

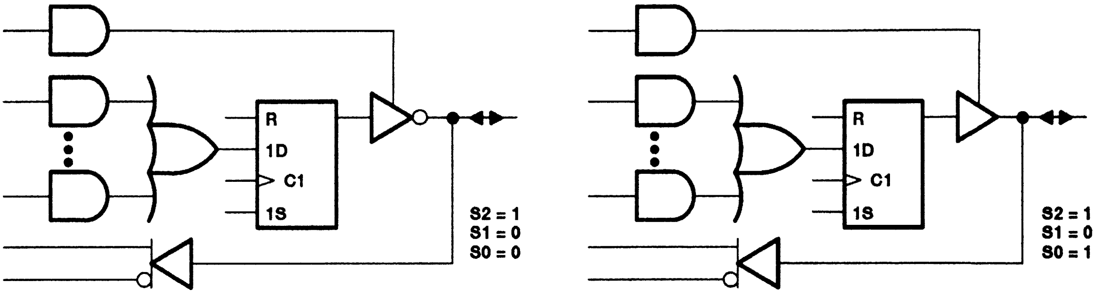


---

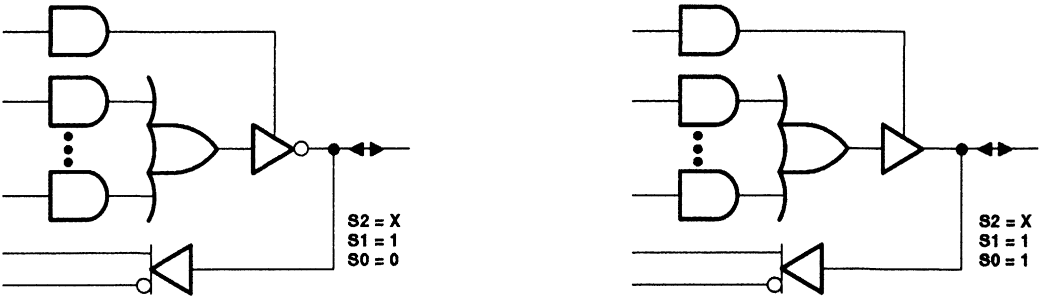
† This fuse is unique to the Texas Instruments TIBPAL22VP10'. It allows feedback from the I/O port using registered outputs as shown in the macrocell fusing logic function table.



REGISTER FEEDBACK, REGISTERED, ACTIVE-LOW OUTPUT **REGISTER FEEDBACK, REGISTERED, ACTIVE-HIGH OUTPUT**



I/O FEEDBACK, REGISTERED, ACTIVE-LOW OUTPUT† **I/O FEEDBACK, REGISTERED, ACTIVE-HIGH OUTPUT†**



I/O FEEDBACK, COMBINATIONAL, ACTIVE-LOW OUTPUT **I/O FEEDBACK, COMBINATIONAL, ACTIVE-HIGH OUTPUT**

† These configurations are unique to the TIBPAL22VP10' and provide added flexibility when comparing it to the TIBPAL22V10 or TIBPAL22V10A.

Figure 1. Resultant Macrocell Feedback and Output Logic After Programming

MACROCELL FEEDBACK AND OUTPUT FUNCTION TABLE

FUSE SELECT			FEEDBACK AND OUTPUT CONFIGURATION		
S2	**S1**	**S0**			
0	0	0	Register feedback	Registered	Active low
0	0	1	Register feedback	Registered	Active high
1	0	0	I/O feedback	Registered	Active low
1	0	1	I/O feedback	Registered	Active high
X	1	0	I/O feedback	Combinational	Active low
X	1	1	I/O feedback	Combinational	Active high

0 = unblown fuse, 1 = blown fuse, X = unblown or blown fuse
S2, S1 and S0 are select-function fuses as shown in the output logic macrocell diagram.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)		7 V
Input voltage (see Note 1)		5.5 V
Voltage applied to disabled output (see Note 1)		5.5 V
Operating free-air temperature range:	TIBPAL22VP10-20C	0°C to 75°C
	TIBPAL22VP10-25M	−55°C to 125°C
Storage temperature range		−65°C to 150°C

NOTE 1: These ratings apply except for programming pins during a programming cycle or during a preload cycle.

recommended operating conditions

			TIBPAL22VP10-20C			TIBPAL22VP10-25M			UNIT
			MIN	**NOM**	**MAX**	**MIN**	**NOM**	**MAX**	
V_{CC}	Supply voltage		4.75	5	5.25	4.5	5	5.5	V
V_{IH}	High-level input voltage		2		5.5	2		5.5	V
V_{IL}	Low-level input voltage				0.8			0.8	V
I_{OH}	High-level output current				−3.2			−2	mA
I_{OL}	Low-level output current				16			12	mA
f_{clock}	Clock frequency†				37			25	MHz
t_w	Pulse duration	Clock high or low	10			20			ns
		Asynchronous Reset high or low	20			30			
t_{su}	Setup time before clock↑	Input	15			20			ns
		Feedback	15			20			
		Synchronous Preset (active)	15			20			
		Asynchronous Reset (inactive)	20			25			
t_h	Hold time, input, preset, or feedback after clock↑		0			0			ns
T_A	Operating free-air temperature		0		75	−55		125	°C

† f_{clock} (with feedback) $= \dfrac{1}{t_{su} + t_{pd}\ (\text{CLK to Q})}$, f_{clock} without feedback can be calculated as

$$f_{clock}\ (\text{without feedback}) = \frac{1}{t_w\ \text{high} + t_w\ \text{low}}.$$

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.75 V,	I_I = −18 mA				−1.2	V
V_{OH}		V_{CC} = 4.75 V,	I_{OH} = −3.2 mA		2.4	3.5		V
V_{OL}		V_{CC} = 4.75 V,	I_{OL} = 16 mA			0.35	0.5	V
I_{OZH}		V_{CC} = 5.25 V,	V_O = 2.7 V				0.1	mA
I_{OZL}	Any output	V_{CC} = 5.25 V,	V_O = 0.4 V				−100	µA
	Any I/O						−250	
I_I		V_{CC} = 5.25 V,	V_I = 5.5 V				1	mA
I_{IH}		V_{CC} = 5.25 V,	V_I = 2.7 V				25	µA
I_{IL}		V_{CC} = 5.25 V,	V_I = 0.4 V				−0.25	mA
I_{OS}‡		V_{CC} = 5.25 V,	V_O = 0.5 V		−30		−90	mA
I_{CC}		V_{CC} = 5.25 V,	V_I = GND,	Outputs open		140	180	mA

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	TYP†	MAX	UNIT
f_{max}§			C_L = 50 pF, R1 = 300 Ω, R2 = 390 Ω, See Figure 4	37	50		MHz
t_{pd}	I, I/O	I/O			12	20	ns
t_{pd}	I, I/O (reset)	Q			12	20	ns
t_{pd}	CLK	Q			8	12	ns
t_{en}	I, I/O	I/O, Q			12	20	ns
t_{dis}	I, I/O	I/O, Q			12	20	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second. V_O is set at 0.5 V to avoid test problems caused by test equipment ground degradation.

§ $f_{max}\ \text{(with feedback)} = \dfrac{1}{t_{su} + t_{pd}\ \text{(CLK to Q)}}$, f_{max} without feedback can be calculated as

$$f_{max}\ \text{(without feedback)} = \frac{1}{t_w\ \text{high} + t_w\ \text{low}}.$$

electrical characteristics over recommended operating free-air temperature range

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{IK}	V_{CC} = 4.5 V,	I_I = −18 mA				−1.2	V
V_{OH}	V_{CC} = 4.5 V,	I_{OH} = −2 mA		2.4	3.5		V
V_{OL}	V_{CC} = 4.5 V,	I_{OL} = 12 mA			0.25	0.5	V
I_{OZH}	V_{CC} = 5.5 V,	V_O = 2.7 V				0.1	mA
I_{OZL}	V_{CC} = 5.5 V,	V_O = 0.4 V				−0.1	mA
I_I	V_{CC} = 5.5 V,	V_I = 5.5 V				1	mA
I_{IH}	V_{CC} = 5.5 V,	V_I = 2.7 V				25	µA
I_{IL}	V_{CC} = 5.5 V,	V_I = 0.4 V				−0.25	mA
I_{OS}‡	V_{CC} = 5.5 V,	V_O = 0.5 V		−30		−90	mA
I_{CC}	V_{CC} = 5.5 V,	V_I = GND,	Outputs open		140	200	mA

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	TYP†	MAX	UNIT
f_{max}§			C_L = 50 pF, R1 = 390 Ω, R2 = 750 Ω, See Figure 4	25	50		MHz
t_{pd}	I, I/O	I/O			12	25	ns
t_{pd}	I, I/O (reset)	Q			12	25	ns
t_{pd}	CLK	Q			8	15	ns
t_{en}	I, I/O	I/O, Q			12	25	ns
t_{dis}	I, I/O	I/O, Q			12	25	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second. V_O is set at 0.5 V to avoid test problems caused by test equipment ground degradation.

§ f_{max} (with feedback) $= \frac{1}{t_{su} + t_{pd}\ (\text{CLK to Q})}$, f_{max} without feedback can be calculated as

$$f_{max}\ (\text{without feedback}) = \frac{1}{t_w\ \text{high} + t_w\ \text{low}}.$$

preload procedure for registered outputs (see Notes 2 and 3)

The output registers can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. Each register is preloaded individually by following the steps given below:

Step 1. With V_{CC} at 5 V and pin 1 at V_{IL}, raise pin 13 to V_{IHH}.
Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.
Step 3. Pulse pin 1, clocking in preload data.
Step 4. Remove output voltage, then lower pin 13 to V_{IL}. Preload can be verified by observing the voltage level at the output pin.

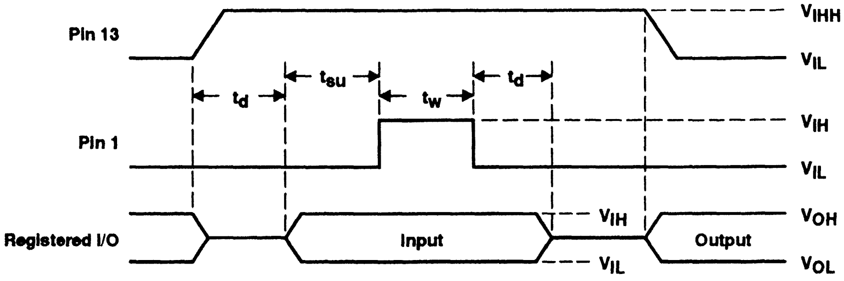
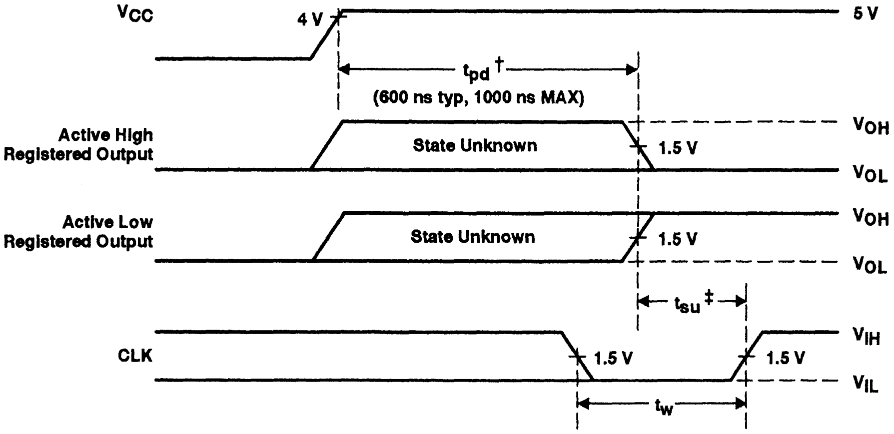


Figure 2. Preload Waveforms

NOTES: 2. Pin numbers shown are for JT and NT packages only. If chip-carrier socket adapter is not used, pin numbers must be changed accordingly.
3. $t_d = t_{su} = t_w$ = 100 ns to 1000 ns. V_{IHH} = 10.25 V to 10.75 V.

power-up reset

Following power up, all registers are reset to zero. The output level depends on the polarity selected during programming. This feature provides extra flexibility to the system designer and is especially valuable in simplifying state-machine initialization. To ensure a valid power-up reset, it is important that the rise of V_{CC} be monotonic. Following power-up reset, a low-to-high clock transition must not occur until all applicable input and feedback setup times are met.



† This is the power-up reset time and applies to registered outputs only. The values shown are from characterization data.
‡ This is the setup time for input or feedback.

Figure 3. Power-Up Reset Waveforms

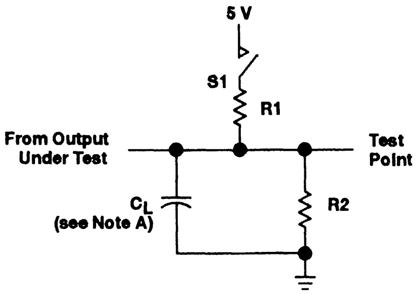
programming information

Texas Instruments programmable logic devices can be programmed using widely available software and inexpensive device programmers.

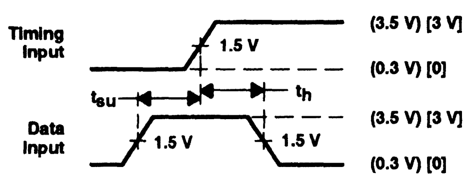
When the additional fuses are not being used, the TIBPAL22VP10 can be programmed using the TIBPAL22V10/10A programming algorithm. The fuse configuration data can either be from a JEDEC file (format per JEDEC Standard No. 3-A) or a TIBPAL22V10/10A master.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments programmable logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

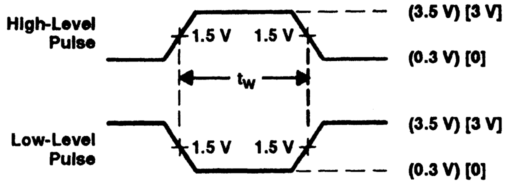
PARAMETER MEASUREMENT INFORMATION



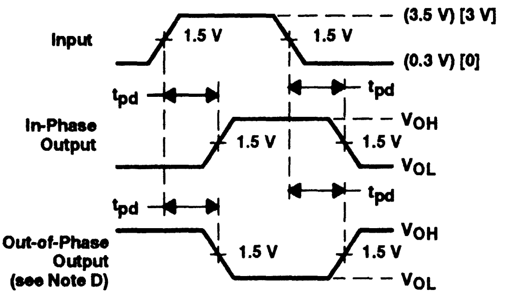
LOAD CIRCUIT FOR
3-STATE OUTPUTS



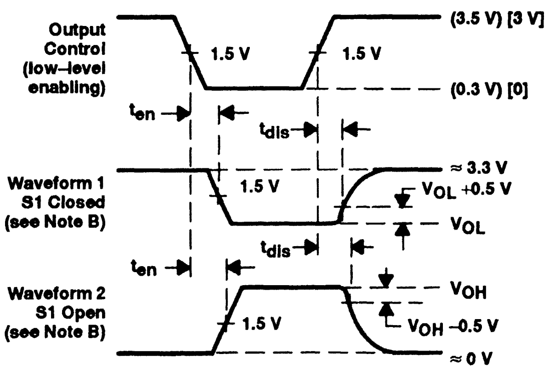
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses have the following characteristics: For C suffix, use the voltage levels indicated in parentheses ( ). PRR ≤ 1 MHz, $t_r = t_f \le 2$ ns, duty cycle = 50%. For M suffix, use the voltage levels indicated in brackets [ ]. PRR ≤ 10 MHz, t_r and $t_f \le 2$ ns, duty cycle = 50%.

D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.

E. Equivalent loads may be used for testing.

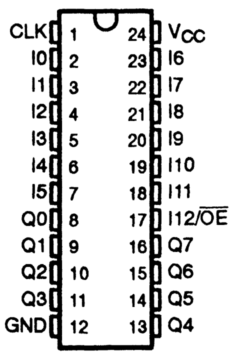
Figure 4. Load Circuit and Voltage Waveforms

TIBPLS506AC
13 × 97 × 8 FIELD-PROGRAMMABLE LOGIC SEQUENCER

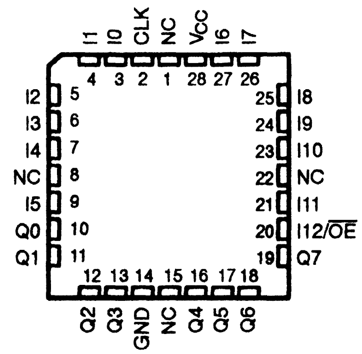
SRPS003B – D3090, DECEMBER 1987 – REVISED JUNE 1991

- **58-MHz Max Clock Rate**
- **Two Transition Complement Array Terms**
- **16-Bit Internal State Registers**
- **8-Bit Output Registers**
- **Outputs Programmable for Registered or Combinational Operation**
- **Ideal for Waveform Generation and High-Performance State Machine Applications**
- **Programmable Output Enable**
- **Programmable Clock Polarity**

JT OR NT PACKAGE
(TOP VIEW)



FK OR FN PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TIBPLS506AC is a TTL field-programmable state machine of the Mealy type. This state machine (logic sequencer) contains 97 product terms (AND terms) and 48 sum terms (OR terms). The product and sum terms are used to control the 16-bit internal state registers and the 8-bit output registers.

The outputs of the internal state registers (P0–P15) are fed back and combined with the 13 inputs (I0–I12) to form the AND array. In addition, two sum terms are complemented and fed back to the AND array, which allows any product term to be summed, complemented, and used as input to the AND array.

The eight output cells can be individually programmed for registered or combinational operation. Nonregistered operation is selected by blowing the output multiplexer fuse. Registered output operation is selected by leaving the output multiplexer fuse intact.

Pin 17 can be programmed to function as an input and/or an output enable. Blowing the output enable fuse lets pin 17 function as an output enable but does not disconnect pin 17 from the input array. When the output enable fuse is intact, pin 17 functions only as an input with the outputs being permanently enabled.

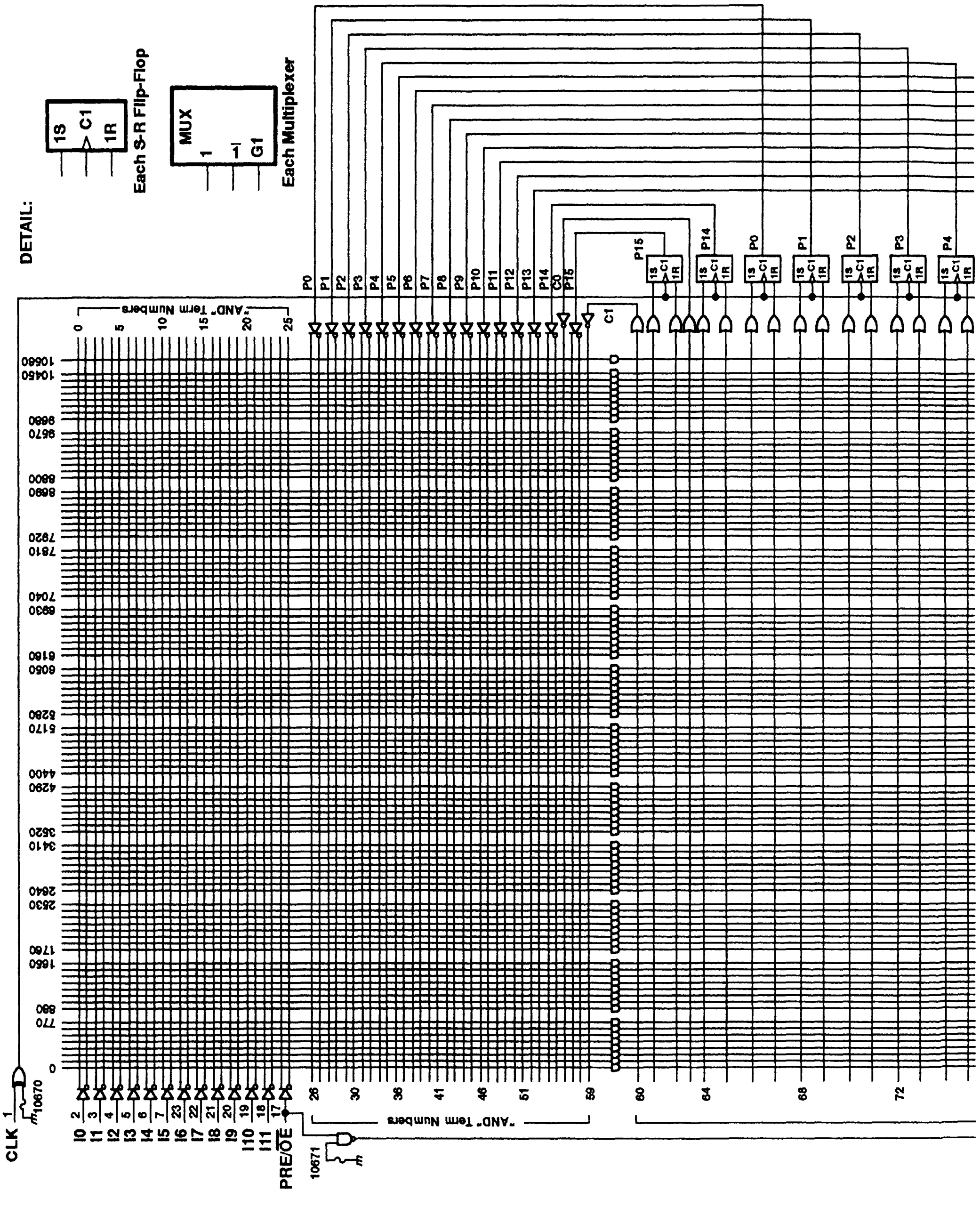
The state and output registers are synchronously clocked by the fuse programmable clock input. The clock polarity fuse selects either postive- or negative-edge triggering. Negative-edge triggering is selected by blowing the clock polarity fuse. Leaving this fuse intact selects positive-edge triggering. After power-up, the device must be initialized to the desired state. When the output multiplexer fuse is left intact, registered operation is selected.

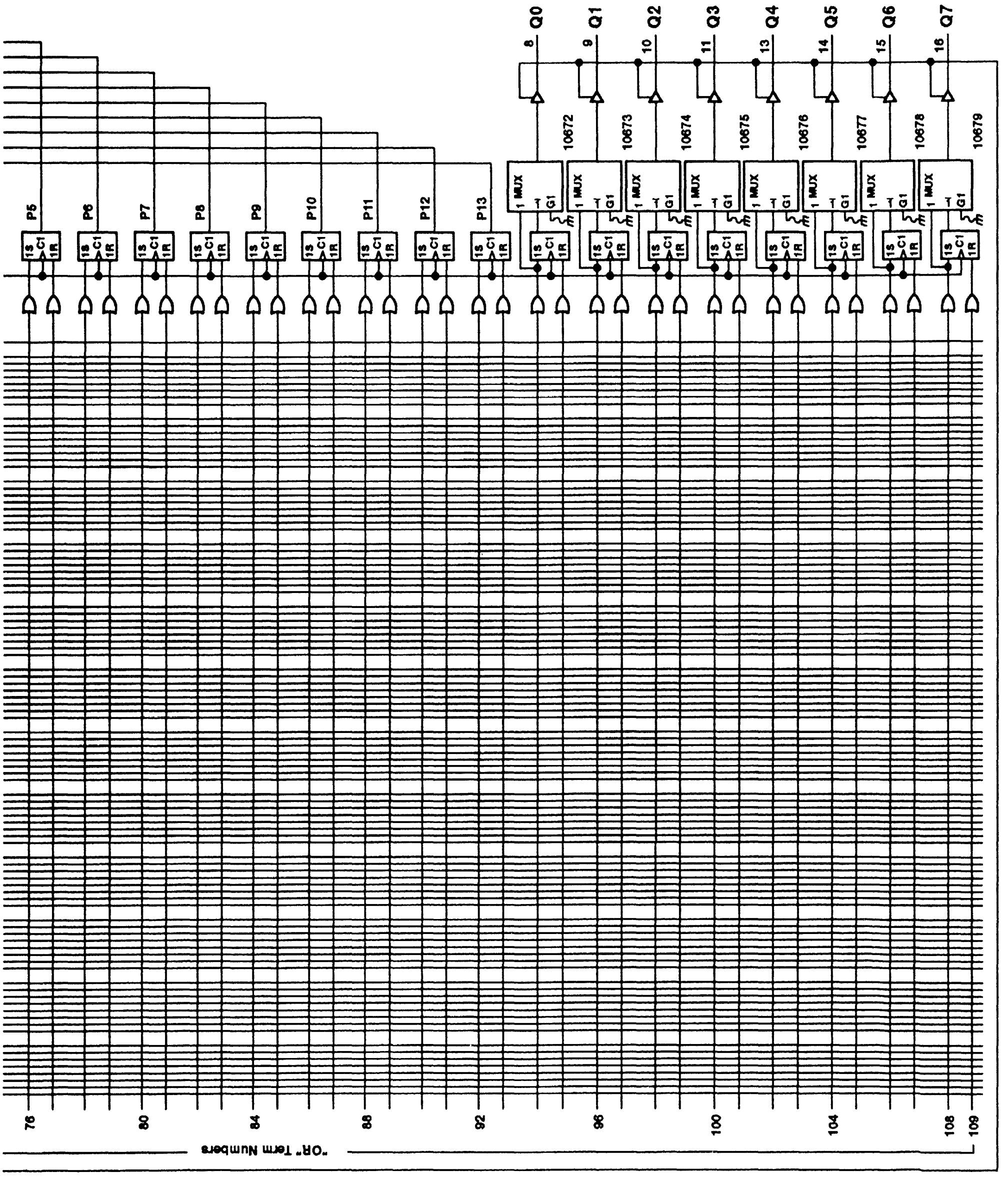
The TIBPLS506AC is characterized for operation from 0°C to 75°C.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 1991, Texas Instruments Incorporated

logic diagram (positive logic)





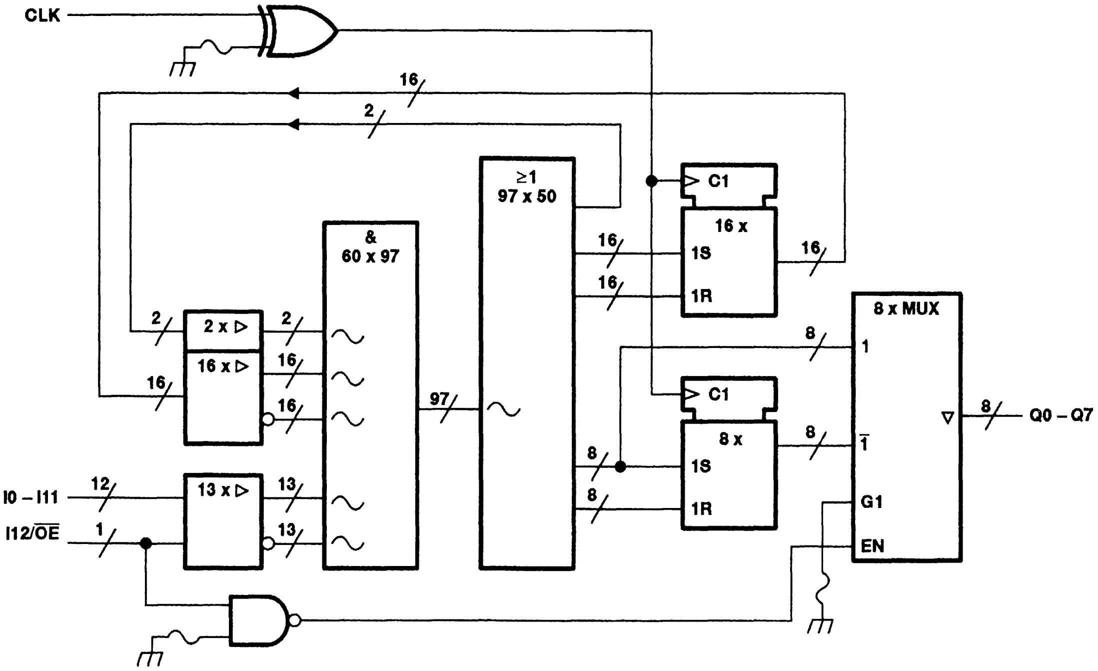
All inputs to AND gates, exclusive-OR gates, and multiplexers with a blown link assume the logic-1 state.
All OR gate inputs with a blown link assume the logic-0 state.

S-R FUNCTION TABLE (see Note 1)

CLK POLARITY FUSE	CLK	S	R	STATE REGISTER
INTACT	↑	L	L	Q_0
INTACT	↑	L	H	L
INTACT	↑	H	L	H
INTACT	↑	H	H	INDETERMINATE
BLOWN	↓	L	L	Q_0
BLOWN	↓	L	H	L
BLOWN	↓	H	L	H
BLOWN	↓	H	H	INDETERMINATE

NOTE 1: Q_0 is the state of the S-R registers before the active clock edge.

functional block diagram (positive logic)



∿ denotes fused inputs

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 2)	7 V
Input voltage (see Note 2)	5.5 V
Voltage applied to disabled output (see Note 2)	5.5 V
Operating free-air temperature range	0°C to 75°C
Storage temperature range	–65°C to 150°C

NOTE 2: These ratings apply except when programming pins during a programming cycle or during diagnostic testing.

recommended operating conditions

				MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage			4.75	5	5.25	V
V_{IH}	High-level input voltage, V_{CC} = 5.25 V			2		5.5	V
V_{IL}	Low-level input voltage, V_{CC} = 4.75 V					0.8	V
I_{OH}	High-level output current					–3.2	mA
I_{OL}	Low-level output current					16	mA
t_w	Pulse duration	Clock high		6			ns
		Clock low		6			
t_{su}	Setup time before CLK active transition[†]	Input or feedback to S/R↑ inputs	Without C-array	12			ns
		Input or feedback to S/R↓ inputs[‡]		20			
		Input or feedback to S/R inputs	With C-array	25			
t_h	Hold time after CLK	Input or feedback to S/R inputs		0			ns
T_A	Operating free-air temperature			0	25	75	°C

[†] The active edge of CLK is determined by the programmed state of CLK polarity fuse.

[‡] See the OR term loading section and Figure 3.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP[§]	MAX	UNIT
V_{IK}	V_{CC} = 4.75 V,	I_I = –18 mA				–1.2	V
V_{OH}	V_{CC} = 4.75 V,	I_{OH} = –3.2 mA		2.4	3		V
V_{OL}	V_{CC} = 4.75 V,	I_{OL} = 16 mA			0.37	0.5	V
I_{OZH}	V_{CC} = 5.25 V,	V_O = 2.7 V				20	µA
I_{OZL}	V_{CC} = 5.25 V,	V_O = 0.4 V				–20	µA
I_I	V_{CC} = 5.25 V,	V_I = 5.5 V				0.1	mA
I_{IH}	V_{CC} = 5.25 V,	V_I = 2.7 V				20	µA
I_{IL}	V_{CC} = 5.25 V,	V_I = 0.4 V				–0.25	mA
I_O[¶]	V_{CC} = 5.25 V,	V_O = 0.5 V		–30		–130	mA
I_{CC}	V_{CC} = 5.25 V,	See Note 3,	Outputs open		156	210	mA
C_i	f = 1 MHz,	V_I = 2 V			7		pF
C_o	f = 1 MHz,	V_O = 2 V			11		pF
C_{clk}	f = 1 MHz,	V_{CLK} = 2 V			14		pF

[§] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[¶] This parameter approximates I_{OS}. The condition V_O = 0.5 V takes tester noise into account. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

NOTE 3: When the clock is programmed for negitive edge, then V_I = 4.75 V. When the clock is programmed for positive edge, then V_I = 0.

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	TYP†	MAX	UNIT
f_{max}‡	Without C-array		R1 = 300 Ω, R2 = 390 Ω, See Figure 5	58	65		MHz
	With C-array			33	45		
	External feedback without C-array			45	60		
	External feedback with C-array			28.5	40		
t_{pd}	CLK	Q (nonregistered)		6		25	ns
		Q (registered)		3		10	
	I or Feedback	Q (nonregistered)		6		20	ns
t_{en}	$\overline{OE}$↓	Q		1	6	10	ns
t_{dis}	$\overline{OE}$↑	Q		1	6	10	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ See the f_{max} calculations section.

f_{max} calculations

The following is a brief description of how the different operating frequencies can be achieved when using the TIBPLS506A.

f_{max} without C-(complementary) array = $\dfrac{1}{t_{su} + t_{pd}\ \text{CLK to Q}}$ where setup time t_{su} before CLK at the S/R register inputs = 12 ns and propagation delay time t_{pd} CLK to Q for the internal S/R registers = 5ns (difference in t_{pd} from CLK and feedback, 25 to 20).

Thus: f_{max} for this condition = $\dfrac{1}{(12 + 5)\ \text{ns}} = \dfrac{1}{17\ \text{ns}}$ = 58 MHz.

f_{max} with the C-array = $\dfrac{1}{t_{su} + t_{pd}\ \text{CLK to Q}}$ where t_{su} setup time before CLK at the S/R register inputs = 25 ns and propagation delay time t_{pd} CLK to Q for the internal S/R registers = 5 ns (difference in t_{pd} from CLK and feedback, 25 to 20)

Thus: f_{max} for this condition = $\dfrac{1}{(25 + 5)\ \text{ns}} = \dfrac{1}{30\ \text{ns}}$ = 33 MHz.

f_{max} external feedback without the C-array = $\dfrac{1}{t_{su} + t_{pd}\ \text{CLK to Q}}$ where setup time t_{su} before CLK at the S/R register inputs = 12 ns and propagation delay time t_{pd} CLK to Q for the internal S/R registers = 10 ns

Thus: f_{max} for this condition = $\dfrac{1}{(12 + 10)\ \text{ns}} = \dfrac{1}{22\ \text{ns}}$ = 45 MHz.

f_{max} external feedback with the C-array = $\dfrac{1}{t_{su} + t_{pd}\ \text{CLK to Q}}$ where setup time t_{su} before CLK at the S/R register inputs = 25 ns and propagation delay time t_{pd} CLK to Q for the internal S/R registers = 10 ns.

Thus: f_{max} for this condition = $\dfrac{1}{(25 + 10)\ \text{ns}} = \dfrac{1}{35\ \text{ns}}$ = 28.5 MHz.

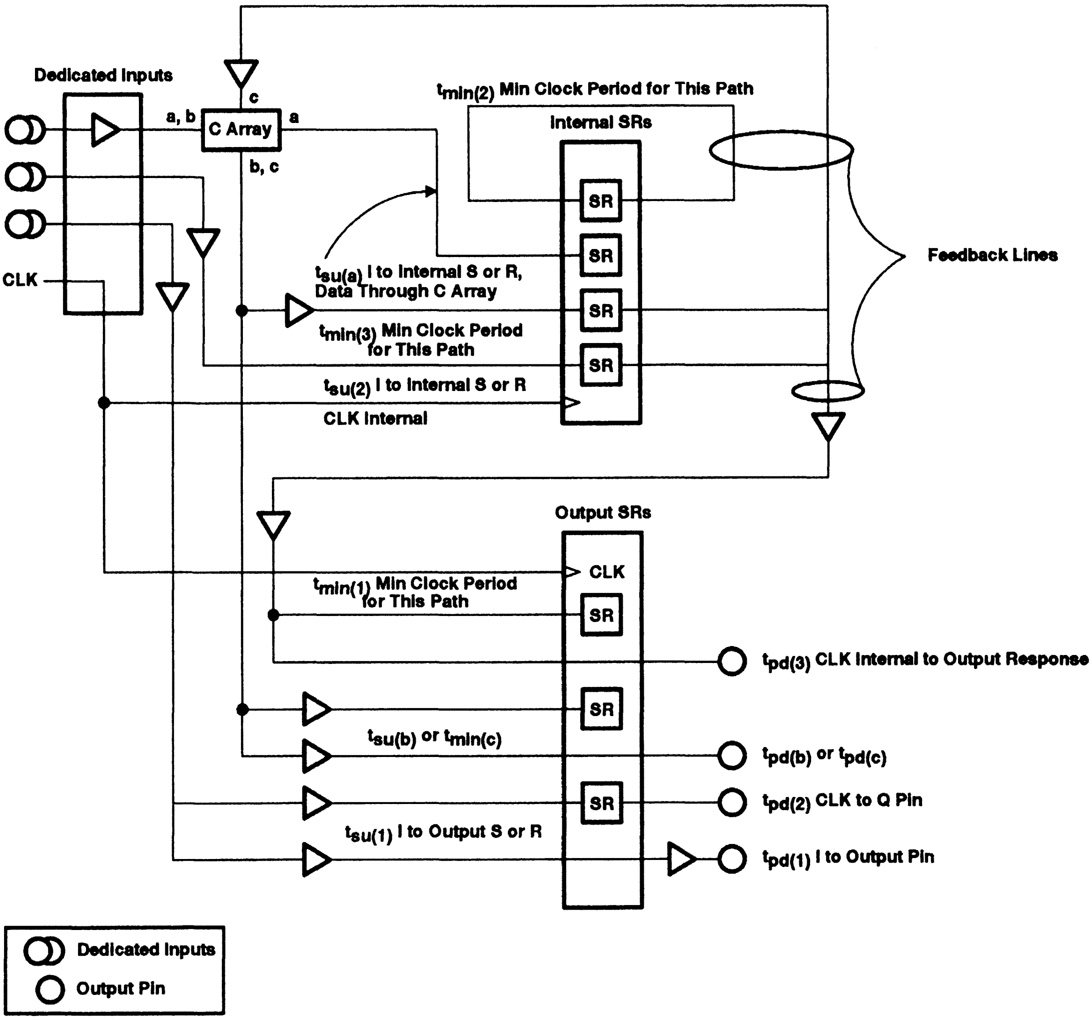


Figure 1. Timing Model

glossary — timing model

$t_{pd(1)}$ — Maximum time interval from the time a signal edge is received at any input pin to the time any logically affected combinational output pin delivers a response.

$t_{pd(2)}$ — Maximum time interval from a positive edge on the clock input pin to data delivery on the output pin corresponding to any output SR register.

$t_{pd(3)}$ — Maximum time interval from the positive edge on the clock input pin to the response on any logically affected combinational configured output (at the pin), where data origin is any internal SR register.

$t_{pd(b)}$ — Maximum time interval from the time a signal edge is received at any input pin to the time any logically affected combinational output pin delivers a response, where data passes through a C-array once before reaching the affected output.

$t_{pd(c)}$ — Maximum time interval from the positive edge on the clock input pin to the response on any logically affected combinational configured output (at the pin), where data origin is any internal SR register and data passes once through a C-array before reaching an affected output.

$t_{su(1)}$ — Minimum time interval that must be allowed between the data edge on any dedicated input and the active clock edge on the clock input pin when data affects the S or R line of any output SR register.

$t_{su(2)}$ — Minimum time interval that must be allowed between the data edge on any dedicated input and the active clock edge on the clock input pin when data affects the S or R line of any internal SR register.

$t_{su(a)}$ — Minimum time interval that must be allowed between the data edge on any dedicated input and the active clock edge on the clock input pin when data passes once through a C-array before reaching an affected S or R line on any internal SR register.

$t_{su(b)}$ — Minimum time interval that must be allowed between the data edge on any dedicated input and the active clock edge on the clock input pin when data passes once through a C-array before reaching an affected S or R line on any output SR register.

$t_{min(1)}$ — Minimum clock period (or 1/[maximum frequency]) that the device will accommodate when using feedback from any internal SR register or counter bit to feed the S or R line of any output SR register.

$t_{min(2)}$ — Minimum clock period (or 1/[maximum frequency]) that the device will accommodate when using feedback from any internal SR register to feed the S or R line of any internal SR register.

$t_{min(3)}$ — Minimum clock period (or 1/[maximum frequency]) that the device will accommodate when using feedback from any internal SR register to feed the S or R line of any internal SR register and data passes once through a C-array before reaching an affected S or R line on any internal SR register.

$t_{min(c)}$ — Minimum clock period (or 1/[maximum frequency]) that the device will accommodate when using feedback from any internal SR register to feed the S or R line of any output SR register and data passes once through a C-array before reaching an affected S or R line on any output SR register.

PARAMETER VALUES FOR TIMING MODEL

$t_{pd(1)}$ = 20 ns	$t_{su(1)}$ = 12 ns[†]	$t_{min(1)}$ = 20 ns
$t_{pd(2)}$ = 10 ns	$t_{su(2)}$ = 12 ns[†]	$t_{min(2)}$ = 20 ns
$t_{pd(3)}$ = 25 ns	$t_{su(a)}$ = 25 ns	$t_{min(3)}$ = 25 ns
	$t_{su(b)}$ = 25 ns	$t_{min(c)}$ = 25 ns

INTERNAL NODE NUMBERS

Q0-Q7	RESET 25-32	P0-P15	SET 33-48
C0	65		RESET 49-64
C1	66		

[†] Use tsu = 20 ns for applications where the setup time for S/R↓ inputs are required.

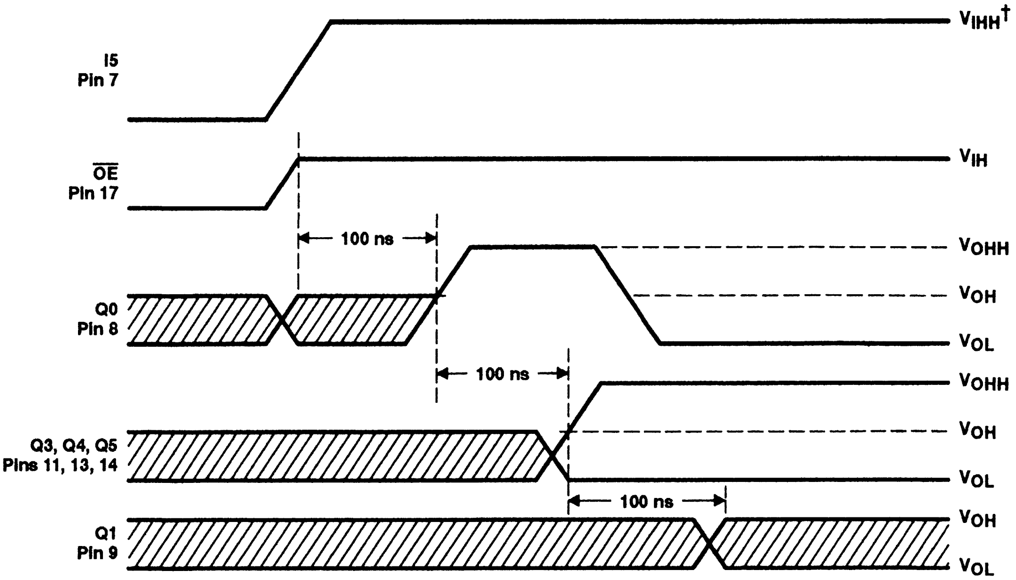
diagnostics

A diagnostic mode is provided with these devices that allows the user to inspect the contents of the state registers. The step-by-step procedures required to use the diagnostics follow.

Step 1. Disable all outputs by taking pin 17 ($\overline{OE}$) high (see Note 4).
Step 2. Take pin 8 (Q0) to V_{IHH} to enable the diagnostics test sequence.
Step 3. Apply appropriate levels of voltage to pins 11 (Q3), 13 (Q4), and 14 (Q5) to select the desired state register (see Table 1).

The voltage level monitored on pin 9 will indicate the state of the selected state register.

NOTE 4: If pin 17 is being used as an input to the array, then pin 7 (I5) must be taken to V_{IHH} before pin 17 is taken high.



[†] V_{IHH} = 10.25 V min, 10.5 V nom, 10.75 V max

Figure 2. Diagnostics Waveforms

Table 1. Addressing State Registers During Diagnostics†

REGISTER BINARY ADDRESS			BURIED REGISTER SELECTED
PIN 11	PIN13	PIN 14	
L	L	L	C1
L	L	H	P15
L	L	HH	C0
L	H	L	P14
L	H	H	P0
L	H	HH	P1
L	HH	L	P2
L	HH	H	P3
L	HH	HH	P4
H	L	L	P5
H	L	H	P6
H	L	HH	P7
H	H	L	P8
H	H	H	P9
H	H	HH	P10
H	HH	L	P11
H	HH	H	P12
H	HH	HH	P13

† V_{IHH} = 10.25 V min, 10.5 V nom, 10.75 V max

programming information

Texas Instruments programmable logic devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers that are capable of programming Texas Instruments programmable logic is also available, upon request, from the nearest TI sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

OR term loading

As shown in Figure 3 and by the f_{max} calculations, f_{max} is affected by the number of terms connected to each OR array line. Theoretically, f_{max} is calculated as:

$$f_{max} = \frac{1}{t_{su} + t_{pd}\ \text{CLK to Q}}$$

Since the setup time (input or feedback to S/R↓) varies with the number of terms connected to each OR array line, (due to capacitance loading) f_{max}will also vary. Figure 3 illustrates the relationship between the number of terms connected per OR line and the setup time.

Use Figure 3 to determine the worst-case setup time for a particular application. Identify the OR array line with the maximum number of terms connected. Count the number of terms and use the graph to determine the setup time.

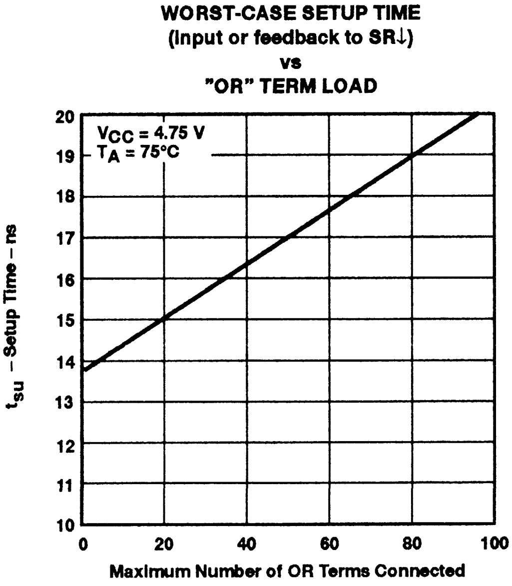


Figure 3

f_{max} with external feedback

The configuration shown is a typical state-machine design with feedback signals sent off-chip. This external feedback could go back to the device inputs or to a second device in a multi-chip state machine. The slowest path defining the clock period is the sum of the clock-to-output delay time and the setup time for the input or feedback signals (t_{su} + t_{pd} CLK to Q).

Thus: f_{max} with external feedback = $\dfrac{1}{t_{su} + t_{pd}\ \text{CLK to Q}}$

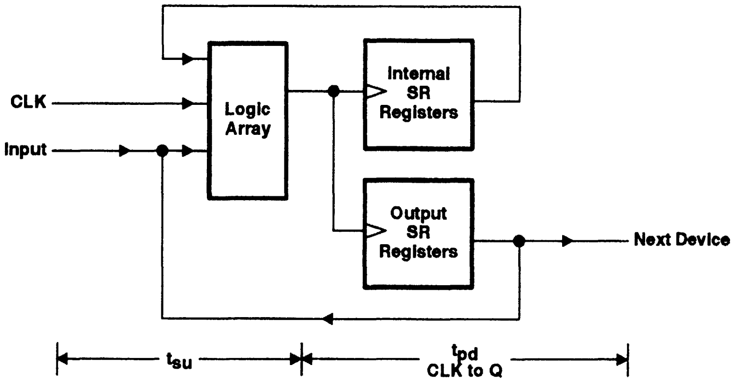
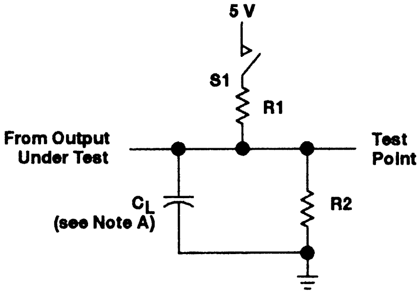
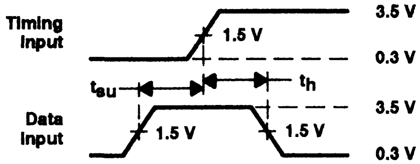


Figure 4

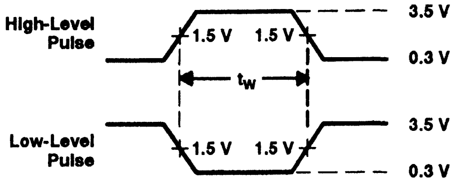
PARAMETER MEASUREMENT INFORMATION



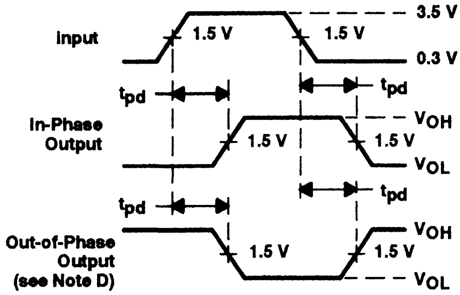
LOAD CIRCUIT FOR
3-STATE OUTPUTS



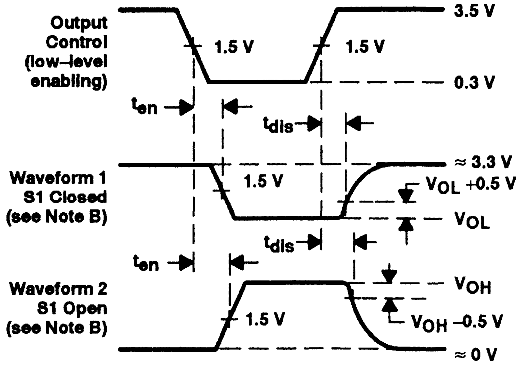
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f \leq 2$ ns, duty cycle = 50%.
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.
E. Equivalent loads may be used for testing.

Figure 5. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

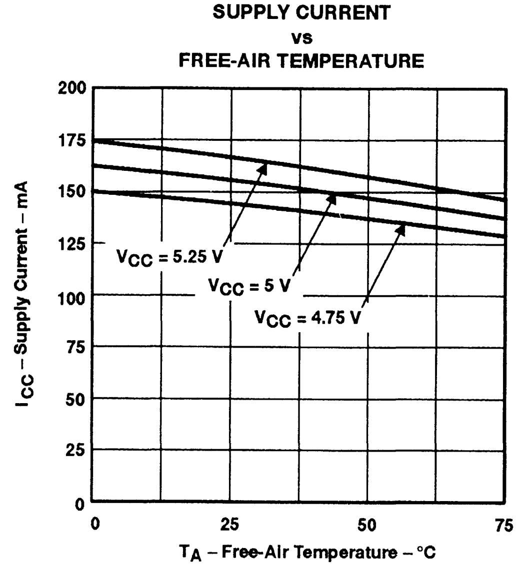


Figure 6

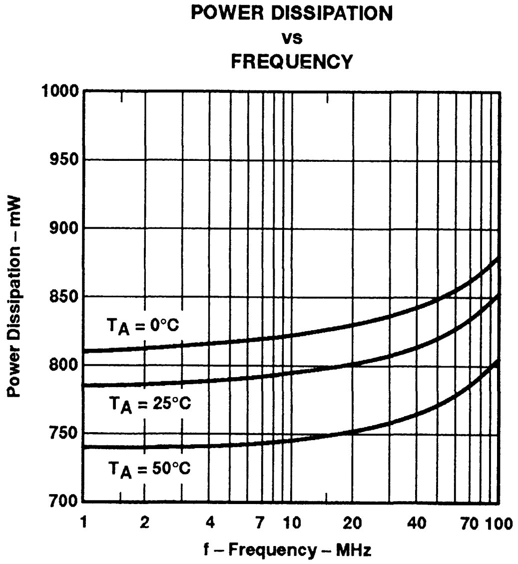


Figure 7

TYPICAL CHARACTERISTICS

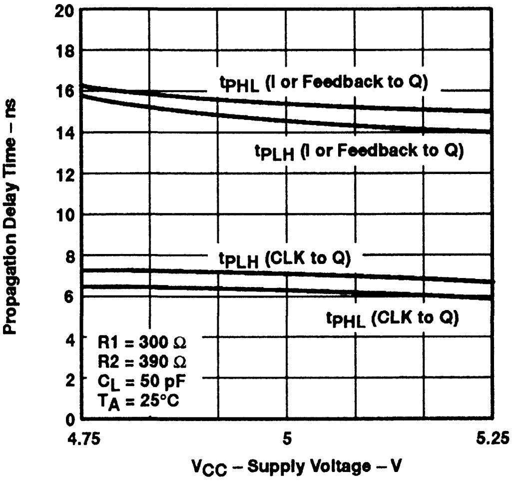

PROPAGATION DELAY TIME
vs
SUPPLY VOLTAGE

Figure 8

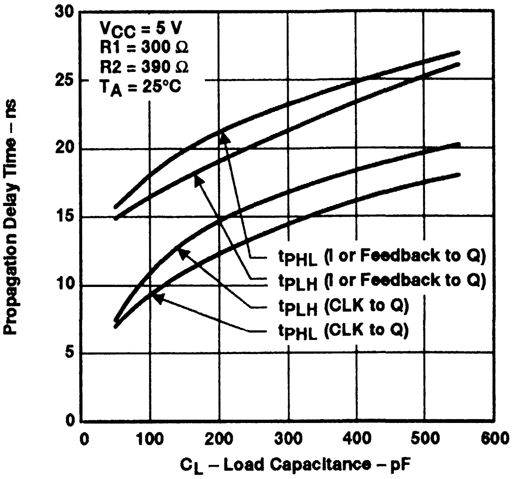

PROPAGATION DELAY TIME
vs
LOAD CAPACITANCE

Figure 9

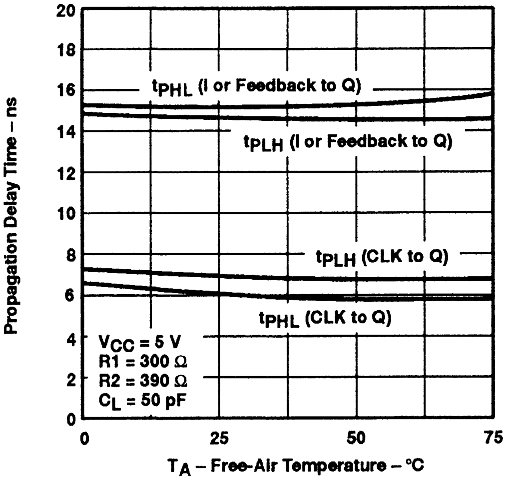

PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

Figure 10

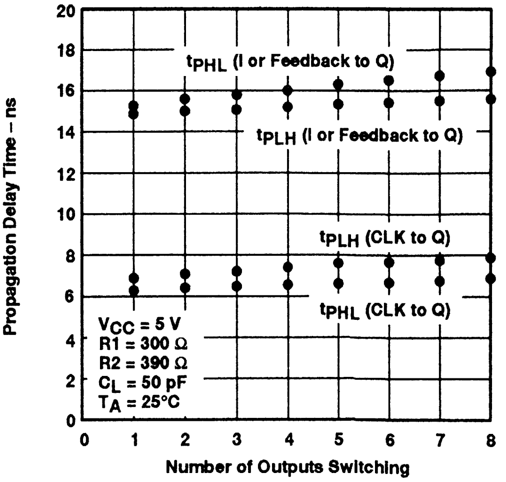

PROPAGATION DELAY TIME
vs
NUMBER OF OUTPUTS SWITCHING

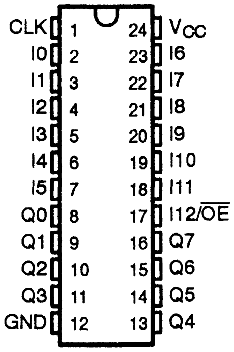
Figure 11

TIBPSG507AC
13 × 80 × 8 PROGRAMMABLE SEQUENCE GENERATOR

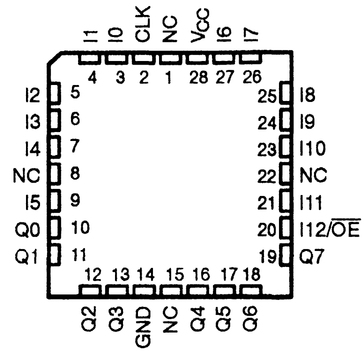
SRPS002C – D3029, MAY 1987 – REVISED MARCH 1992

- **58-MHz Max Clock Rate**
- **Ideal for Waveform Generation and High-Performance State Machine Applications**
- **6-Bit Internal Binary Counter**
- **8-Bit Internal State Register**
- **Programmable Clock Polarity**
- **Outputs Programmable for Registered or Combinational Operation**
- **6-Bit Counter Simplifies Logic Equation Development in State Machine Designs**
- **Programmable Output Enable**

JT OR NT PACKAGE
(TOP VIEW)



FK OR FN PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TIBPSG507AC is a 13 × 80 × 8 Programmable Sequence Generator (PSG) that offers the system designer unprecedented flexibility in a high-performance field-programmable logic device. Applications such as waveform generators, state machines, dividers, timers, and simple logic reduction are all possible with the PSG. By utilizing the built-in binary counter, the PSG is capable of generating complex timing controllers. The binary counter also simplifies logic equation development in state machine and waveform generator applications.

The TIBPSG507AC contains 80 product (AND) terms, a 6-bit binary counter with control logic, eight S/R state holding registers, and eight outputs. The eight outputs can be individually programmed for either registered or combinational operation. The clock input is fuse programmable for either positive- or negative-edge operation.

The 6-bit binary counter is controlled by a synchronous-clear and a count/hold function. Each control function has a nonregistered and registered option. When either SCLR0 or SCLR1 is taken high, the counter resets to zero on the next active clock edge. When either $\overline{\mathrm{CNT}}$/HLD0 or $\overline{\mathrm{CNT}}$/HLD1 is taken high, the counter is held at the present count and is not allowed to advance on the active clock edge. The SCLR function overrides the $\overline{\mathrm{CNT}}$/HLD feature when both lines are simultaneously high.

Clock polarity is programmable through the clock polarity fuse. Leaving this fuse intact selects positive-edge triggering. Negative-edge triggering is selected by blowing this fuse. Pin 17 functions as an input and/or an output enable. When the output enable fuse is intact, all outputs are always enabled allowing pin 17 to be used strictly as an input. Blowing the output enable fuse lets pin 17 function as an output enable and an input. In this mode, the outputs are enabled when pin 17 is low and are in a high-impedance state when pin 17 is high.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 1992, Texas Instruments Incorporated

TEXAS INSTRUMENTS

POST OFFICE BOX 655303 • DALLAS, TEXAS 75265

description (continued)

The eight outputs can be individually programmed for combinational operation by blowing the output multiplexer fuse. After power up, the device must be initialized to the desired state. When the output multiplexer fuse is left intact, registered operation is selected.

The TIBPSG507AC is characterized for operation from 0°C to 75°C.

6-BIT COUNTER CONTROL FUNCTION TABLE (see Note 1)

$\overline{\text{CNT}}$/HLD1	$\overline{\text{CNT}}$/HLD0	SCLR1	SCLR0	OPERATION
L	L	L	L	counter active
X	X	X	H	synchronous clear
X	X	H	X	synchronous clear
X	H	L	L	hold counter
H	X	L	L	hold counter

NOTE 1: When all fuses are blown on a product line (AND), its output will be high. When all fuses are blown on a sum line (OR), its output will be low. All product and sum terms are low on devices with fuses intact.

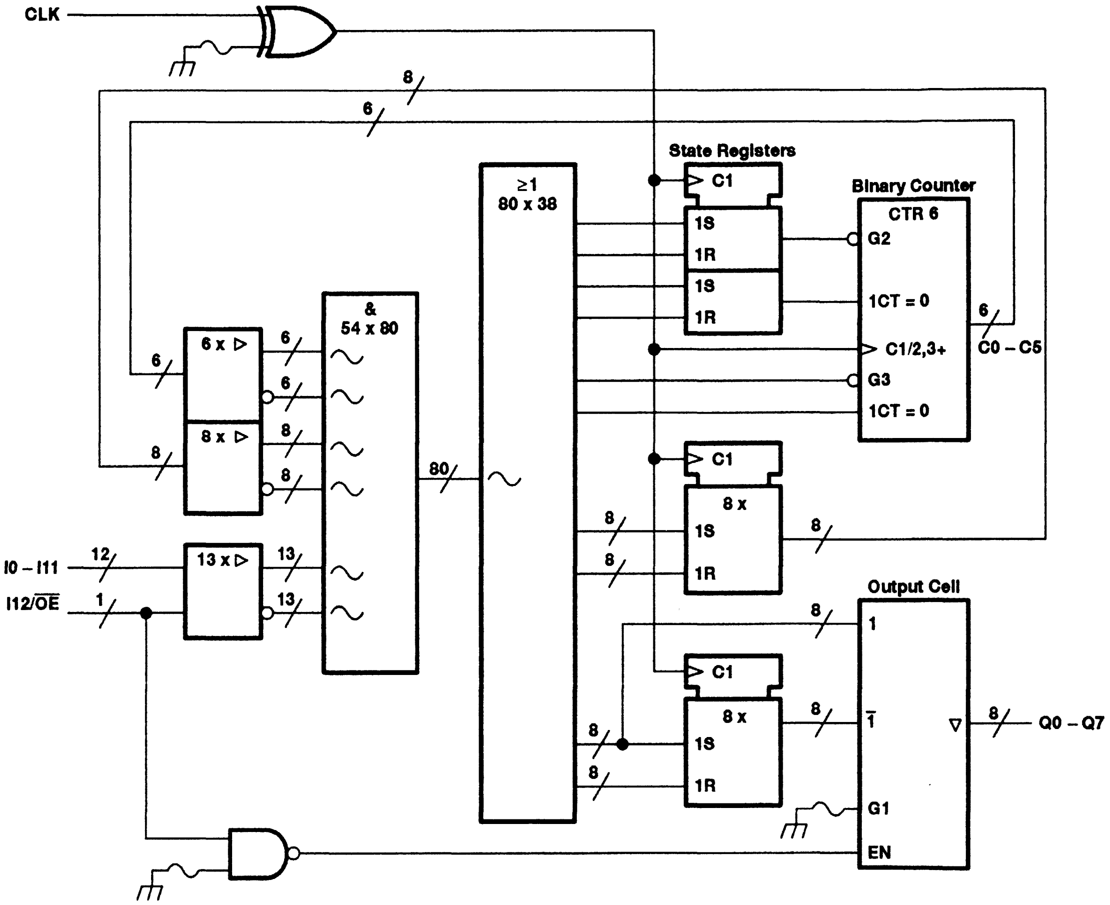
S/R FUNCTION TABLE (see Note 2)

CLK POLARITY FUSE	CLK	S	R	STATE REGISTER
INTACT	↑	L	L	Q_0
INTACT	↑	L	H	L
INTACT	↑	H	L	H
INTACT	↑	H	H	INDET[†]
BLOWN	↓	L	L	Q_0
BLOWN	↓	L	H	L
BLOWN	↓	H	L	H
BLOWN	↓	H	H	INDET[†]

[†] Output state is indeterminate

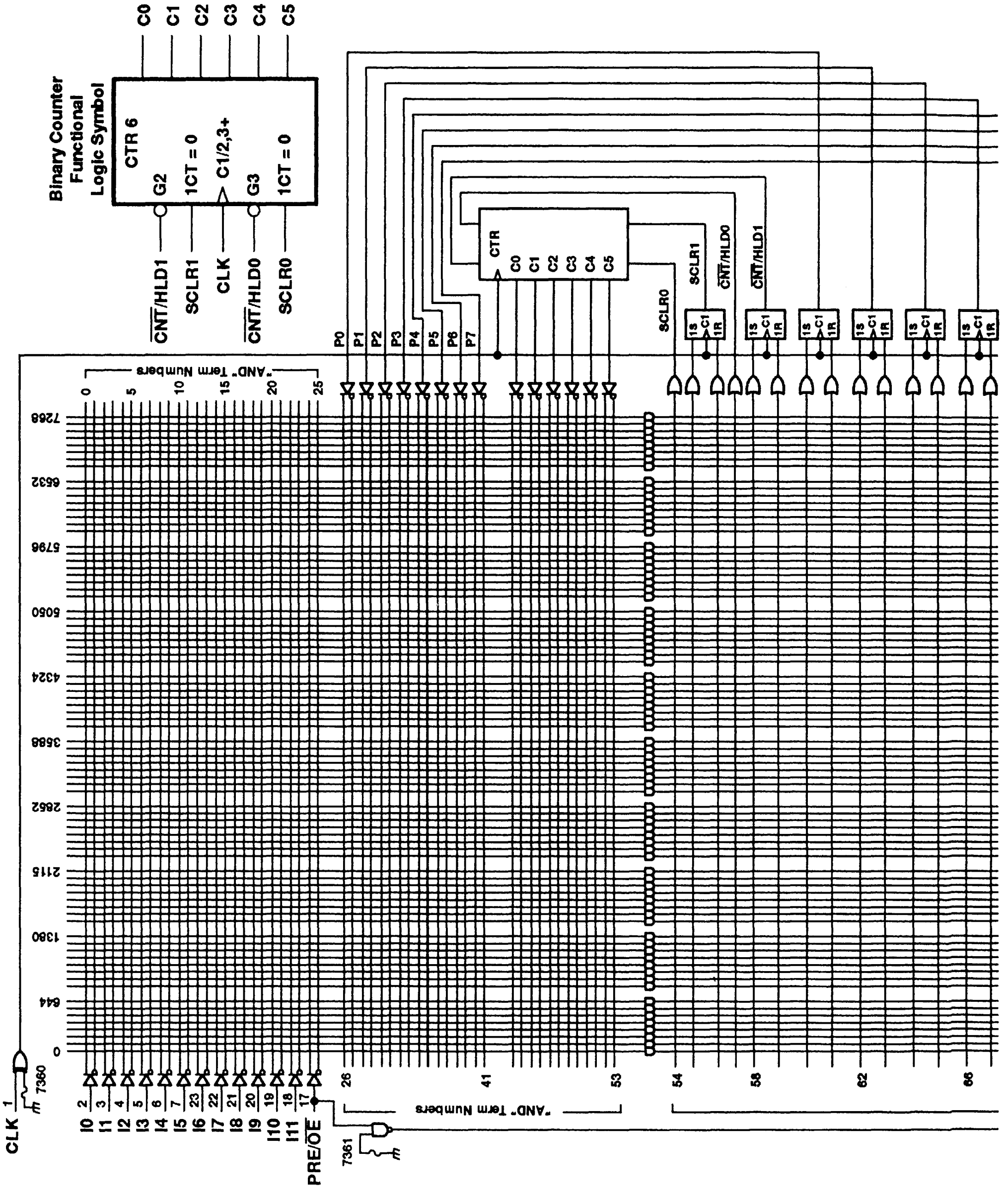
NOTE 2: After power up, the device must be initialized to its desired state. Q_0 is the state of the S/R register before the active clock edge.

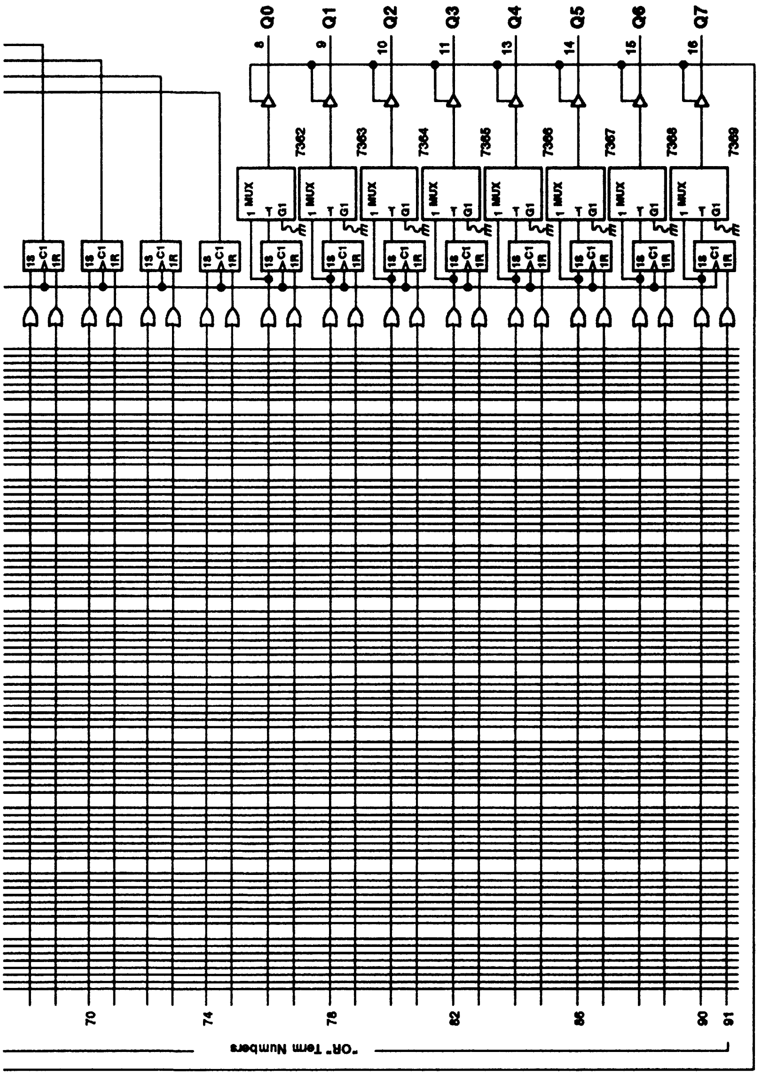
functional block diagram (positive logic)



∿ denotes fused inputs

logic diagram (positive logic)





All inputs to AND gates, exclusive-OR gates, and multiplexers with a blown link assume the logic-1 state.
All OR gate inputs with a blown link assume the logic-0 state.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 3)	7 V
Input voltage (see Note 3)	5.5 V
Voltage applied to disabled output (see Note 3)	5.5 V
Operating free-air temperature range	0°C to 75°C
Storage temperature range	−65°C to 150°C

NOTE 3: These ratings apply except for programming pins during a programming cycle or during the diagnostic mode.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−3.2	mA
I_{OL}	Low-level output current				16	mA
t_w	Pulse duration	Clock high	6			ns
		Clock low	6			
t_{su}	Setup time before CLK active transition[†]	Input or feedback to S/R↑ inputs	12			ns
		Input or feedback to S/R↓ inputs[‡]	19			
		Input or feedback to SCLR0	20			
		Input or feedback to $\overline{\text{CNT}}$/HLD0	25			
t_h	Hold time after CLK active transition[†]	Input or feedback at S/R inputs	0			ns
		Input or feedback at SCLR0	0			
		Input or feedback at $\overline{\text{CNT}}$/HLD0	0			
T_A	Operating free-air temperature		0	25	75	°C

[†] Internal setup and hold times, t_{su} feedback to SCLR1, feedback to $\overline{\text{CNT}}$/HLD1; t_h feedback at SCLR1 and feedback at $\overline{\text{CNT}}$/HLD1, are guaranteed by f_{max} specifications. The active transition of CLK is determined by the programmed state of the CLK polarity fuse.

[‡] See the OR term loading section and Figure 3.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP[†]	MAX	UNIT
V_{IK}	V_{CC} = 4.75 V,	I_I = –18 mA				–1.2	V
V_{OH}	V_{CC} = 4.75 V,	I_{OH} = –3.2 mA		2.4	3.2		V
V_{OL}	V_{CC} = 4.75 V,	I_{OL} = 16 mA			0.25	0.5	V
I_{OZH}	V_{CC} = 5.25 V,	V_O = 2.7 V				20	µA
I_{OZL}	V_{CC} = 5.25 V,	V_O = 0.4 V				–20	µA
I_I	V_{CC} = 5.25 V,	V_I = 5.5 V				0.1	mA
I_{IH}	V_{CC} = 5.25 V,	V_I = 2.7 V				20	µA
I_{IL}	V_{CC} = 5.25 V,	V_I = 0.4 V				–0.25	mA
I_O[‡]	V_{CC} = 5.25 V,	V_O = 0.5 V		–30		–130	mA
I_{CC}	V_{CC} = 5.25 V,	See Note 4,	Outputs open		156	210	mA
C_i	f = 1 MHz,	V_I = 2 V			7		pF
C_o	f = 1 MHz,	V_O = 2 V			11		pF
C_{clk}	f = 1 MHz,	V_{CLK} = 2 V			14		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	TYP[†]	MAX	UNIT
f_{max}[§]	6-Bit counter with SCLR1 or $\overline{\text{CNT}}$/HLD1		R1 = 300 Ω, R2 = 390 Ω, See Figure 6	58	65		MHz
	6-Bit counter with SCLR0			40	55		
	6-Bit counter with $\overline{\text{CNT}}$/HLD0			33	50		
	With external feedback (see Figure 1)			45	60		
t_{pd}[¶]	CLK	Q (nonregistered)[#]		6		25	ns
		Q (registered)		3		10	
	I or Feedback	Q (nonregistered)		6		20	ns
t_{en}	$\overline{\text{OE}}$↓	Q		1	6	10	ns
t_{dis}	$\overline{\text{OE}}$↑	Q		1	6	10	ns

[†] All typical values are at V_{CC} = 5 V, T_A = 25°C.

[‡] This parameter approximates I_{OS}. The condition V_O = 0.5 V takes tester noise into account. Not more than one output should be shorted at a time and duration of the short circuit should not exceed one second.

[§] See the f_{max} calculations section.

[¶] The active edge of CLK is determined by the programmed state of the CLK polarity fuse.

[#] t_{pd} CLK to Q (nonregistered) is the same for data clocked from the counter or state registered.

NOTE 4: When the clock is programmed for negitive edge, then V_I = 4.5 V. When the clock is programmed for positive edge, then V_I = 0.

f_{max} calculations

The following are the different speeds that can be achieved when using the TIBPSG507AC as a state machine. The way the 6-bit counter is controlled will largely determine the operating frequency of the state machine.

f_{max} for a 6-bit counter using SCLR1 or $\overline{\text{CNT}}$/HLD1 = $\frac{1}{t_{su} + t_{pd}\ \text{CLK to Q}}$ where setup time t_{su} for input or feedback to the S/R inputs = 12 ns and propagation delay time t_{pd} CLK to Q for the internal S/R registers = 5 ns (difference in t_{pd} from CLK and feedback, 25 to 20).

Thus: f_{max} for this condition = $\frac{1}{(12 + 5)\ \text{ns}} = \frac{1}{17\ \text{ns}} = 58$ MHz.

f_{max} for a 6-bit counter using SCLR0 for reset = $\frac{1}{t_{su} + t_{pd}\ \text{CLK to Q}}$ where setup time t_{su} for input or feedback to the SCLR0 inputs = 20 ns and propagation delay time t_{pd} CLK to Q for the internal S/R registers = 5 ns (difference in t_{pd} from CLK and feedback, 25 to 20)

Thus: f_{max} for this condition = $\frac{1}{(20 + 5)\ \text{ns}} = \frac{1}{25\ \text{ns}} = 40$ MHz.

f_{max} for a 6-bit counter using $\overline{\text{CNT}}$/HLD0 for reset = $\frac{1}{t_{su} + t_{pd}\ \text{CLK to Q}}$ where setup time t_{su} for input or feedback to $\overline{\text{CNT}}$/HLD0 = 25 ns and propagation delay time t_{pd} CLK to Q for the internal S/R registers = 5 ns (difference in t_{pd} from CLK and feedback, 25 to 20).

Thus: f_{max} for this condition = $\frac{1}{(25 + 5)\ \text{ns}}. = \frac{1}{30\ \text{ns}} = 33$ MHz.

programming information

Texas Instruments programmable logic devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers that are capable of programming Texas Instruments programmable logic is also available, upon request, from the nearest TI sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

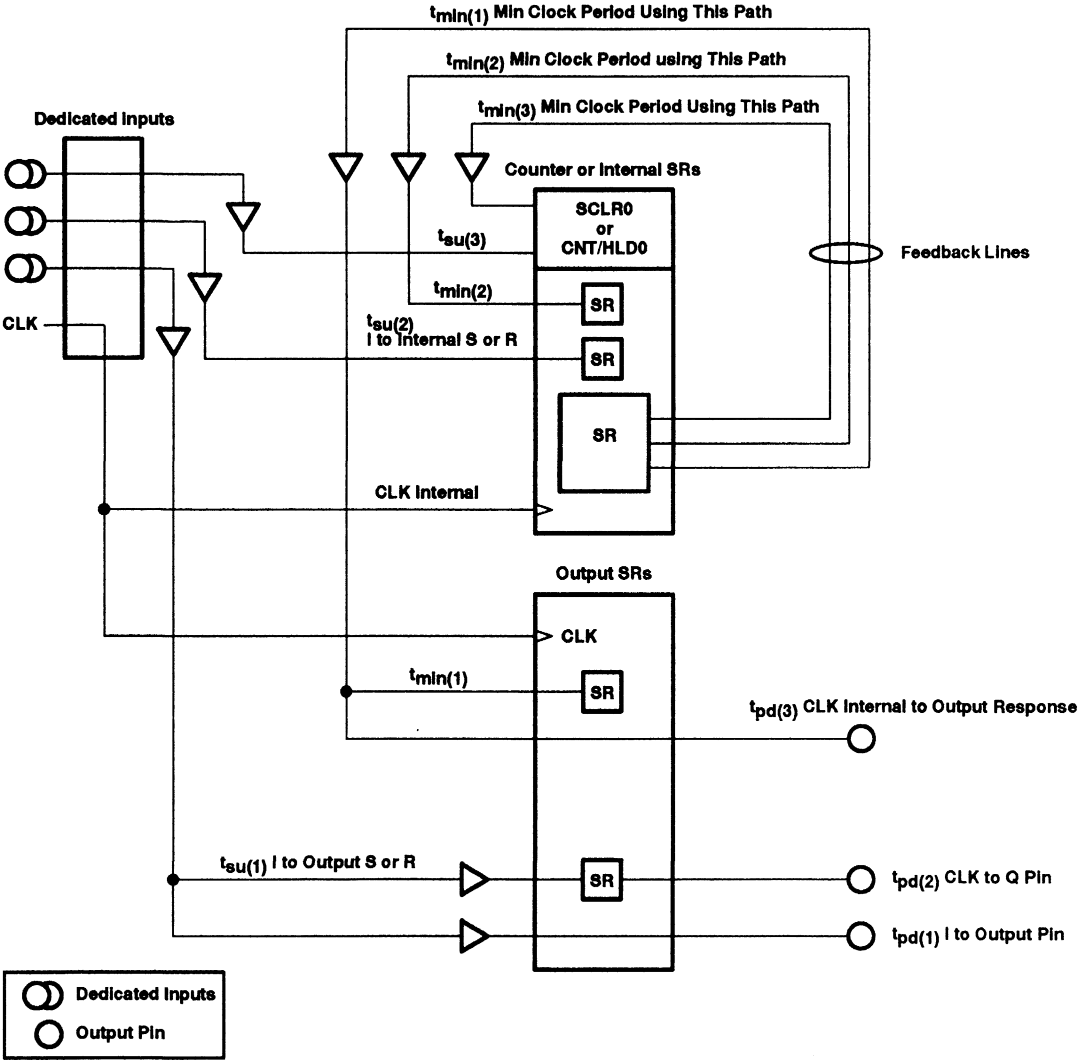


Figure 1. Timing Model

glossary — timing model

$t_{pd(1)}$ — Maximum time interval from the time a signal edge is received at any input pin to the time any logically affected combinational output pin delivers a response.

$t_{pd(2)}$ — Maximum time interval from a positive edge on the clock input pin to data delivery on the output pin corresponding to any output SR register.

$t_{pd(3)}$ — Maximum time interval from the positive edge on the clock input pin to the response on any logically affected combinational configured output (at the pin), where data origin is any internal SR register or counter bit.

$t_{su(1)}$ — Minimum time interval that must be allowed between the data edge on any dedicated input and the active clock edge on the clock input pin when data affects the S or R line of any output SR register.

$t_{su(2)}$ — Minimum time interval that must be allowed between the data edge on any dedicated input and the active clock edge on the clock input pin when data affects the S or R line of any internal SR register.

$t_{su(3)}$ — Minimum time interval that must be allowed between the data edge on any dedicated input and the active clock edge on the clock input pin only when entering data on the $\overline{\text{CNT}}$/HLD0 line.

$t_{su(4)}$ — Minimum time interval that must be allowed between the data edge on any dedicated input and the active clock edge on the clock input pin only when entering data on the SCLR0 line.

$t_{min(1)}$ — Minimum clock period (or 1/[maximum frequency]) that the device will accommodate when using feedback from any internal SR register or counter bit to feed the S or R line of any output SR register.

$t_{min(2)}$ — Minimum clock period (or 1/[maximum frequency]) that the device will accommodate when using feedback from any internal SR register to feed the S or R line of any internal SR register.

$t_{min(3)}$ — Minimum clock period (or 1/[maximum frequency]) that the device will accommodate when using feedback from any internal SR register or counter bit to feed SCLR0 or $\overline{\text{CNT}}$/HLD0.

PARAMETER VALUES FOR TIMING MODEL

$t_{pd(1)}$ = 20 ns
$t_{pd(2)}$ = 10 ns
$t_{pd(3)}$ = 25 ns

$t_{su(1)}$ = 12 ns†
$t_{su(2)}$ = 12 ns†
$t_{su(3)}$ = 25 ns
$t_{su(4)}$ = 20 ns

$t_{min(1)}$ = 17 ns
$t_{min(2)}$ = 17 ns
$t_{min(3)}$ = 25 ns

INTERNAL NODE NUMBERS

SCLR0	25	CNTHLD0	28	P0-P7	SET 31-38
SCLR1	SET 26	CNTHLD1	SET 29		RESET 39-46
	RESET 27		RESET 30	Q0-Q7	RESET 47-54
		C0-C5	55-60		

† Use t_{su} = 19 ns for applications where the setup time for S/R↓ inputs are required.

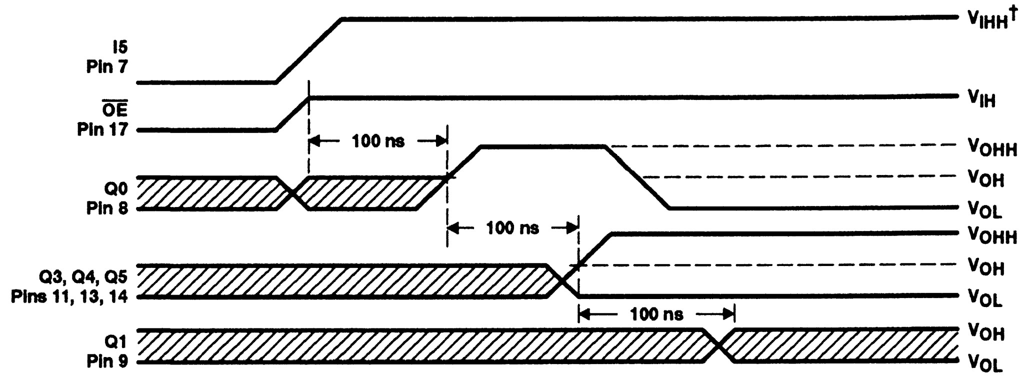
diagnostics

A diagnostic mode is provided that allows the user to inspect the contents of the state registers. The following are step-by-step procedures required for the diagnostics.

Step 1. Disable all outputs by taking pin 17 ($\overline{\text{OE}}$) high (see Note 5).
Step 2. Take pin 8 (Q0) to V_{IHH} to enable the diagnostics test sequence.
Step 3. Apply appropriate levels of voltage to pins 11 (Q3), 13 (Q4), and 14 (Q5) to select the desired state register (see Table 1).

The voltage level monitored on pin 9 will indicate the state of the selected state register.

NOTE 5: If pin 17 is being used as an input to the array, then pin 7 (I5) must be taken to V_{IHH} before pin 17 is taken high.



† V_{IHH} = 10.25 V min, 10.5 V nom, 10.75 V max

Figure 2. Diagnostics Waveforms

Table 1. Addressing State Registers During Diagnostics

REGISTER BINARY ADDRESS			BURIED REGISTER SELECTED
PIN 11	PIN13	PIN 14	
L	L	L	SCLR0
L	L	H	SCLR1
L	L	HH	$\overline{\text{CNT}}$/HLD0
L	H	L	$\overline{\text{CNT}}$/HLD1
L	H	H	P0
L	H	HH	P1
L	HH	L	P2
L	HH	H	P3
L	HH	HH	P4
H	L	L	P5
H	L	H	P6
H	L	HH	P7
H	H	L	C0
H	H	H	C1
H	H	HH	C2
H	HH	L	C3
H	HH	H	C4
H	HH	HH	C5

PRINCIPLES OF OPERATION

PSG design theory

Most state machine and waveform generator designs can be simplified with the PSG by referencing all or part of each sequence to a binary count. The internal state registers can then be used to keep track of which binary count sequence is in operation, to store input data and keep track of internally generated status bits, or as output registers when connected to a nonregistered output cell. State registers can also be used to expand the binary counter when a larger counter is needed.

Through the use of the binary counter, the number of product lines and state registers required for a design is usually reduced. In addition, the designer does not have to be concerned about generating wait states where the outputs are unaffected because these can be timed from the binary counter. For detailed information and examples using this design concept, see *A Designer's Guide to the TIBPSG507* located in the applications report section of the *Programmable Logic Data Book*, 1993.

OR term loading

As shown in Figure 3 and by the f_{max} calculation, f_{max} is affected by the number of terms connected to each OR array line. Theoretically, f_{max} is calculated as:

$$f_{max} = \frac{1}{t_{su} + t_{pd}\ \text{CLK to Q}}$$

Since the setup time (input or feedback to S/R↓) varies with the number of terms connected to each OR array line, (due to capacitance loading) f_{max} will also vary. Figure 3 illustrates the relationship between the number of terms connected per OR line and the setup time.

Use Figure 3 to determine the worst-case setup time for a particular application. Identify the OR array line with the maximum number of terms connected. Count the number of terms and use the graph to determine the setup time.

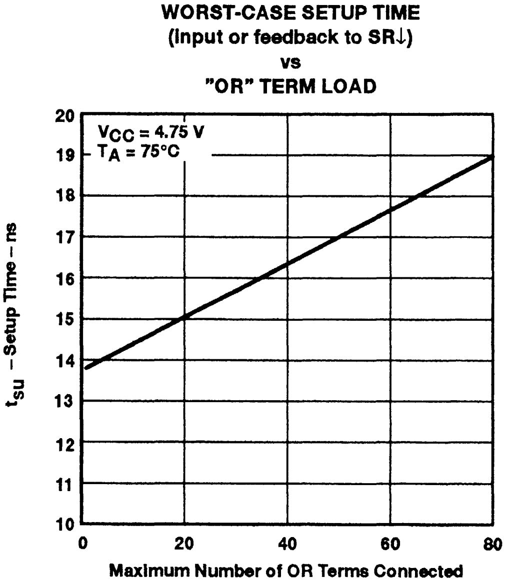


Figure 3

f_{max} with external feedback

The configuration shown is a typical state-machine design with feedback signals sent off-chip. This external feedback could go back to the device inputs or to a second device in a multi-chip state machine. The slowest path defining the clock period is the sum of the clock-to-output delay time and the setup time for the input or feedback signals (t_{su} + t_{pd} CLK to Q).

$$\text{Thus: } f_{max} \text{ with external feedback} = \frac{1}{t_{su} + t_{pd} \text{ CLK to Q}}$$

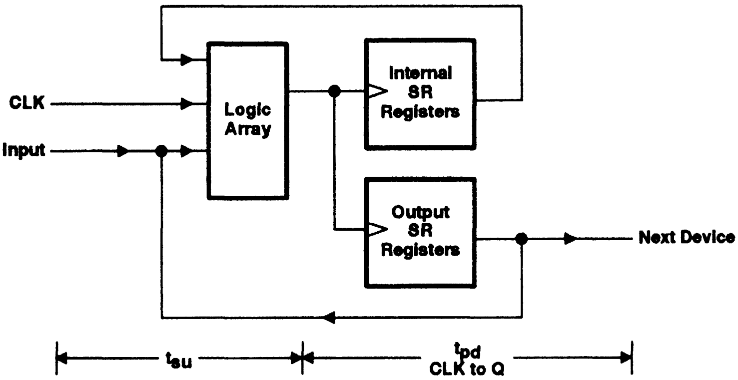
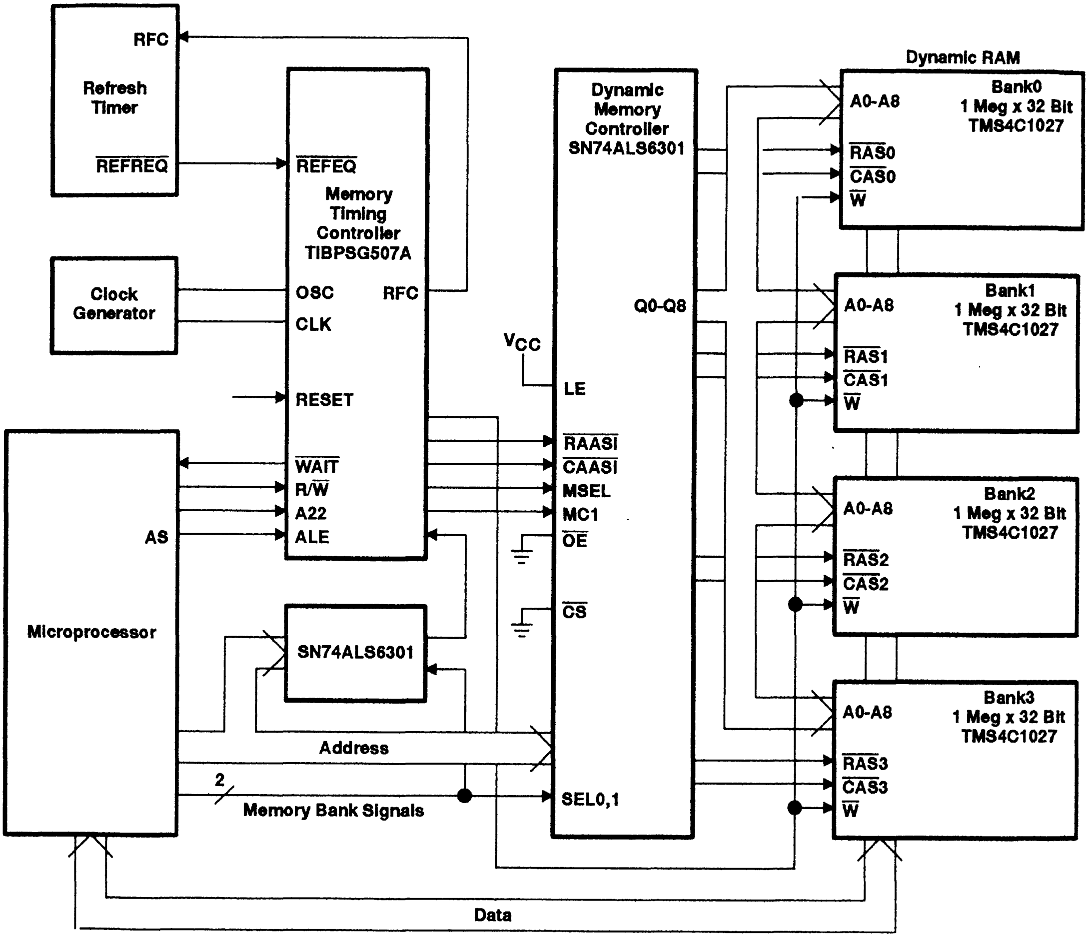


Figure 4

APPLICATION INFORMATION

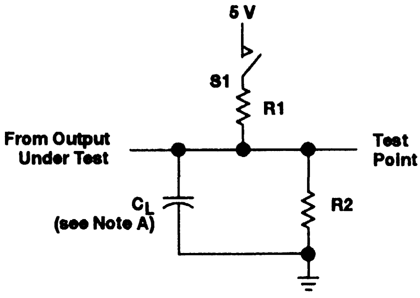
The TIBPSG507AC is used in this application to generate the required memory timing control signals ($\overline{RAS}$, $\overline{CAS}$, etc.) for the memory timing controller.



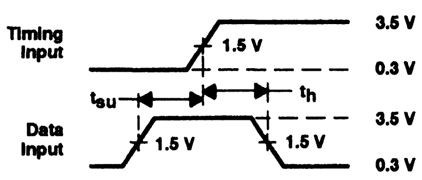
For detailed information, please see the *Systems Solution for Static Column Decode* Application Report.

Figure 5

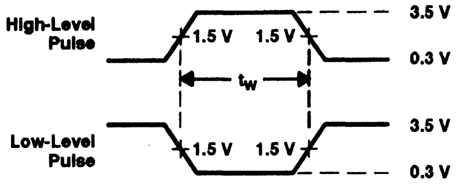
PARAMETER MEASUREMENT INFORMATION



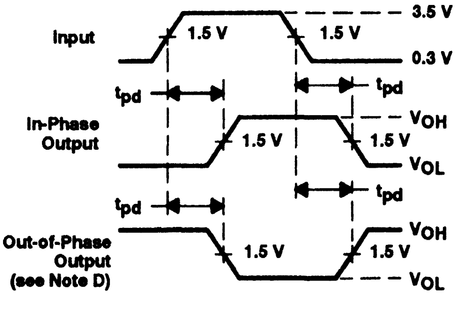
LOAD CIRCUIT FOR 3-STATE OUTPUTS



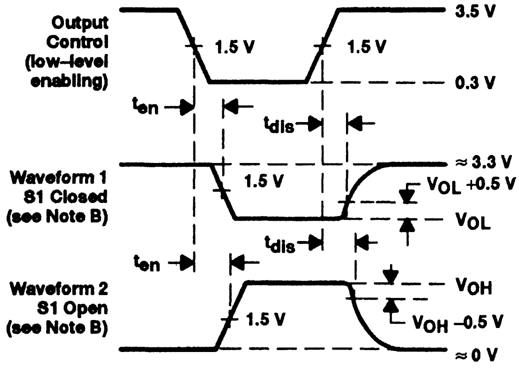
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATIONS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.

B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

C. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f \leq 2$ ns, duty cycle = 50%.

D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.

E. Equivalent loads may be used for testing.

Figure 6. Load Circuit and Voltage Waveforms

TYPICAL CHARACTERISTICS

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

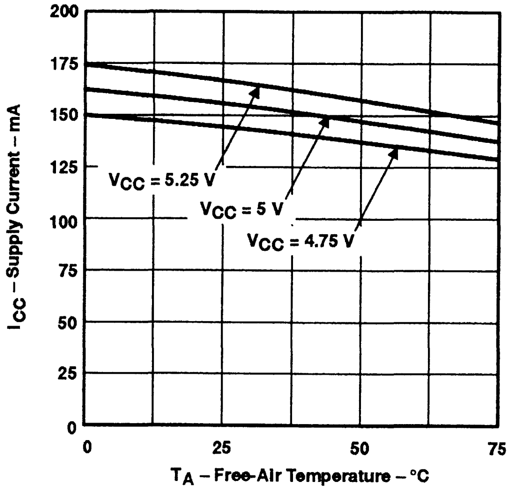


Figure 7

POWER DISSIPATION
vs
FREQUENCY

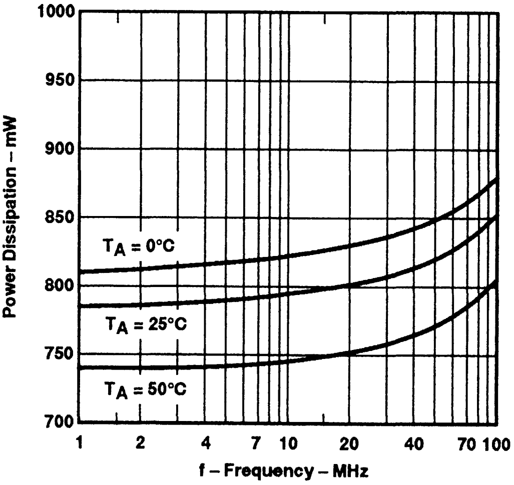


Figure 8

TYPICAL CHARACTERISTICS

PROPAGATION DELAY TIME
vs
SUPPLY VOLTAGE

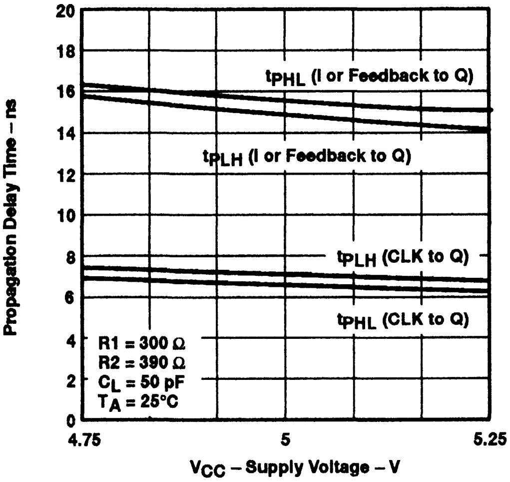


Figure 9

PROPAGATION DELAY TIME
vs
LOAD CAPACITANCE

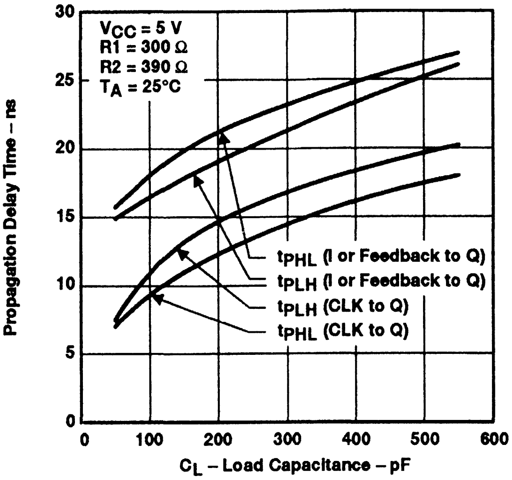


Figure 10

PROPAGATION DELAY TIME
vs
FREE-AIR TEMPERATURE

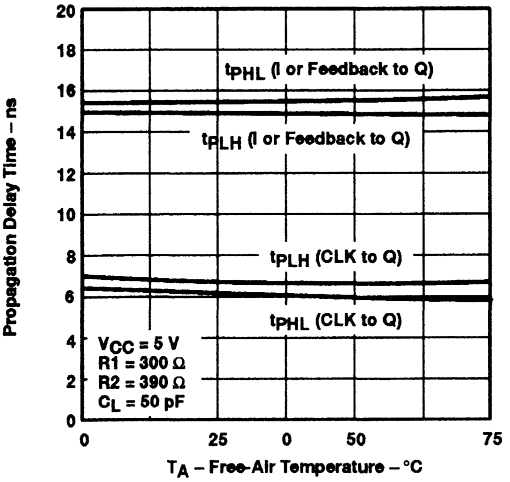


Figure 11

PROPAGATION DELAY TIME
vs
NUMBER OF OUTPUTS SWITCHING

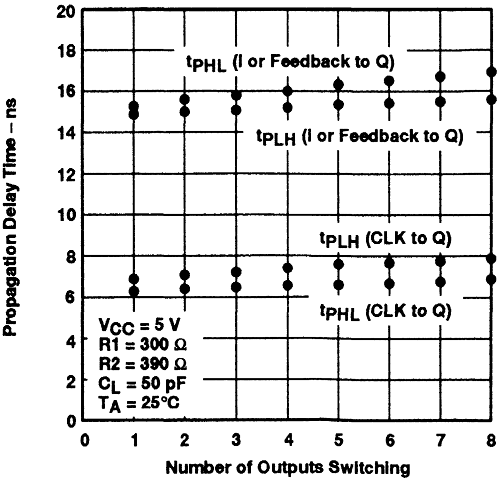


Figure 12

TIB82S105BC
16 × 48 × 8 FIELD-PROGRAMMABLE LOGIC SEQUENCER WITH 3-STATE OUTPUTS OR PRESET

SRPS025 – D2897, SEPTEMBER 1985 – REVISED MARCH 1992

- **50-MHz Clock Rate**
- **Power-On Preset of All Flip-Flops**
- **6-Bit Internal State Register With 8-Bit Output Register**
- **Power Dissipation . . . 600 mW Typical**
- **Programmable Asynchronous Preset or Output Control**
- **Functionally Equivalent to, but Faster Than 82S105A†**

description

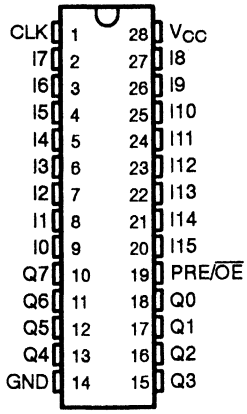
The TIB82S105BC is a TTL field-programmable state machine of the Mealy type. This state machine (logic sequencer) contains 48 product terms (AND terms) and 14 pairs of sum terms (OR terms). The product and sum terms are used to control the 6-bit internal state register and the 8-bit output register.

The outputs of the internal state register (P0–P5) are fed back and combined with the 16 inputs (I0–I15) to form the AND array. In addition a single sum term is complemented and fed back to the AND array, which allows any of the product terms to be summed, complemented, and used as an input to the AND array.

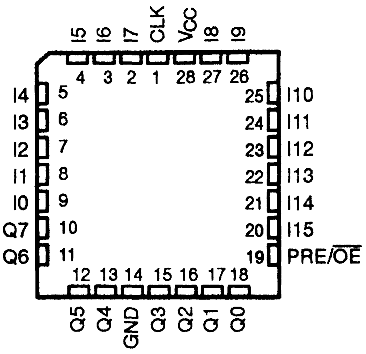
The state and output registers are positive-edge-triggered S/R flip-flops. These registers are unconditionally preset high during power up. Pin19 can be used to preset both registers or, by blowing the proper fuse, be converted to an output control function.

The TIB82S105BC is characterized for operation from 0°C to 75°C.

N PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



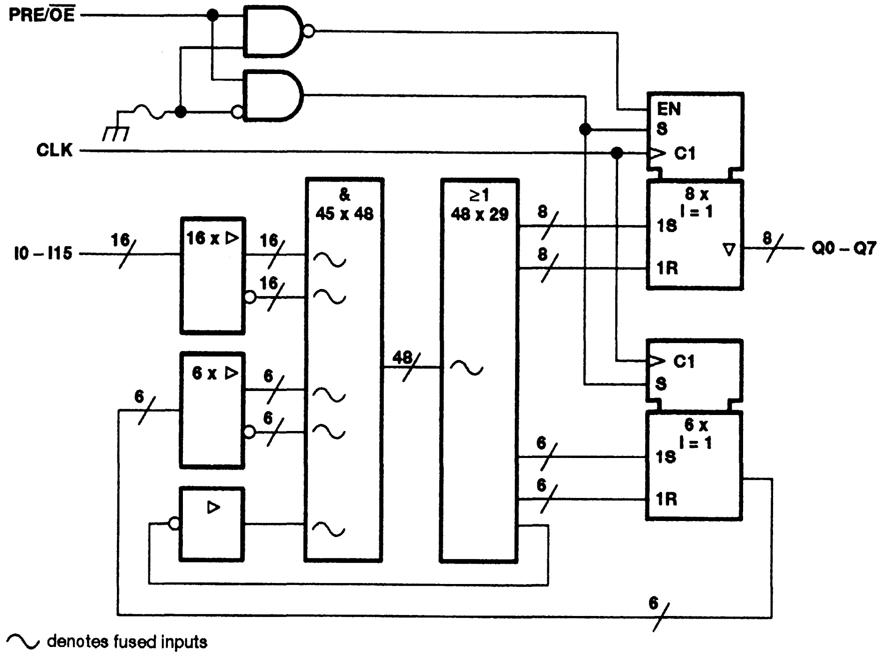
---

† Power-up preset and asynchronous preset functions are not identical to 82S105A. See Recommended Operating Conditions.

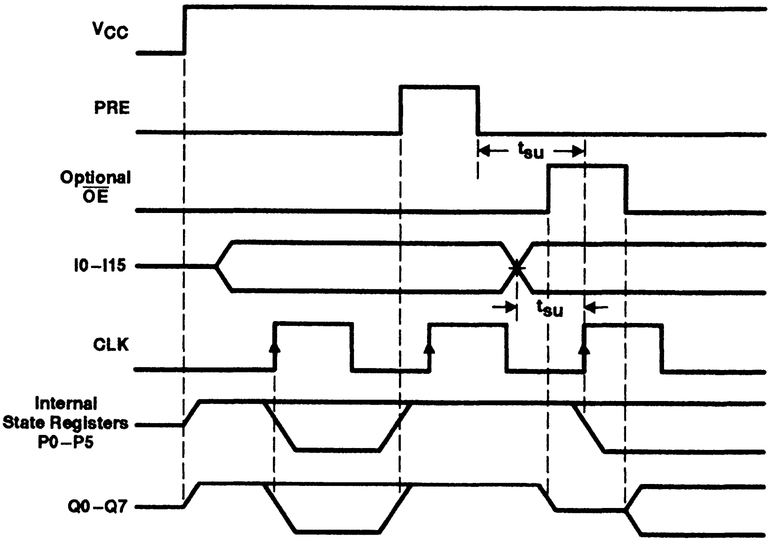
PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 1992, Texas Instruments Incorporated

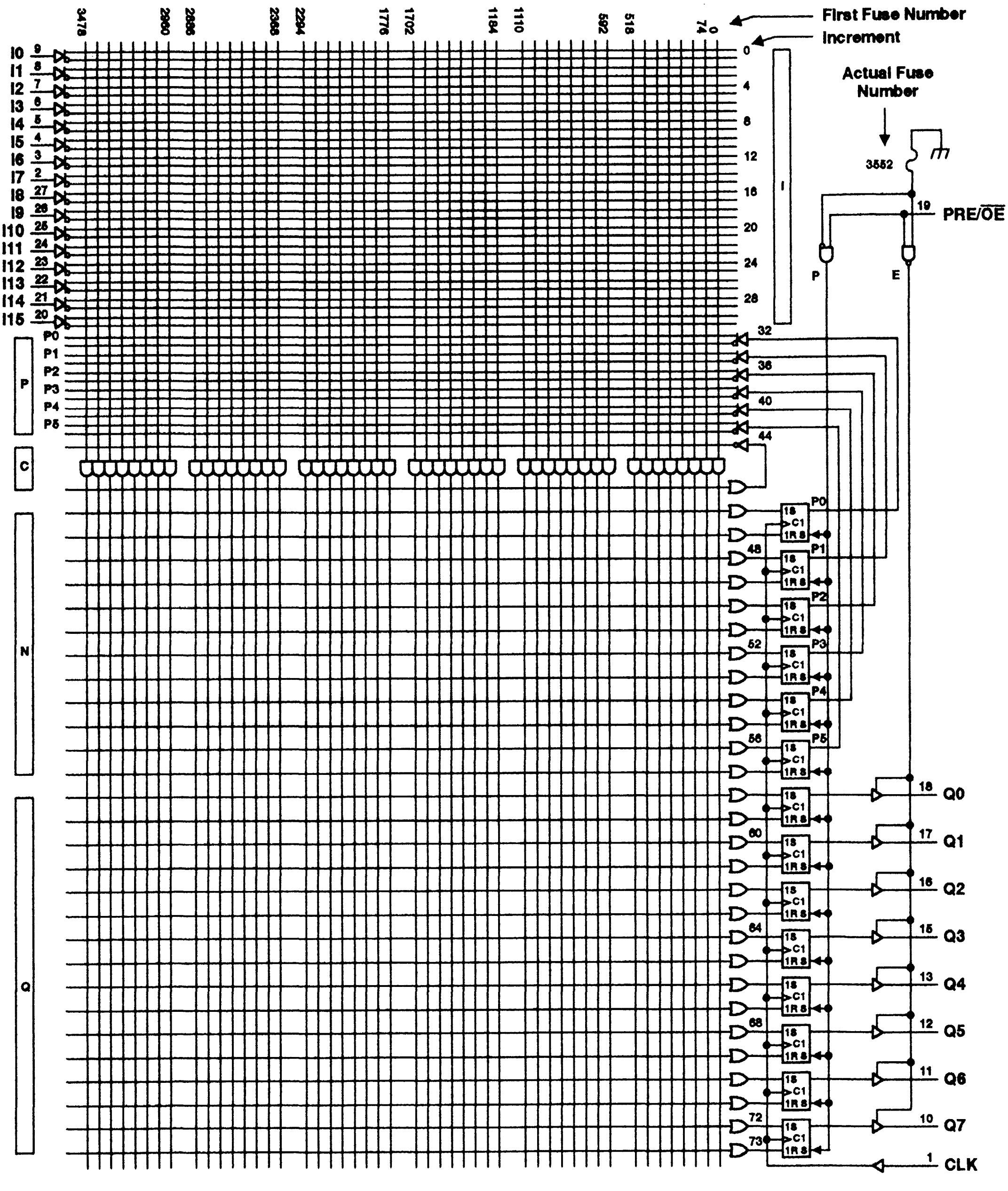
functional block diagram (positive logic)



timing diagram



logic diagram (positive logic)



NOTES: 1. All AND gate inputs with a blown link float to the high level.
2. All OR gate inputs with a blown link float to the low level.
3. Fuse numbers = First fuse number + Increment

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 4)	7 V
Input voltage (see Note 4)	5.5 V
Voltage applied to disabled output (see Note 4)	5.5 V
Operating free-air temperature range	0°C to 75°C
Storage temperature range	–65°C to 150°C

NOTE 4: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				–3.2	mA
I_{OL}	Low-level output current				24	mA
f_{clock}	Clock frequency†	1 thru 48 product terms without C-array ‡	0		50	MHz
		1 thru 48 product terms with C-array	0		30	
t_w	Pluse duration	Clock high or low	10			ns
		Preset	15			
t_{su}	Setup time before CLK↑, 1 thru 48 product terms	Without C-array	15			ns
		With C-array	30			
t_{su}	Setup time, Preset low (inactive) before CLK↑§		8			ns
t_h	Hold time, input after CLK↑		0			ns
T_A	Operating free-air temperature		0	25	75	°C

† The maximum clock frequency is independent of the internal programmed configuration. If an output is fed back externally to an input, the maximum clock frequency must be calculated.
‡ The C-array is the single sum term that is complemented and fed back to the AND array.
§ After Preset goes inactive, normal clocking resumes on the first low-to-high clock transition.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	$V_{CC} = 4.75$ V,	$I_I = -18$ mA			−1.2	V
V_{OH}	$V_{CC} = 4.75$ V,	$I_{OH} = -3.2$ mA	2.4	3		V
V_{OL}	$V_{CC} = 4.75$ V,	$I_{OL} = 24$ mA		0.37	0.5	V
I_{OZH}	$V_{CC} = 5.25$ V,	$V_O = 2.7$ V			20	µA
I_{OZL}	$V_{CC} = 5.25$ V,	$V_O = 0.4$ V			−20	µA
I_I	$V_{CC} = 5.25$ V,	$V_I = 5.5$ V			25	µA
I_{IH}	$V_{CC} = 5.25$ V,	$V_I = 2.7$ V			20	µA
I_{IL}	$V_{CC} = 5.25$ V,	$V_I = 0.4$ V			−0.25	mA
I_O‡	$V_{CC} = 5.25$ V,	$V_O = 2.25$ V	−30		−112	mA
I_{CC}	$V_{CC} = 5.25$ V, PRE/$\overline{OE}$ at GND,	$V_I = 4.7$ V, Outputs open		120	180	mA

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	TYP†	MAX	UNIT
f_{max}§	Without C array		R1 = 500 Ω, R2 = 500 Ω, See Figure 5	50	70		MHz
	With C array			30	45		
t_{pd}	CLK↑	Q			8	15	ns
t_{pd}	PRE↑	Q			12	20	ns
t_{pd}	V_{CC}↑	Q			0	10	ns
t_{en}	$\overline{OE}$↓	Q			10	20	ns
t_{dis}	$\overline{OE}$↑	Q			5	10	ns

† All typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

‡ The output conditions hace been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

§ f_{max} is independent of the internal programmed configuration and the number of product terms used.

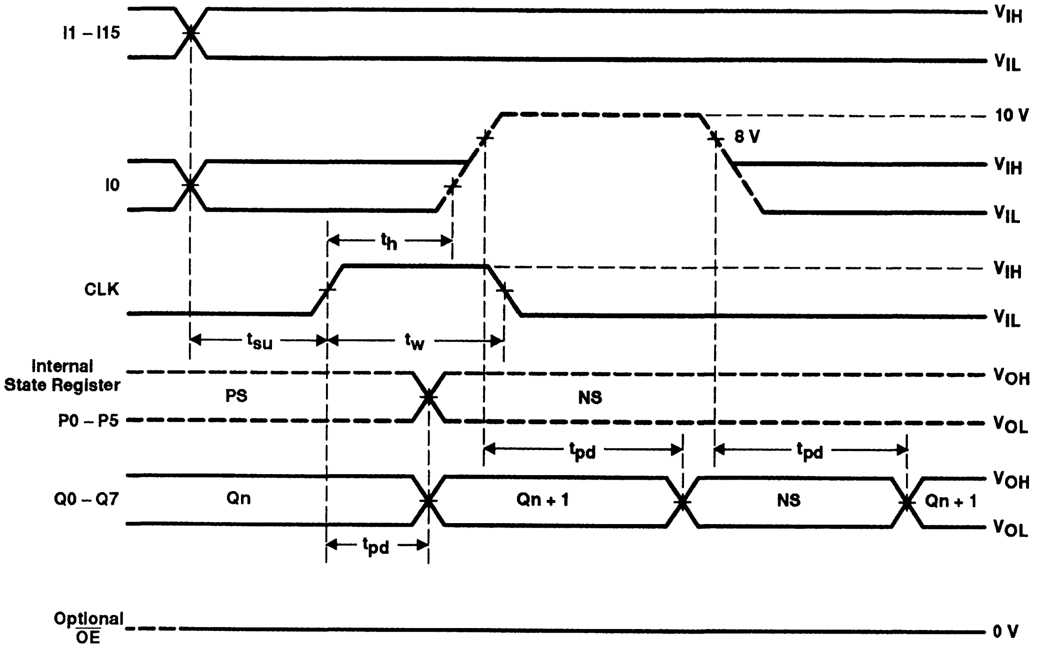
programming information

Texas Instruments Programmable Logic Devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments Programmable Logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

diagnostics

A diagnostics mode is provided with these devices that allows the user to inspect the contents of the state register. When I0 (pin 9) is held at 10 V, the state register bits P0–P5 will appear at the Q0–Q5 outputs and Q6–Q7 will be high. The contents of the output register will remain unchanged.



PS = Present state, NS = Next state

Figure 1. Diagnostic Waveforms

test array

A test array that consists of product lines 48 and 49 has been added to these devices to allow testing prior to programming. The test array is factory programmed as shown in Table 1. Testing is accomplished by connecting Q0–Q7 to I8–I15, PRE/$\overline{OE}$ to GND, and applying the proper input signals as shown in Figure 2. Product lines 48 and 49 must be deleted during user programming to avoid interference with the programmed logic function.

Table 1. Test Array Program

																								OPTION PRE/$\overline{OE}$													H
	AND																								OR													
PRODUCT LINE	C	$\overline{C}$	INPUT (In)																PRESENT STATE (PS)						NEXT STATE (NS)						OUT (Qn)							
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	5	4	3	2	1	0	5	4	3	2	1	0	7	6	5	4	3	2	1	0
48	X	–	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L
49	–	X	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H

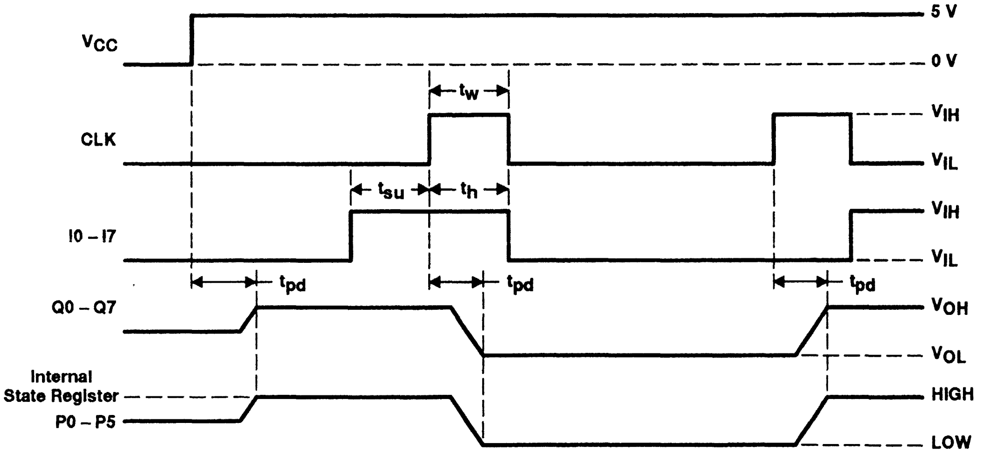


Figure 2. Test Array Waveforms

Table 2. Test Array Deleted

																								OPTION PRE/$\overline{OE}$													H
	AND																								OR													
PRODUCT LINE	C	$\overline{C}$	INPUT (In)																PRESENT STATE (PS)						NEXT STATE (NS)						OUT (Qn)							
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	5	4	3	2	1	0	5	4	3	2	1	0	7	6	5	4	3	2	1	0
48	–	–	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	–	–	–	–	–	–	–	–	–	–	–	–	–	–
49	–	X	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	–	–	–	–	–	–	–	–	–	–	–	–	–	–

X = Fuse intact, – = Fuse blown

TIB82S105B, 82S105A COMPARISON

The Texas Instruments TIB82S105B is a 16 × 48 × 8 Field-Programmable Logic Sequencer that is functionally equivalent to the Signetics 82S105A. However, the TIB82S105B is designed for a maximum speed of 50 MHz with the preset function being made conventional. As a result the TIB82S105B differs from the 82S105A in speed and in the preset recovery function.

The TIB82S105B is a high-speed version of the original 82S105A. The TIB82S105B features increased switching speeds with no increase in power. The maximum operating frequency is increased from 20 MHz to 50 MHz and does not decrease as more product terms are connected to each sum (OR) line. For instance, if all 48 product tems were connected to a sum line on the original 82S105A, the f_{max} would be about 15 MHz. The f_{max} for the TIB82S105B remains at 50 MHz regardless of the programmed configuration. In addition, the preset recovery sequence was changed to a conventional recovery sequence, providing quicker clock recovery times. This is explained in the following paragraph.

The TIB82S105B and the 82S105A are equipped with power-up preset and asynchronous preset functions. The power-up preset causes the registers to go high during power up. The asynchronous preset inhibits clocking and causes the registers to go high whenever the preset pin is taken high. After a power-up preset occurs, the minimum setup time from power up to the first clock pulse must be met in order to assure that clocking is not inhibited. In a similar manner after an asynchronous preset, the preset input must return low (inactive) for a given time, t_{su}, before clocking.

The Signetics 82S105A was designed in such a way that after both power-up preset and asynchronous preset it requires that a high-to-low clock transition occur before a clocking transition (low-to-high) will be recognized. This is shown in Figure 3. The Texas Instruments TIB82S105B does not require a high-to-low clock transition before clocking can be resumed, it only requires that the preset be inactive 8 ns (preset inactive-state setup time) before the clock rising edge. See Figure 4.

The TIB82S105B, with an f_{max} of 50 MHz, is ideal for systems in which the state machine must run several times faster than the system clock. It is recommended that the TIB82S105B be used in new designs. ***However, if the TIB82S105B is used to replace the 82S105A, then the customer must understand that clocking will begin with the first clock rising edge after preset.***

Table 3. Speed Differences

PARAMETER	82S105A SIGNETICS	TIB82S105B TI ONLY
f_{max}	20 MHz	50 MHz
t_{pd}, CLK to Q	20 ns	15 ns

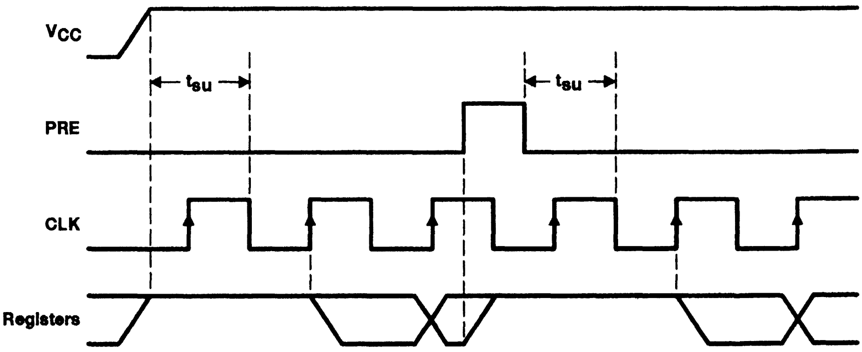


Figure 3. 82S105A Preset Recovery Operation

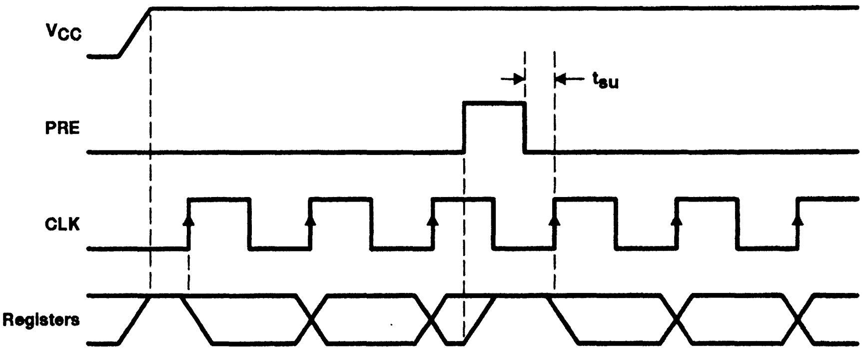
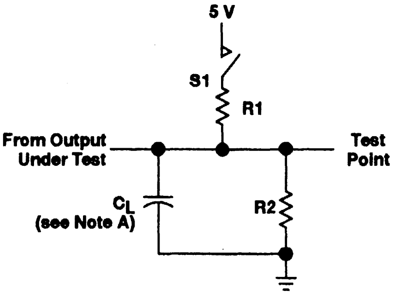
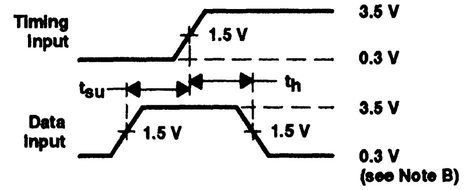


Figure 4. TIB82S105B Preset Recovery Operation

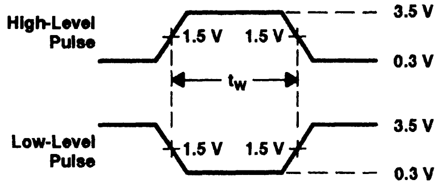
PARAMETER MEASUREMENT INFORMATION



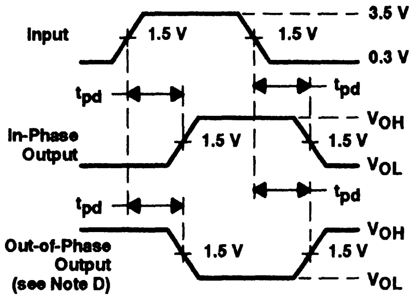
LOAD CIRCUIT FOR
3-STATE OUTPUTS



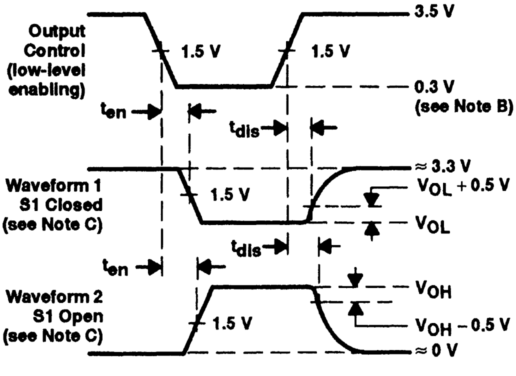
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
B. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.
E. Equivalent loads may be used for testing.

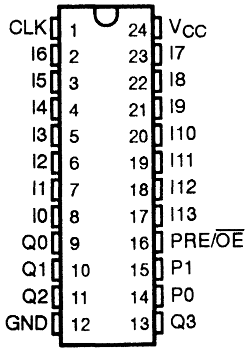
Figure 5. Load Circuit and Voltage Waveforms

TIB82S167BC
14 × 48 × 6 FIELD-PROGRAMMABLE LOGIC SEQUENCER WITH 3-STATE OUTPUTS OR PRESET

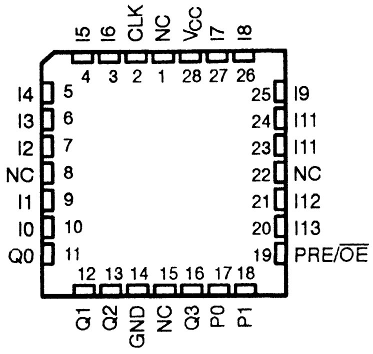
SRPS026 – D2896, JANUARY 1985 – REVISED MARCH 1992

- **Programmable Asynchronous Preset or Output Control**
- **Power-On Preset of All Flip-Flops**
- **8-Bit Internal State Register With 4-Bit Output Register**
- **Power Dissipation . . . 600 mW Typical**
- **Functionally Equivalent to, but Faster Than 82S105A†**

NT PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



NC – No internal connection

description

The TIB82S167BC is a TTL field-programmable state machine of the Mealy type. This state machine (logic sequencer) contains 48 product terms (AND terms) and 12 pairs of sum terms (OR terms). The product and sum terms are used to control the 8-bit internal state register and the 4-bit output register.

The outputs of the internal state register (P0–P7) are fed back and combined with the 14 inputs (I0–I13) to form the AND array. In addition the first two bits of the internal state register (P0–P1) are brought off-chip to allow the output register to be extended to 6 bits if desired. A single sum term is complemented and fed back to the AND array, which allows any of the product terms to be summed, complemented, and used as inputs to the AND array.

The state and output registers are positive-edge-triggered S/R flip-flops. These registers are unconditionally preset high during power up. PRE/$\overline{\text{OE}}$ can be used as PRE to preset both registers or, by blowing the proper fuse, be converted to an output control function, $\overline{\text{OE}}$.

The TIB82S167BC is characterized for operation from 0°C to 75°C.

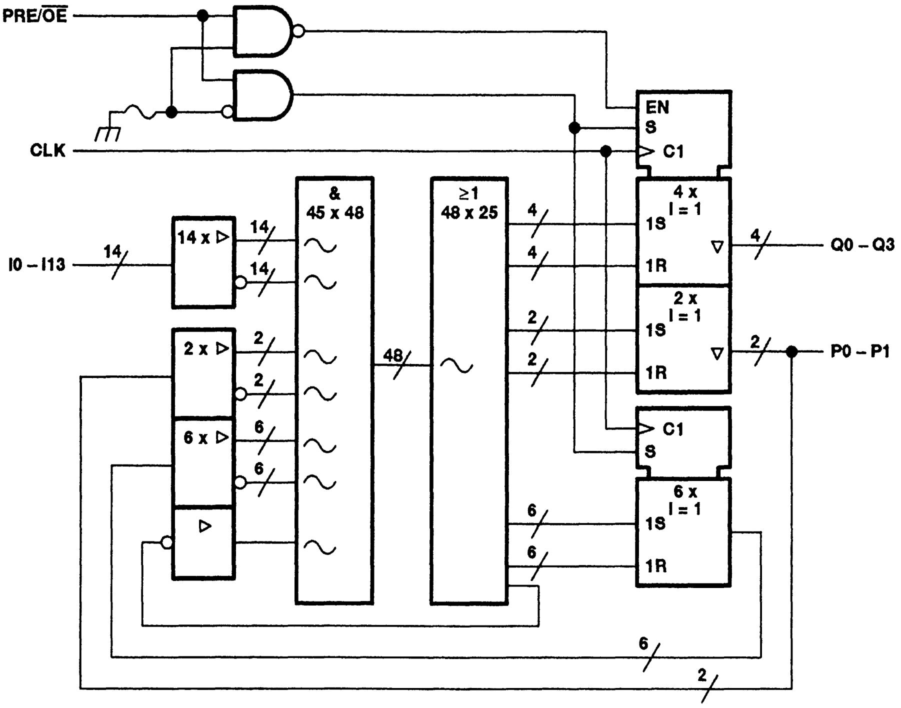
---

† Power-up preset and asynchronous preset functions are not identical to 82S167A.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

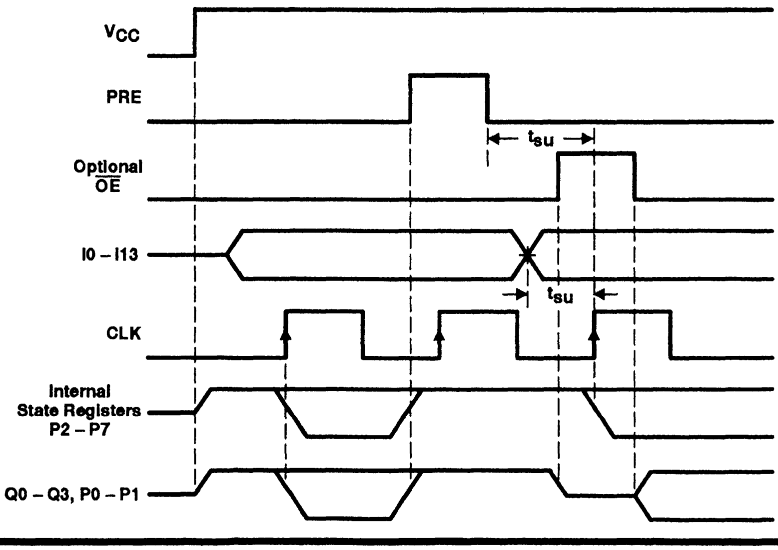
Copyright © 1992, Texas Instruments Incorporated

functional block diagram (positive logic)

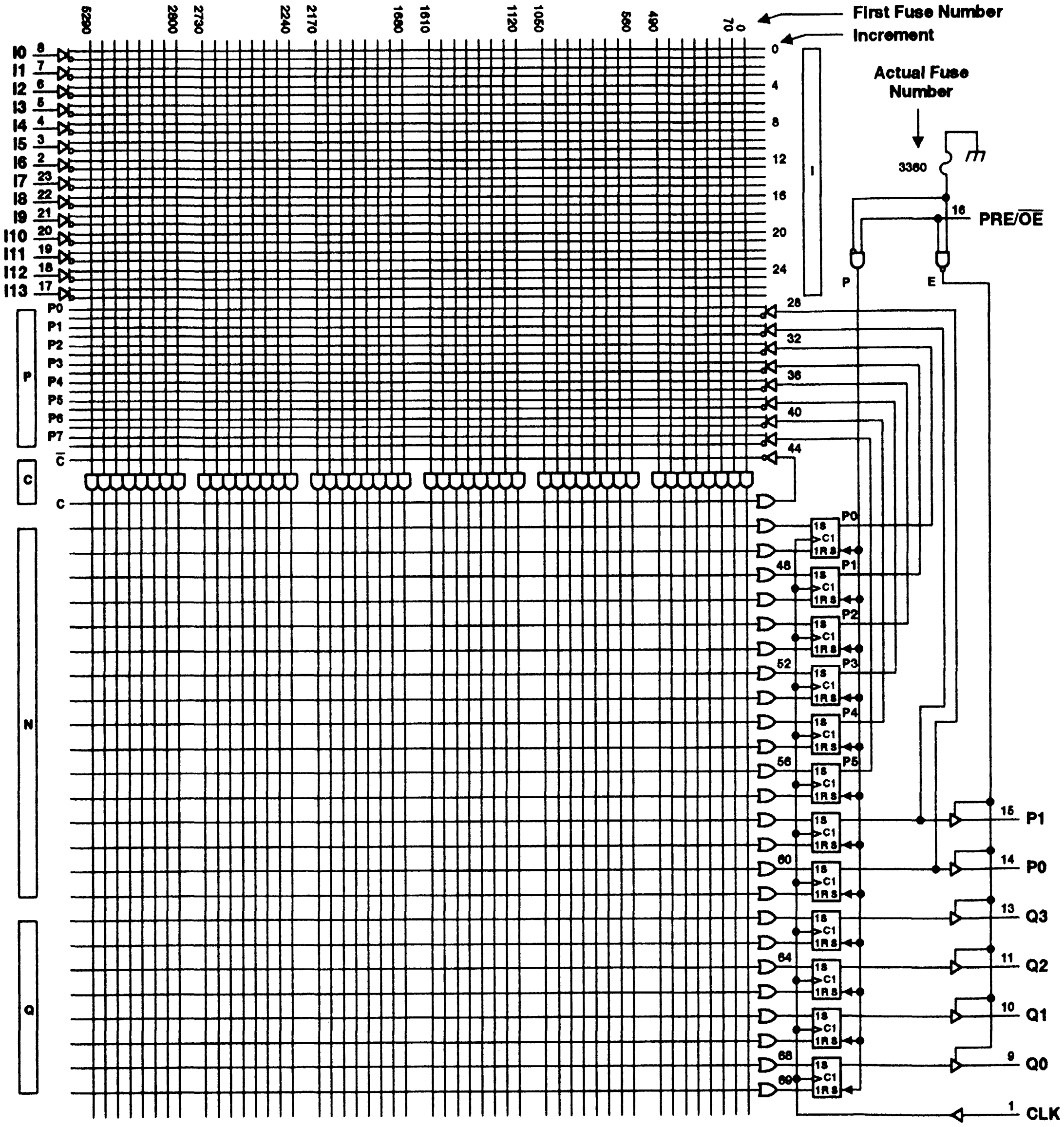


∿ denotes fused inputs

timing diagram



logic diagram (positive logic)



NOTES: 1. All AND gate inputs with a blown link float to the high level.
2. All OR gate inputs with a blown link float to the low level.
3. Fuse numbers = First fuse number + Increment

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 4) .... 7 V
Input voltage (see Note 4) .... 5.5 V
Voltage applied to disabled output (see Note 4) .... 5.5 V
Operating free-air temperature range .... 0°C to 75°C
Storage temperature range .... –65°C to 150°C

NOTE 4: These ratings apply except for programming pins during a programming cycle.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage		2		5.5	V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				–3.2	mA
I_{OL}	Low-level output current				24	mA
f_{clock}	Clock frequency†	1 thru 48 product terms without C-array ‡	0		50	MHz
		1 thru 48 product terms with C-array	0		30	
t_w	Pluse duration	Clock high or low	10			ns
		Preset	15			
t_{su}	Setup time before CLK↑, 1 thru 48 product terms	Without C-array	15			ns
		With C-array	30			
t_{su}	Setup time, Preset low (inactive) before CLK↑§		8			ns
t_h	Hold time, input after CLK↑		0			ns
T_A	Operating free-air temperature		0	25	75	°C

† The maximum clock frequency is independent of the internal programmed configuration. If an output is fed back externally to an input, the maximum clock frequency must be calculated.
‡ The C-array is the single sum term that is complemented and fed back to the AND array.
§ After Preset goes inactive, normal clocking resumes on the first low-to-high clock transition.

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}	$V_{CC} = 4.75$ V,	$I_I = -18$ mA			−1.2	V
V_{OH}	$V_{CC} = 4.75$ V,	$I_{OH} = -3.2$ mA	2.4	3		V
V_{OL}	$V_{CC} = 4.75$ V,	$I_{OL} = 24$ mA		0.37	0.5	V
I_{OZH}	$V_{CC} = 5.25$ V,	$V_O = 2.7$ V			20	µA
I_{OZL}	$V_{CC} = 5.25$ V,	$V_O = 0.4$ V			−20	µA
I_I	$V_{CC} = 5.25$ V,	$V_I = 5.5$ V			25	µA
I_{IH}	$V_{CC} = 5.25$ V,	$V_I = 2.7$ V			20	µA
I_{IL}	$V_{CC} = 5.25$ V,	$V_I = 0.4$ V			−0.25	mA
I_O‡	$V_{CC} = 5.25$ V,	$V_O = 2.25$ V	−30		−112	mA
I_{CC}	$V_{CC} = 5.25$ V, PRE/$\overline{OE}$ at GND,	$V_I = 4.5$ V, Outputs open		90	160	mA

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	TYP†	MAX	UNIT
f_{max}§	Without C array			50	70		MHz
	With C array			30	45		
t_{pd}	CLK↑	Q	R1 = 500 Ω,		10	15	ns
t_{pd}	PRE↑	Q	R2 = 500 Ω,		8	20	ns
t_{pd}	V_{CC}↑	Q	See Figure 5		0	10	ns
t_{en}	$\overline{OE}$↓	Q			10	20	ns
t_{dis}	$\overline{OE}$↑	Q			5	10	ns

† All typical values are at $V_{CC} = 5$ V, $T_A = 25°C$.

‡ The output conditions hace been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

§ f_{max} is independent of the internal programmed configuration and the number of product terms used.

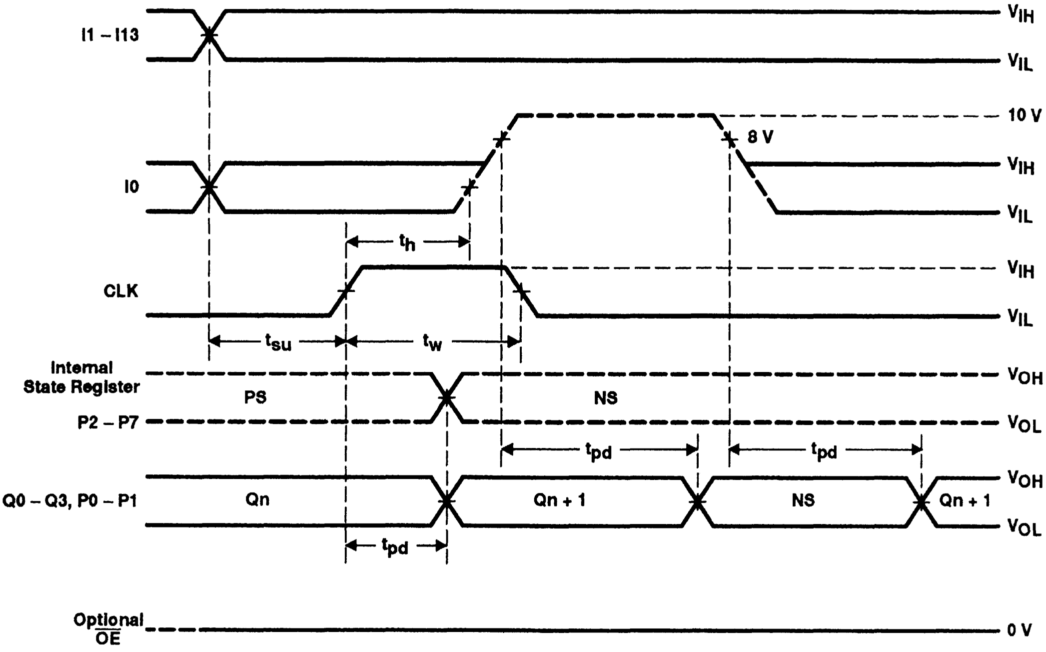
programming information

Texas Instruments Programmable Logic Devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments Programmable Logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

diagnostics

A diagnostics mode is provided with these devices that allows the user to inspect the contents of the state register. When I0 is held at 10 V, the state register bits P2–P7 will appear at the Q0–Q3 and P0–P1 outputs. The contents of the output registers, Q0–Q3, P0–P1 remain unchanged.



PS = Present State, NS = Next State

Figure 1. Diagnostic Waveforms

test array

A test array that consists of product lines 48 and 49 has been added to these devices to allow testing prior to programming. The test array is factory programmed as shown in Table 1. Testing is accomplished by connecting Q0–Q3 to I10–I13, PRE/$\overline{OE}$ to GND, and applying the proper input signals as shown in Figure 2. Product lines 48 and 49 must be deleted during user programming to avoid interference with the programmed logic function.

Table 1. Test Array Program

																									OPTION PRE/$\overline{OE}$													H
PRODUCT LINE	AND																								OR													
	C	$\overline{C}$	INPUT (In)																PRESENT STATE (PS)						NEXT STATE (NS)						OUT (Qn)							
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	5	4	3	2	1	0	5	4	3	2	1	0	7	6	5	4	3	2	1	0
48	X	-	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	L	L	L	L	L	L	L	L	L	L	L	L	L	L
49	-	X	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	H	H	H	H	H	H	H	H	H	H	H	H	H	H

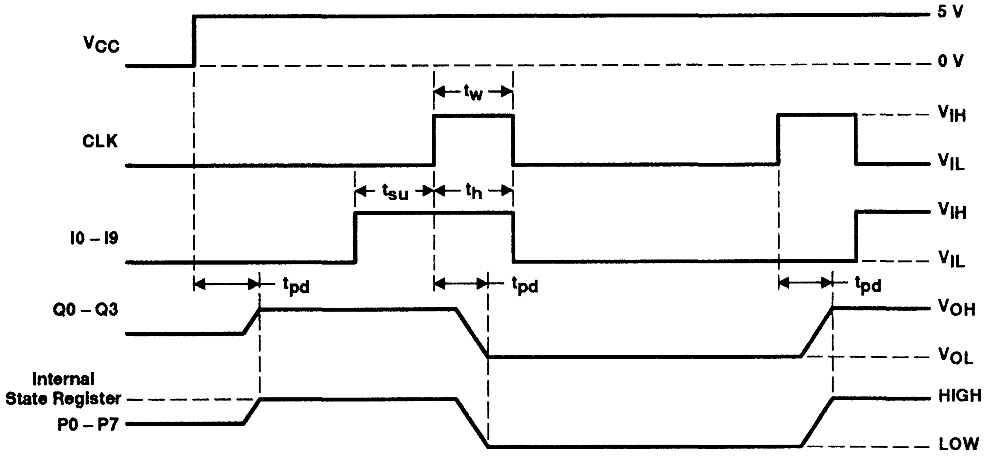


Figure 2. Test Array Waveforms

Table 2. Test Array Deleted

																									OPTION PRE/OE													H
PRODUCT LINE	AND																								OR													
	C	$\overline{C}$	INPUT (In)																PRESENT STATE (PS)						NEXT STATE (NS)						OUT (Qn)							
			15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	5	4	3	2	1	0	5	4	3	2	1	0	7	6	5	4	3	2	1	0
48	-	-	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	H	-	-	-	-	-	-	-	-	-	-	-	-	-	-
49	-	X	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	L	-	-	-	-	-	-	-	-	-	-	-	-	-	-

X = Fuse intact, – = Fuse blown

TIB82S167B, 82S167A COMPARISON

The Texas Instruments TIB82S167B is a 14 × 48 × 6 Field-Programmable Logic Sequencer that is functionally equivalent to the Signetics 82S167A. However, the TIB82S167B is designed for a maximum speed of 50 MHz with the preset function being made conventional. As a result the TIB82S167B differs from the 82S167A in speed and in the preset recovery function.

The TIB82S167B is a high-speed version of the original 82S167A. The TIB82S167B features increased switching speeds with no increase in power. The maximum operating frequency is increased from 20 MHz to 50 MHz and does not decrease as more product terms are connected to each sum (OR) line. For instance, if all 48 product tems were connected to a sum line on the original 82S167A, the f_{max} would be about 15 MHz. The f_{max} for the TIB82S167B remains at 50 MHz regardless of the programmed configuration. In addition, the preset recovery sequence was changed to a conventional recovery sequence, providing quicker clock recovery times. This is explained in the following paragraph.

The TIB82S167B and the 82S167A are equipped with power-up preset and asynchronous preset functions. The power-up preset causes the registers to go high during power up. The asynchronous preset inhibits clocking and causes the registers to go high whenever the preset pin is taken high. After a power-up preset occurs, the minimum setup time from power up to the first clock pulse must be met in order to assure that clocking is not inhibited. In a similar manner after an asynchronous preset, the preset input must return low (inactive) for a given time, t_{su}, before clocking.

The Signetics 82S167A was designed in such a way that after both power-up preset and asynchronous preset it requires that a high-to-low clock transition occur before a clocking transition (low-to-high) will be recognized. This is shown in Figure 3. The Texas Instruments TIB82S167B does not require a high-to-low clock transition before clocking can be resumed, it only requires that the preset be inactive 8 ns (preset inactive-state setup time) before the clock rising edge. See Figure 4.

The TIB82S167B, with an f_{max} of 50 MHz, is ideal for systems in which the state machine must run several times faster than the system clock. It is recommended that the TIB82S167B be used in new designs. ***However, if the TIB82S167B is used to replace the 82S167A, then the customer must understand that clocking will begin with the first clock rising edge after preset.***

Table 3. Speed Differences

PARAMETER	82S167A SIGNETICS	TIB82S167B TI ONLY
f_{max}	20 MHz	50 MHz
t_{pd}, CLK to Q	20 ns	15 ns

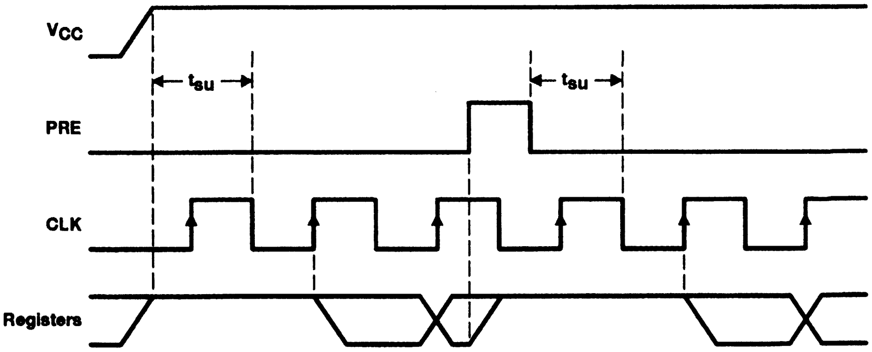


Figure 3. 82S167A Preset Recovery Operation

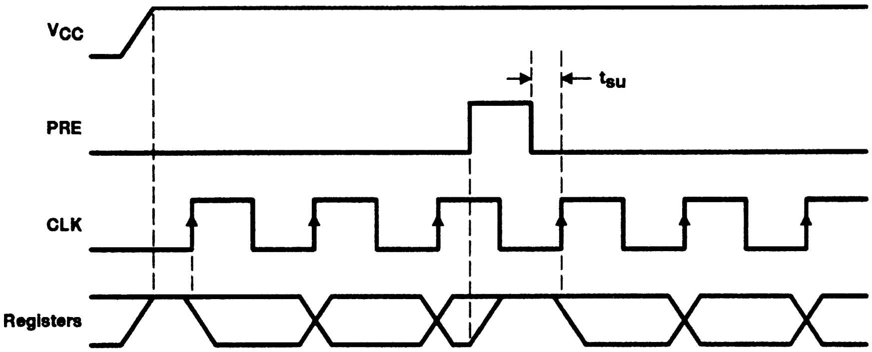
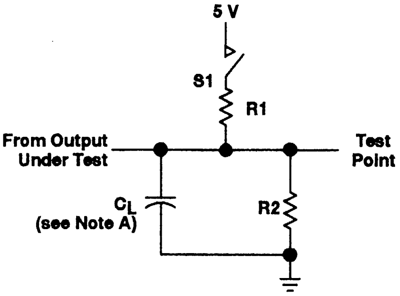
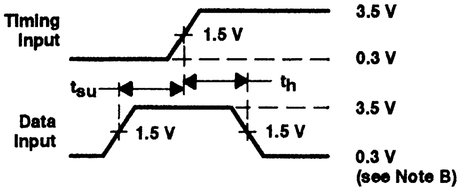


Figure 4. TIB82S167B Preset Recovery Operation

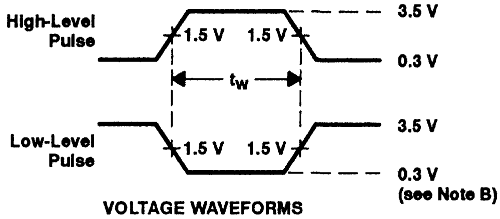
PARAMETER MEASUREMENT INFORMATION



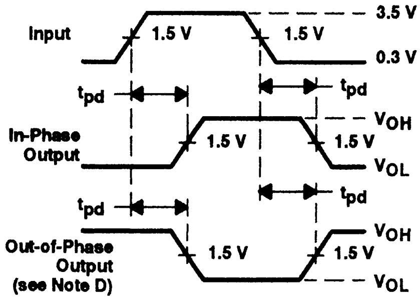
LOAD CIRCUIT FOR
3-STATE OUTPUTS



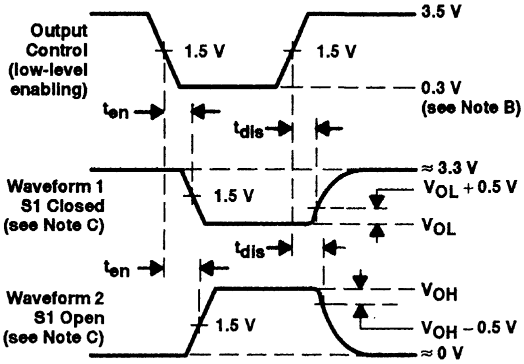
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES:
- A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
- B. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f = 2$ ns, duty cycle = 50%.
- C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.
- E. Equivalent loads may be used for testing.

Figure 5. Load Circuit and Voltage Waveforms

TICPAL16L8-55C, TICPAL16R4-55C, TICPAL16R6-55C, TICPAL16R8-55C
STANDARD CMOS *PAL*® CIRCUITS

SRPS027 – D3062, NOVEMBER 1987 – REVISED MARCH 1992

- **Standard 20-Pin PLD Family**
- **Virtually Zero Standby Power**
- **Propagation Delay Time . . . 55 ns Max**
- **TTL- and HC-Compatible Inputs and Outputs**
- **Preload Capability to Aid Testing**
- **Fully Tested for High Programming Yield Before Packaging**
- **Greater Than 2000-V Input Protection for Electrostatic Discharge**
- **Devices in the 'JL' Package Can Be Erased and Reprogrammed More Than Once**

DEVICE	I INPUTS	3-STATE O OUTPUTS	REGISTERED Q OUTPUTS	I/O PORTS
PAL16L8	10	2	0	6
PAL16R4	8	0	4 (3-state buffers)	4
PAL16R6	8	0	6 (3-state buffers)	2
PAL16R8	8	0	8 (3-state buffers)	0

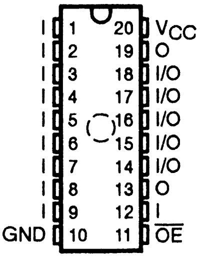
description

These programmable array logic devices provide reliable, high-performance substitutes for conventional TTL and HCT logic. They are also compatible with HC logic over the V_{CC} range of 4.75 V to 5.25 V. Their easy programmability allows for quick design of custom functions and typically results in a more compact circuit board. Static power dissipation for these devices is negligible.

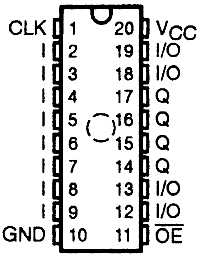
The output registers of these devices are D-type flip-flops that store data on the low-to-high transition of the clock input. The registered outputs may be disabled by taking $\overline{OE}$ high, whereas the nonregistered outputs may be disabled through the use of individual product terms. Unused inputs must always be connected to an appropriate logic level, preferably either V_{CC} or ground.

The programming cell consists of a floating-gate device like those used in EPROMs. All terms are initially connected. The unwanted terms are programmed out to provide the desired function. The output of a given AND gate is low if both the

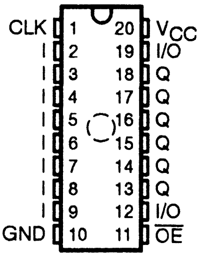
TICPAL16L8'
JL OR N PACKAGE
(TOP VIEW)



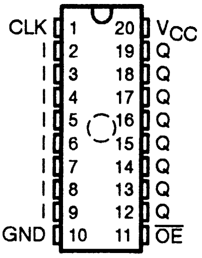
TICPAL16R4'
JL OR N PACKAGE
(TOP VIEW)



TICPAL16R6'
JL OR N PACKAGE
(TOP VIEW)



TICPAL16R8'
JL OR N PACKAGE
(TOP VIEW)



These devices are covered by U.S. Patent 4,410,987
PAL is a registered trademark of Advanced Micro Devices Inc.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 1992, Texas Instruments Incorporated

description (continued)

true and complement cells of a term are connected, and high if all related cells are programmed. Programming can be done manually but is usually achieved through the use of commercially available programming equipment.

This TICPAL16' series has internal electrostatic discharge (EDS) protection circuits and has been classified with a 2000-V EDS rating tested under MIL-STD-883B, Method 3015.1. However, care should be exercised in handling these devices, as exposure to EDS may result in a degradation of the device parametric performance.

The floating-gate programming cells allow these PLD to be fully programmed and tested before assembly to assure high field programming yield and functionality. They are then erased by ultraviolet light before packaging.

All devices in this series contain a security feature. Once the security cell is programmed, additional programming and verification cannot be performed. This prevents easy duplication of a design.

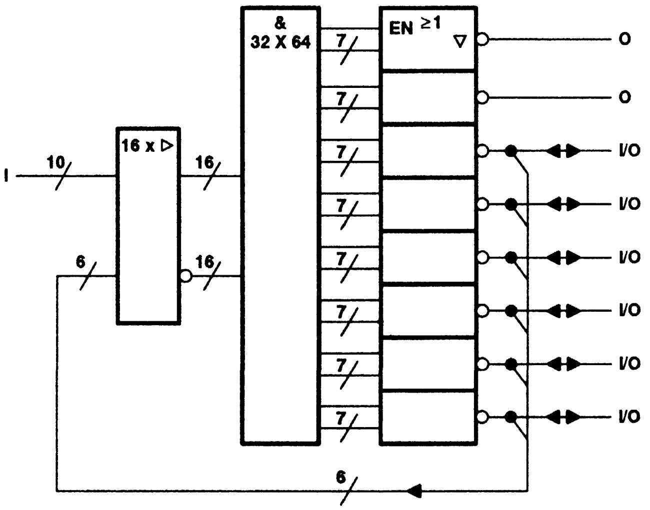
The TICPAL16' C series is characterized for operation from 0°C to 75°C.

erasure

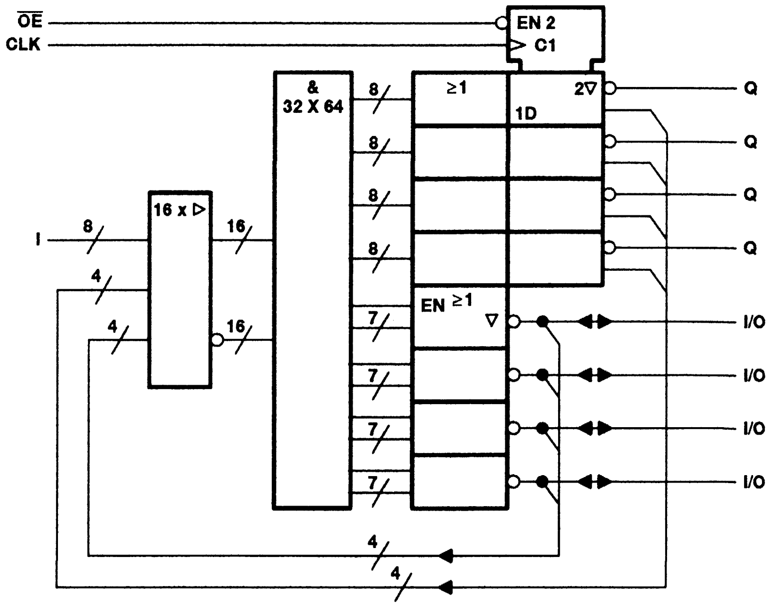
The TICPAL16' (JL package) series can be erased after programming by exposure to ultraviolet light that has a wavelength of 253.7 nm (2537 Å). The recommended minimum exposure dose (UV intensity x exposure time) is fifteen w•s•cm^{-2}. The lamp should be located about 2.5 cm (1 inch) above the chip during erasure. It should be noted that normal ambient light contains the correct wavelength for erasure. Therefore, when using the TICPAL16' series (JL package), the window should be covered with an opaque label.

functional block diagrams (positive logic)

TICPAL16L8'

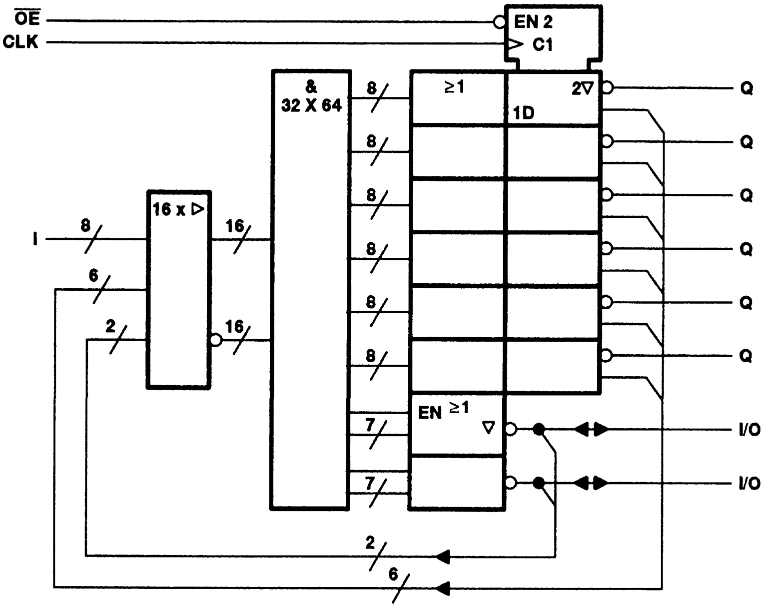


TICPAL16R4'

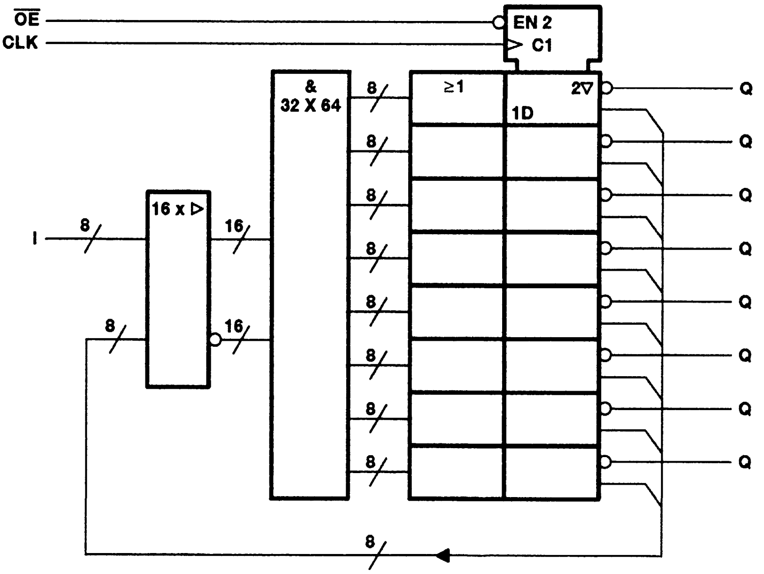


functional block diagrams (positive logic)

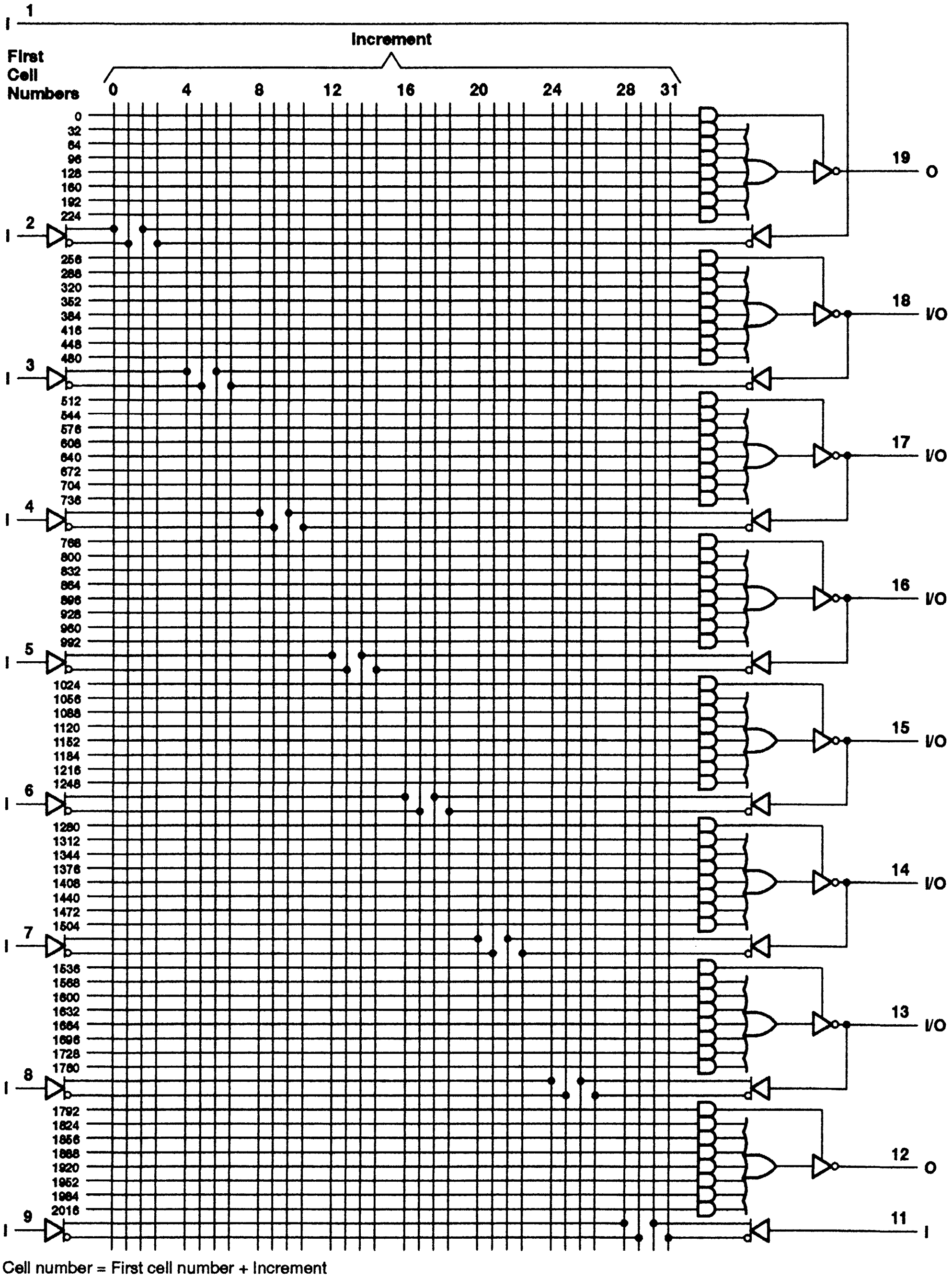
TICPAL16R6'



TICPAL16R8'

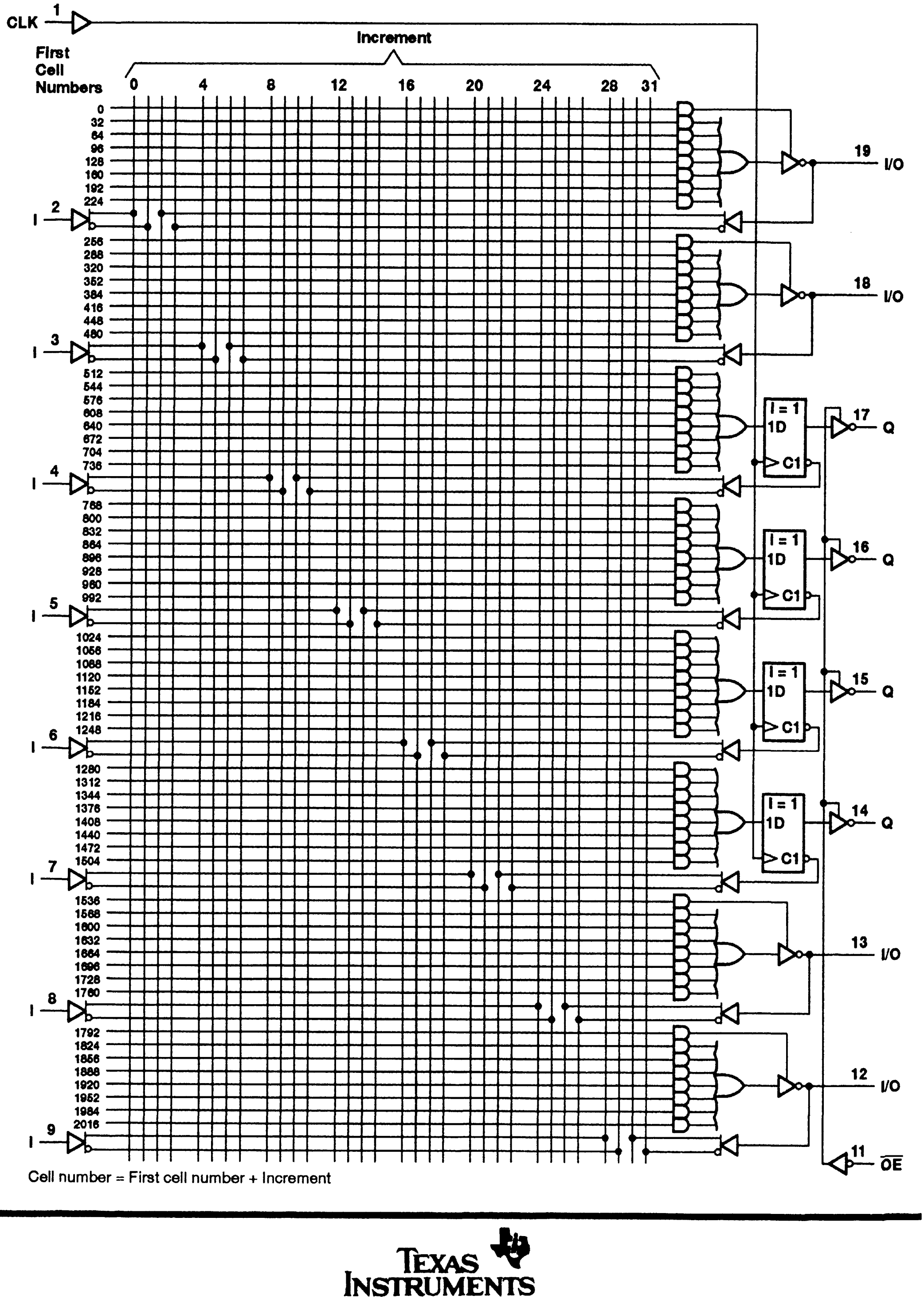


logic diagram (positive logic)



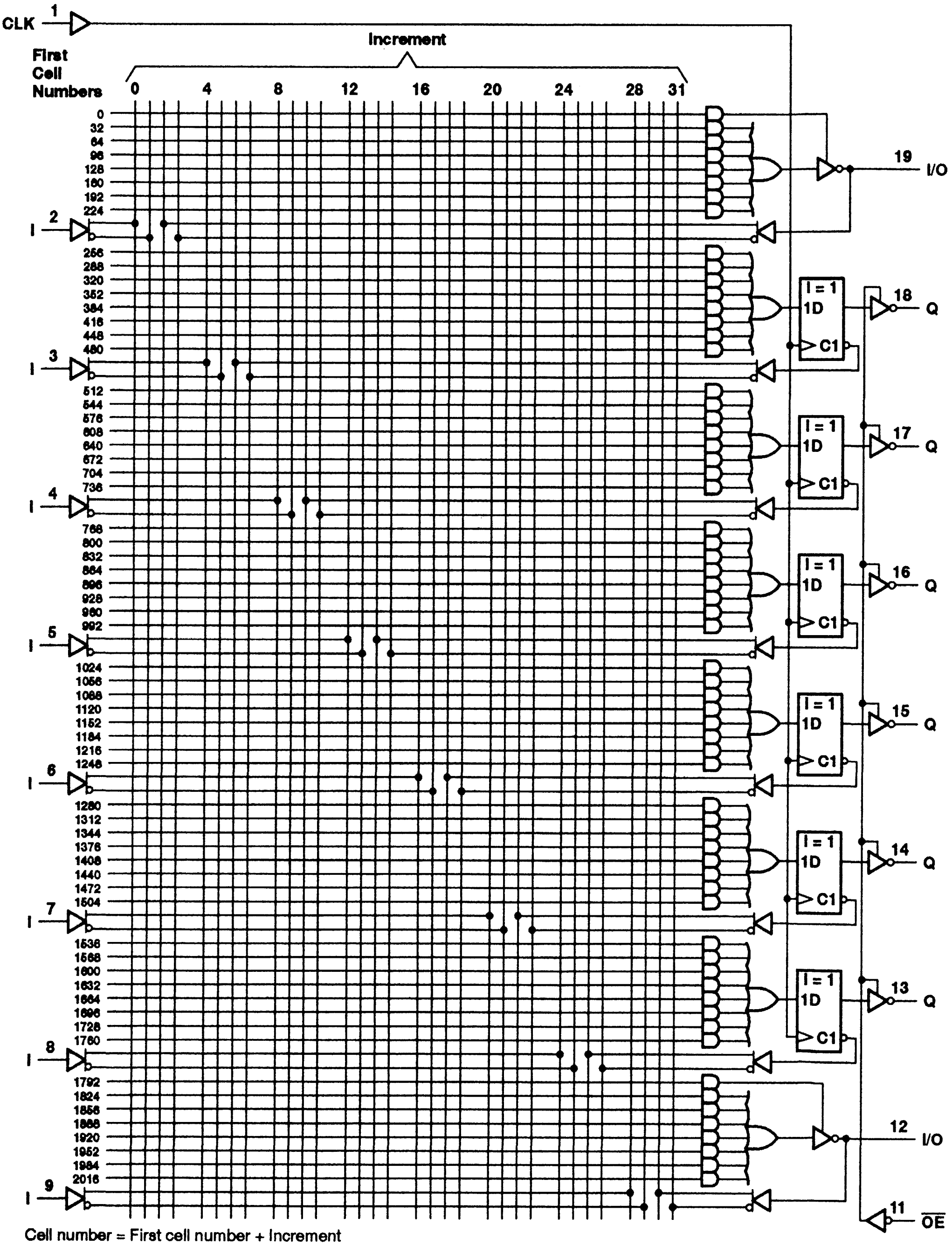
Cell number = First cell number + Increment

logic diagram (positive logic)



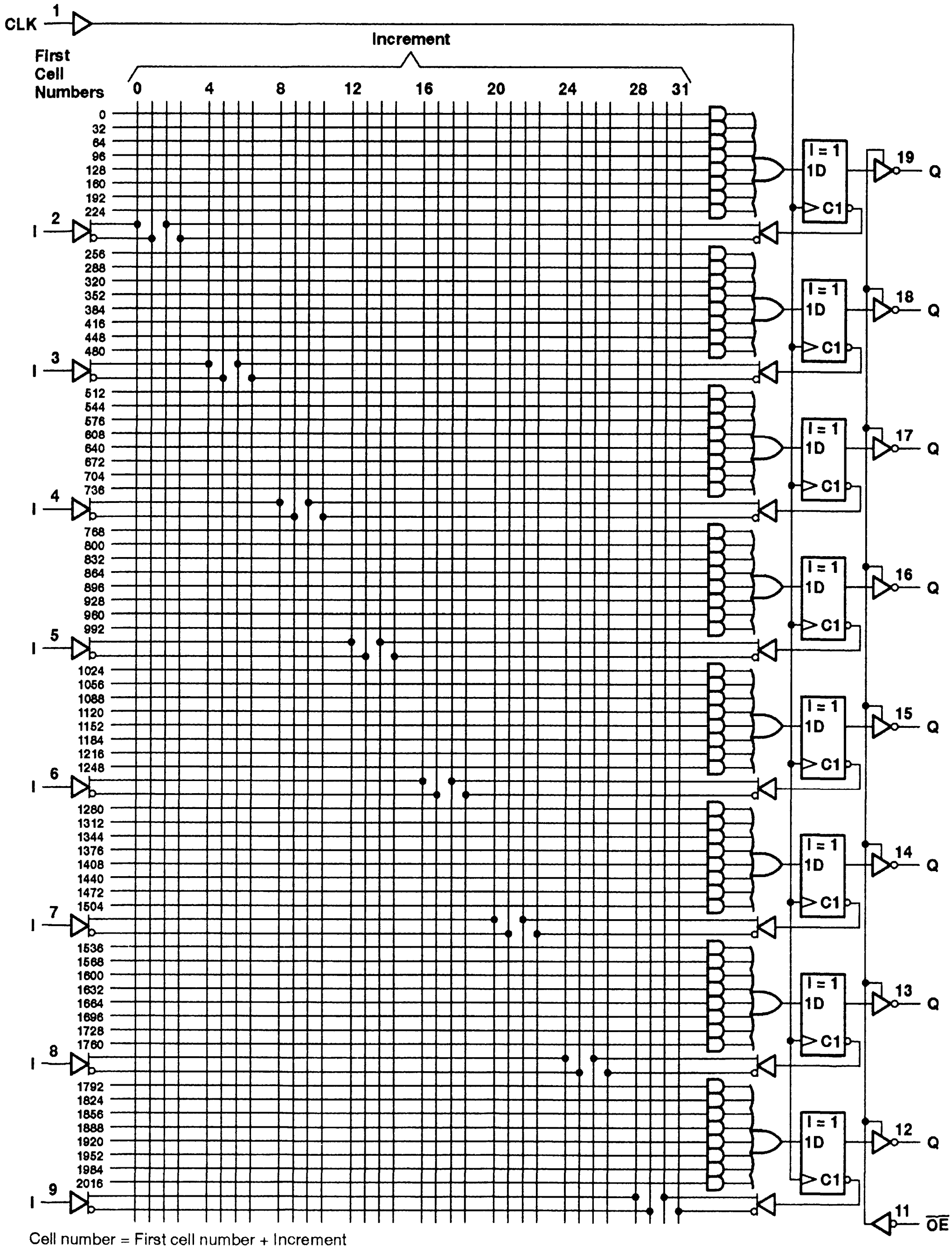
Cell number = First cell number + Increment

logic diagram (positive logic)



Cell number = First cell number + Increment

logic diagram (positive logic)



Cell number = First cell number + Increment

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to V_{CC}+0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	± 20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	± 20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	± 35 mA
Continuous current through V_{CC} pin	70 mA
Continuous current through GND pin	–200 mA
Lead temperature 1,6 mm (1/16 in) from case for 60 seconds (JL package)	300°C
Lead temperature 1,6 mm (1/16 in) from case for 10 seconds (N package)	260°C
Operating free-air temperature range	0°C to 75°C
Storage temperature range	–65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: These ratings apply except for programming pins during a programming cycle or during a preload cycle.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
t_w	Pulse duration	Clock high	20			ns
		Clock low	20			
t_{su}	Setup time, input or feedback before clock↑		40			ns
t_h	Hold time, input or feedback after clock↑		0			ns
T_A	Operating free-air temperature		0	25	75	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS			MIN	TYP†	MAX	UNIT
V_{OH}	V_{CC} = 4.75 V,	I_{OH} = −3.2 mA (for TTL)		4			V
	V_{CC} = 4.75 V,	I_{OH} = −4 mA (for CMOS)		3.86			
V_{OL}	V_{CC} = 4.75 V,	I_{OL} = 24 mA (for TTL)				0.5	V
	V_{CC} = 4.75 V,	I_{OL} = 4 mA (for CMOS)				0.4	
I_{OZH}	V_{CC} = 5.25 V,	V_O = 2.4 V				10	µA
I_{OZL}	V_{CC} = 5.25 V,	V_O = 0.4 V				−10	µA
I_{IH}	V_{CC} = 5.25 V,	V_I = V_{CC}				10	µA
I_{IL}	V_{CC} = 5.25 V,	V_I = 0				−10	µA
I_{CC} (standby)	V_{CC} = 5.25 V,	V_I = 0 or V_{CC},	I_O = 0			100	µA
$\frac{I_{CC}\text{ (operating)}}{f}$	V_{CC} = 5.25 V, f = 1 MHz to 25 MHz	V_I = 0 or V_{CC},	I_O = 0,		2		$\frac{\text{mA}}{\text{MHz}}$
ΔI_{CC}‡	V_{CC} = 5.25 V, Other inputs at 0 V or V_{CC}	V_I = 0.5 V or 2.4 V,			1.4	3	mA
C_i	f = 1 MHz,	V_I = 2 V			6		pF

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITION	MIN	TYP†	MAX	UNIT
f_{max}§	With feedback		R1 = 200 Ω, R2 = 390 Ω, C_L = 50 pF, See Figure 2	16			MHz
	Without feedback			25			
t_{pd}	I, I/O, feedback	O, I/O			35	55	ns
t_{pd}	CLK↑	Q			15	22	ns
t_{en}	$\overline{\text{OE}}$↓	Q			15	25	ns
t_{dis}	$\overline{\text{OE}}$↑	Q			15	25	ns
t_{en}	I, I/O	O, I/O			35	55	ns
t_{dis}	I, I/O	O, I/O			35	55	ns

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ This is the increase in supply current for each in[ut that is at one of the specified TTL voltage levels rather than 0 or V_{CC}.

§ f_{max} (with feedback) = $\frac{1}{t_{su} + t_{pd}(\text{CLK to Q})}$; f_{max} (without feedback) = $\frac{1}{t_{su}}$

preload procedure for registered outputs

The output registers can be preloaded to any desired state during device testing. This permits any state to be tested without having to step through the entire state-machine sequence. All of the registers may be preloaded simultaneously by following the steps below.

Step 1. With V_{CC} at 5 V and Pin 11 at V_{IH}, raise Pin 1 to V_{IHH}.
Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.
Step 3. Lower Pin 1 to V_{IL}, then remove the output voltage. Preload can be verified by lowering Pin 11 to V_{IL} and observing the voltage level at the output pins.

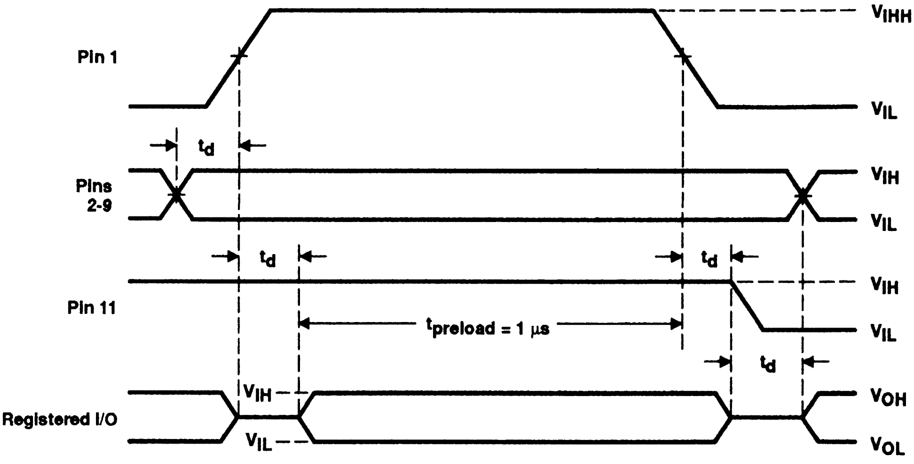


Figure 1. Preload Waveforms

preload recommended operating conditions, $T_A = 25°C$[†]

		MIN	NOM	MAX	UNIT
V_{IHH}	Preload voltage on pin 1	12.5	13	13.5	V
I_{IHH}	Preload input current at pin 1	3.2	4	4.8	mA
V_{IL}	Preload voltage transition rate	50			V/µs
t_d	Setup and hold times	2			µs

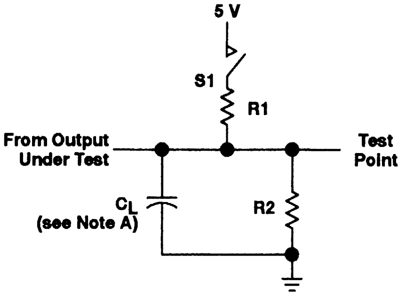
[†] Other test parameters and conditions are shown in recommended operating conditions and electrical characteristics tables.

programming information

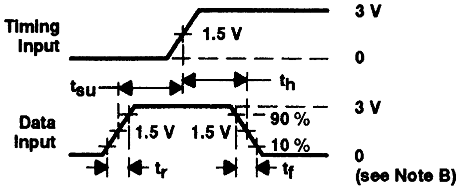
Texas Instruments programmable logic devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments programmable logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

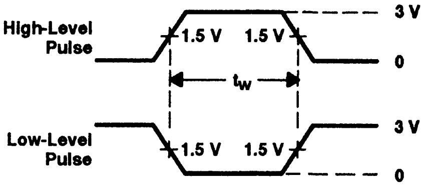
PARAMETER MEASUREMENT INFORMATION



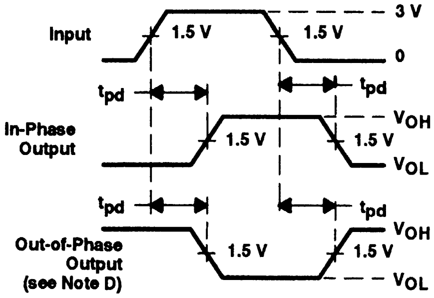
LOAD CIRCUIT FOR 3-STATE OUTPUTS



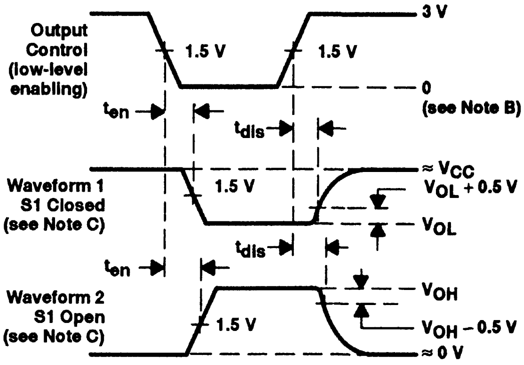
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATIONS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.

B. All input pulses have the following characteristics: PRR ≤ 1 MHz, Z_0 = 50 Ω, t_r = t_f = 6 ns, duty cycle = 50%

C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.

E. Equivalent loads may be used for testing.

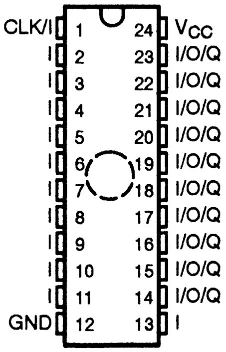
Figure 2. Load Circuit and Voltage Waveforms

TICPAL22V10Z-25C, TICPAL22V10Z-30I
EPIC™ CMOS PROGRAMMABLE ARRAY LOGIC CIRCUITS

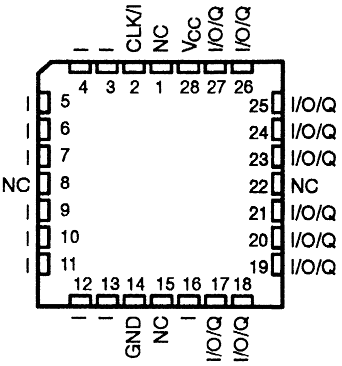
SRPS007C – D3323, SEPTEMBER 1989 – REVISED FEBRUARY 1992

- **24-Pin Advanced CMOS PLD**
- **Virtually Zero Standby Power**
- **Propagation Delay Time:**
  I, I/O to I/O in the Turbo Mode
  -25C . . . 25 ns Max
  -30I . . . 30 ns Max
  I, I/O to I/O in the Zero-Power Mode
  -25C . . . 35 ns Max
  -30I . . . 40 ns Max
  CLK to Q
  -25C . . . 15 ns Max
  -30I . . . 20 ns Max
- **Variable Product Term Distribution Allows More Complex Functions to Be Implemented**
- **Each Output Is User-Programmable for Registered or Combinatorial Operation, Polarity, and Output Enable Control**
- **Extra Terms Provide Logical Synchronous Set and Asynchronous Reset Capability**
- **Preload Capability on All Registered Outputs Allow for Improved Device Testing**
- **UV Light Erasable Cell Technology Allows for:**
  - **Reconfigurable Logic**
  - **Reprogrammable Cells**
  - **Full Factory Testing for High Programming Yield**
- **Programmable Design Security Bit Prevents Copying of Logic Stored in Device**
- **Package Options Include Plastic Dual-In-Line and Clip Carrier [for One-Time-Programmable (OTP) Devices] and Ceramic Dual-In-Line Windowed Package**

JTL AND NT PACKAGE
(TOP VIEW)



FN PACKAGE
(TOP VIEW)



NC – No internal connection
Pin assignments in operating mode

AVAILABLE OPTIONS

T_A RANGE	PACKAGE TYPE		
	CERAMIC WINDOWED DUAL-IN-LINE (JTL)	PLASTIC DUAL-IN-LINE (NT)	PLASTIC CHIP CARRIER (FN)
0°C to 75°C	TICPAL22V10Z-25CJTL	TICPAL22V10Z-25CNT	TICPAL22V10Z-25CFN
–40°C to 85°C	NA	TICPAL22V10Z-30INT	TICPAL22V10Z-30IFN

These devices are covered by U.S. Patent 4,410,987.
EPIC is a trademark of Texas Instruments Incorporated.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 1992, Texas Instruments Incorporated

TICPAL22V10Z-25C, TICPAL22V10Z-30I
EPIC™ CMOS PROGRAMMABLE ARRAY LOGIC CIRCUITS

SRPS007C – D3323, SEPTEMBER 1989 – REVISED FEBRUARY 1992

description

The CMOS PLD devices feature variable product terms, flexible outputs, and virtually zero standby power. It combines TI's EPIC™ (Enhanced Processed Implanted CMOS) process with ultraviolet-light-erasable EPROM technology. Each output has an output logic macrocell (OLM) configuration allowing for user definition of the output type. This device provides reliable, low-power substitutes for numerous high-performance TTL PLDs with gate complexities between 300 and 800 gates.

The TICPAL22V10Z has 12 dedicated inputs and 10 user-definable outputs. Individual outputs can be programmed as registered or combinational and inverting or noninverting as shown in the OLM diagram. These ten outputs are enabled through the use of individual product terms

The variable product-term distribution on this device removes rigid limitation to a maximum of eight product terms per output. This technique allocates from 8 to 16 logical product terms to each output for an average of 12 product terms per output. The variable allocation of product terms allows for far more complex functions to be implemented in this device than in previously available devices.

With features such as the programmable OLMs and the variable product-term distribution, the TICPAL22V10Z offers quick design and development of custom LSI functions. Since each of the ten output pins may be individually configured as inputs on either a temporary or permanent basis, functions requiring up to 21 inputs and a single output or down to 12 inputs and 10 outputs can be implemented with this device.

Design complexity is enhanced by the addition of synchronous set and asynchronous reset product terms. These functions are common to all registers. When the synchronous set product term is a logic 1, the output registers are loaded with a logic 1 on the next low-to-high clock transition. When the asynchronous reset product term is a logic 1, the output registers are loaded with a logic 0 independently of the clock. The output logic level after set or reset will depend on the polarity selected during programming.

Output registers of this device can be preloaded to any desired state during testing, thus allowing for full logical verification during product testing.

The TICPAL22V10Z has internal electrostatic discharge (ESD) protection circuits and has been classified with a 2000-V ESD rating tested under MIL-STD-883C, Method 3015.6. However, care should be exercised in handling these devices, as exposure to ESD may result in a degradation of the device parametric performance.

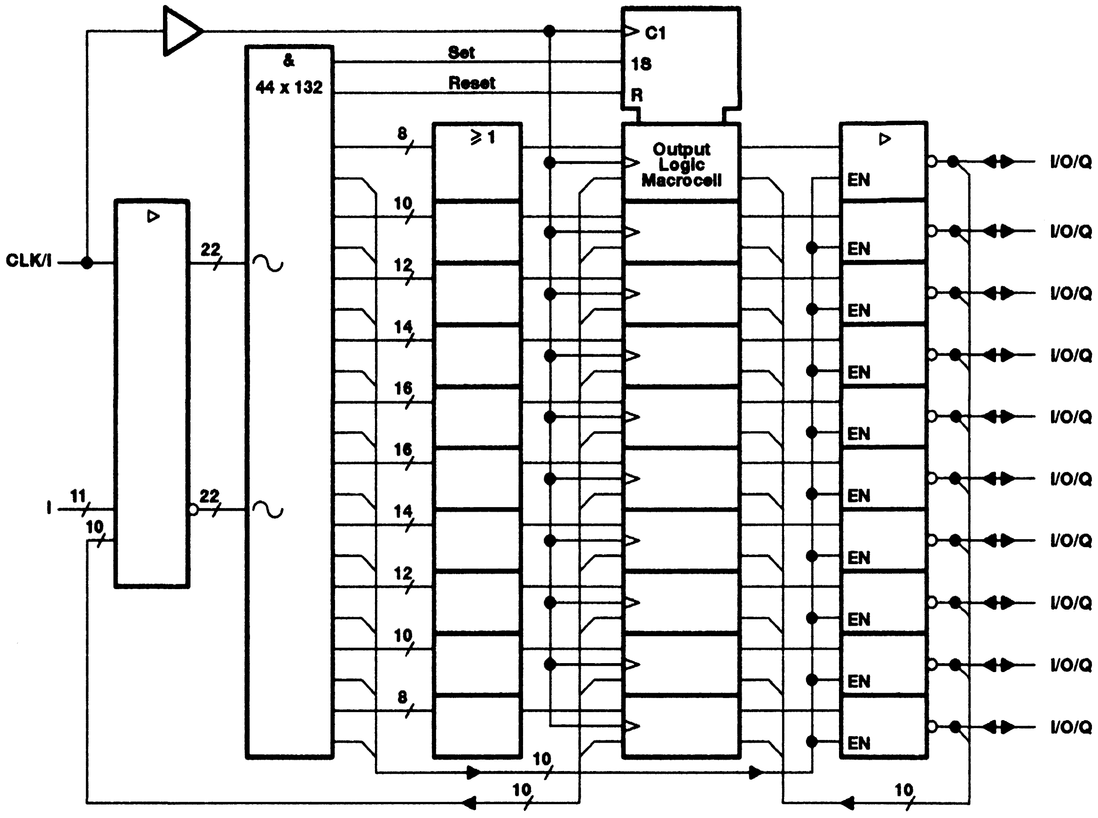
The floating-gate programmable cells allow the devices to be fully programmed and tested before assembly to assure high field programming yield and functionality. They are then erased by ultraviolet light before packaging.

The TICPAL22V10Z-25C is characterized for operation from 0°C to 75°C. The TICPAL22V10Z-30I is characterized for operation from −40°C to 85°C.

design security

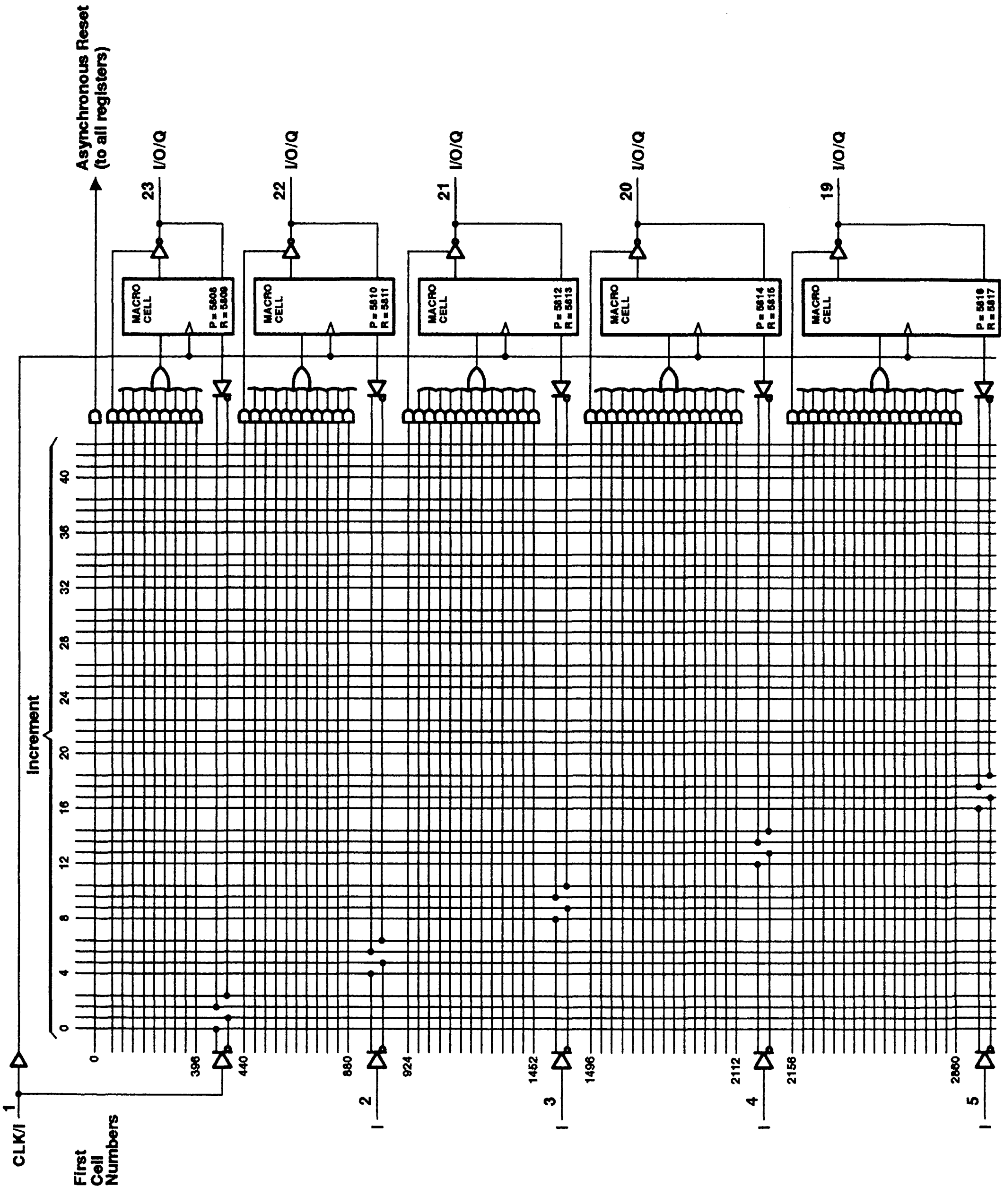
The 'PAL22V10Z contains a programmable design security cell. Programming this cell will disable the read verify and programming circuitry protecting the design from being copied. The security cell is usually programmed after the design is finalized and released to production. A secured device will verify as if every location in the device is programmed. Because programming is accomplished by storing an invisible charge instead of opening a metal link, the '22V10Z cannot be copied by visual inspection. Once a secured device is fully erased, it can be reprogrammed to any desired configuration.

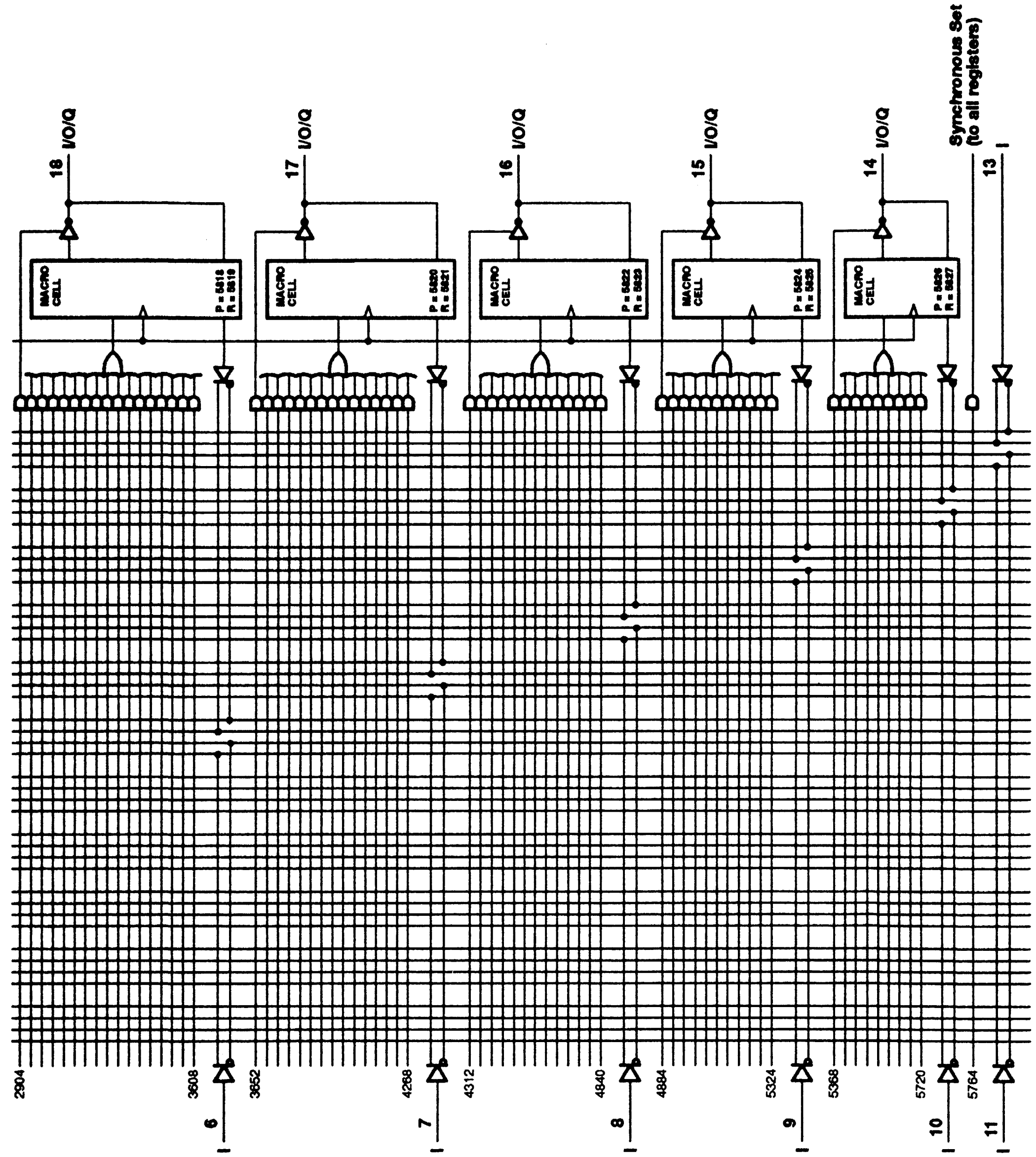
functional block diagram (positive logic)



∿ denotes programmable cell inputs

logic diagram (positive logic)





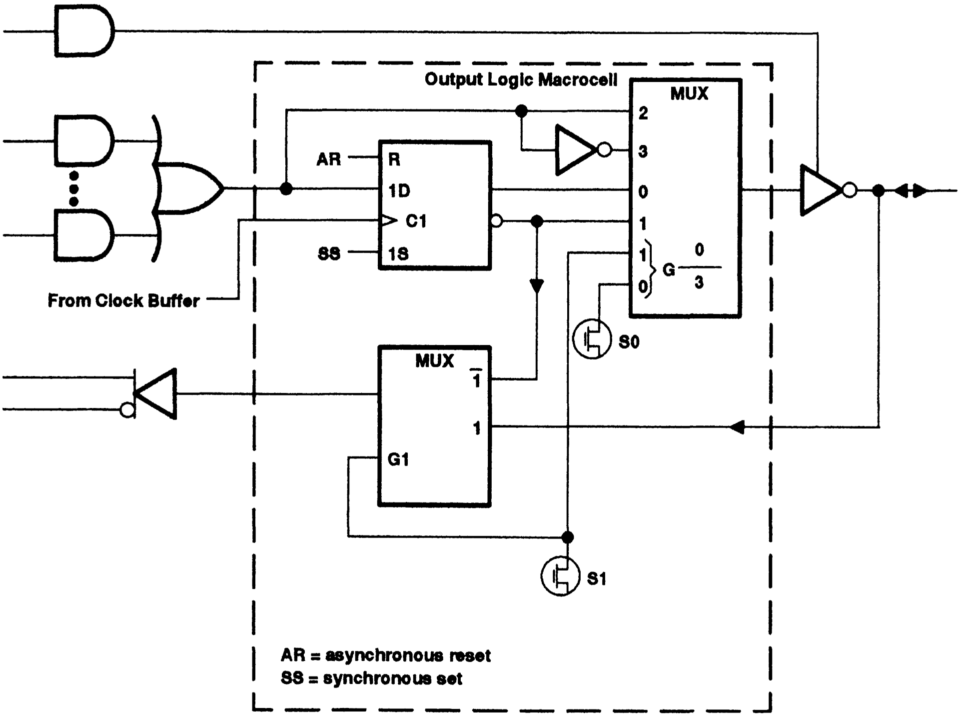
Programmable Cell Number = First Cell Number + Increment
Inside each MACROCELL the (P) cell is the polarity cell and the (R) cell is the register cell.

output logic macrocell (OLM) description

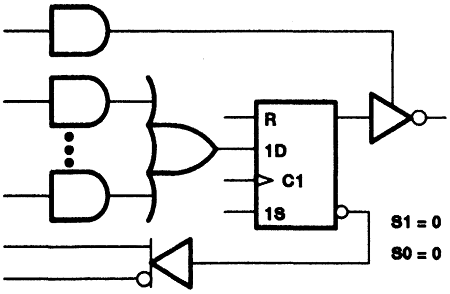
A great amount of architectural flexibility is provided by the user-configurable macrocell output options. The macrocell consists of a D-type flip-flop and two select multiplexers. The D-type flip-flop operates like a standard TTL D-type flip-flop. The input data is latched on the low-to-high transition of the clock input. The Q and $\overline{Q}$ outputs are made available to the output select multiplexer. The asynchronous reset and synchronous set controls are available in all flip-flops.

The select multiplexers are controlled by programmable cells. The combination of these programmable cells will determine which macrocell functions are implemented. It is this user control of the architectural structure that provides the generic flexibility of this device.

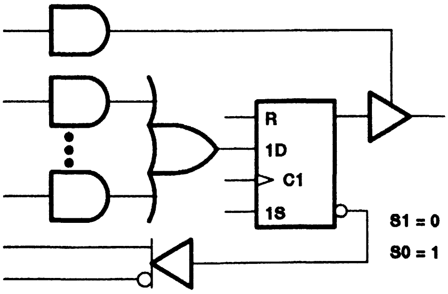
output logic macrocell diagram



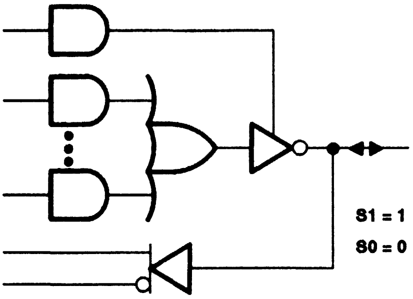
output logic macrocell options (see Figure 1)



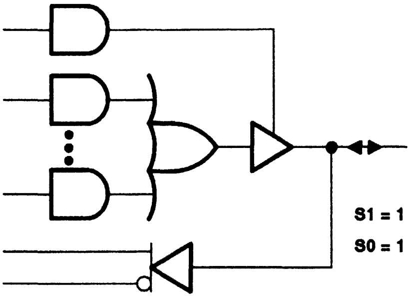
REGISTER FEEDBACK, REGISTERED, ACTIVE-LOW OUTPUT



REGISTER FEEDBACK, REGISTERED, ACTIVE-HIGH OUTPUT



I/O FEEDBACK, COMBINATIONAL, ACTIVE-LOW OUTPUT



I/O FEEDBACK, COMBINATIONAL, ACTIVE-HIGH OUTPUT

MACROCELL FEEDBACK AND OUTPUT FUNCTION TABLE

CELL SELECT		FEEDBACK AND OUTPUT CONFIGURATION		
S1	S0			
0	0	Register feedback	Registered	Active low
0	1	Register feedback	Registered	Active high
1	0	I/O feedback	Combinational	Active low
1	1	I/O feedback	Combinational	Active high

0 = erased cell, 1 = programmed cell
S1 and S0 are select-function cells as shown in the output logic macrocell diagram.

Figure 1. Resultant Macrocell Feedback and Output Logic After Programming

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC} .... –0.5 V to 7 V
Input voltage range, V_I (see Note 1) .... –0.5 V to V_{CC}+0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$) .... ±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$) .... ±20 mA
Continuous output current, I_O (V_O = 0 to V_{CC}) .... ±40 mA
Lead temperature 1,6 mm (1/16 in) from case for 10 seconds: FN or NT package .... 260°C
Lead temperature 1,6 mm (1/16 in) from case for 10 seconds: JTL package .... 300°C
Operating free-air temperature range .... 0°C to 75°C
Storage temperature range .... –65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: These ratings apply except for programming pins during a programming cycle or during a preload cycle.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	Driving TTL			–3.2	mA
		Driving CMOS			–4	
I_{OL}	Low-level output current	Driving TTL			16	mA
		Driving CMOS			4	
t_w	Pulse duration	Clock high	10			ns
		Clock low	10			
		Asynchronous reset	20			
t_{su}	Setup time, turbo mode	Input or feedback	17			ns
		Asynchronous reset inactive	20			
		Synchronous preset inactive	20			
t_{su}	Setup time, zero-power mode	Input or feedback	25			ns
		Asynchronous reset inactive	30			
		Synchronous preset inactive	30			
t_h	Hold time	Input or feedback	0			ns
T_A	Operating free-air temperature		0		75	°C

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITION		MIN	TYP†	MAX	UNIT
V_{OH}		V_{CC} = 4.75 V,	I_{OH} = −3.2 mA for TTL	4	4.8		V
		V_{CC} = 4.75 V,	I_{OH} = −4 mA for CMOS	3.86	4.7		
V_{OL}		V_{CC} = 4.75 V,	I_{OL} = 16 mA for TTL		0.25	0.5	V
		V_{CC} = 4.75 V,	I_{OL} = 4 mA for CMOS		0.07	0.4	
I_{OZH}		V_{CC} = 5.25 V,	V_O = 2.7 V		0.01	10	µA
I_{OZL}		V_{CC} = 5.25 V,	V_O = 0.5 V		−0.01	−10	µA
I_{IH}		V_{CC} = 5.25 V,	V_I = 5.25 V		0.01	10	µA
I_{IL}		V_{CC} = 5.25 V,	V_I = 0.5 V		−0.01	−10	µA
I_O‡		V_{CC} = 5.25 V,	V_O = 0.5 V	−30	−45	−90	mA
I_{CC}§		V_{CC} = 5.25 V, Outputs open,	V_I = 0 or V_{CC}, Zero-power mode		10	100	µA
C_i	I	V_I = 2 V,	f = 1 MHz		6		pF
	I/O				10		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 3)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
f_{max}¶	Without feedback			50	66		MHz
	With feedback			31.2	55		
t_{pd}	Turbo mode	I, I/O	O, I/O		16	25	ns
	Zero-power mode				21	35	
t_{pd}	Turbo mode	Asynchronous RESET	Q		18	30	ns
	Zero-power mode				23	40	
t_{pd}		CLK↑	Q		10	15	ns
t_{en}	Turbo mode	I, I/O	I, Q, I/O		15	25	ns
	Zero-power mode				20	35	
t_{dis}	Turbo mode	I, I/O	I, Q, I/O		15	25	ns
	Zero-power mode				17	35	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second. V_O is set at 0.5 V to avoid test problems caused by test equipment ground degradation.

§ Disabled outputs are tied to GND or V_{CC}.

¶ f_{max} (with feedback) $= \dfrac{1}{t_{su} + t_{pd}(\text{CLK to Q})}$; f_{max} (without feedback) $= \dfrac{1}{t_{w(high)} + t_{w(low)}}$

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, V_{CC}	−0.5 V to 7 V
Input voltage range, V_I (see Note 1)	−0.5 V to V_{CC}+0.5 V
Input clamp current, I_{IK} ($V_I < 0$ or $V_I > V_{CC}$)	±20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±40 mA
Lead temperature 1,6 mm (1/16 in) from case for 10 seconds: FN or NT package	260°C
Operating free-air temperature range	−40°C to 85°C
Storage temperature range	−65°C to 150°C

† Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTE 1: These ratings apply except for programming pins during a programming cycle or during a preload cycle.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current	Driving TTL			−3.2	mA
		Driving CMOS			−4	
I_{OL}	Low-level output current	Driving TTL			16	mA
		Driving CMOS			4	
t_w	Pulse duration	Clock high	12			ns
		Clock low	12			
		Asynchronous reset	30			
t_{su}	Setup time, turbo mode	Input or feedback	22			ns
		Asynchronous reset inactive	25			
		Synchronous preset inactive	25			
t_{su}	Setup time, zero-power mode	Input or feedback	30			ns
		Asynchronous reset inactive	35			
		Synchronous preset inactive	35			
t_h	Hold time	Input or feedback	0			ns
T_A	Operating free-air temperature		−40		85	°C

electrical characteristics over recommended operating free-air temperature range

PARAMETER		TEST CONDITION		MIN	TYP†	MAX	UNIT
V_{OH}		V_{CC} = 4.5 V,	I_{OH} = −3.2 mA for TTL	4	4.8		V
		V_{CC} = 4.5 V,	I_{OH} = −4 mA for CMOS	3.86	4.7		
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 16 mA for TTL		0.25	0.5	V
		V_{CC} = 4.5 V,	I_{OL} = 4 mA for CMOS		0.07	0.4	
I_{OZH}		V_{CC} = 5.5 V,	V_O = 2.7 V		0.01	10	µA
I_{OZL}		V_{CC} = 5.5 V,	V_O = 0.5 V		−0.01	−10	µA
I_{IH}		V_{CC} = 5.5 V,	V_I = 5.5 V		0.01	10	µA
I_{IL}		V_{CC} = 5.5 V,	V_I = 0.5 V		−0.01	−10	µA
I_O‡		V_{CC} = 5.5 V,	V_O = 0.5 V	−30	−45	−90	mA
I_{CC}§		V_{CC} = 5.5 V, Outputs open,	V_I = 0 or V_{CC}, Zero-power mode		10	100	µA
C_i	I	V_I = 2 V,	f = 1 MHz		6		pF
	I/O				10		

switching characteristics over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Figure 3)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	TYP†	MAX	UNIT
f_{max}¶	Without feedback			41.6	66		MHz
	With feedback			23.8	55		
t_{pd}	Turbo mode	I, I/O	O, I/O		16	30	ns
	Zero-power mode				21	40	
t_{pd}	Turbo mode	Asynchronous RESET	Q		18	35	ns
	Zero-power mode				23	45	
t_{pd}		CLK↑	Q		10	20	ns
t_{en}	Turbo mode	I, I/O	I, Q, I/O		15	30	ns
	Zero-power mode				20	40	
t_{dis}	Turbo mode	I, I/O	I, Q, I/O		15	30	ns
	Zero-power mode				17	40	

† All typical values are at V_{CC} = 5 V, T_A = 25°C.

‡ Not more than one output should be shorted at a time, and the duration of the short circuit should not exceed one second. V_O is set at 0.5 V to avoid test problems caused by test equipment ground degradation.

§ Disabled outputs are tied to GND or V_{CC}.

¶ f_{max} (with feedback) $= \dfrac{1}{t_{su} + t_{pd}(\text{CLK to Q})}$; f_{max} (without feedback) $= \dfrac{1}{t_{w}(\text{high}) + t_{w}(\text{low})}$

preload procedure for registered outputs (see Notes 2 and 3)

The output registers can be preloaded to any desired state during device testing. This permits any state to be tested without having to setup through the entire state-machine sequence. Each register is preloaded individually by following the steps given below. The output level depends on the polarity selected during programming.

Step 1. With V_{CC} at 5 V and pin 1 at V_{IL}, raise pin 8 to V_{IHH}.
Step 2. Apply either V_{IL} or V_{IH} to the output corresponding to the register to be preloaded.
Step 3. Pulse pin 1, clocking in preload data.
Step 4. Remove output voltage, then lower pin 8 to V_{IL}. Preload can be verified by observing the voltage level at the output pin.

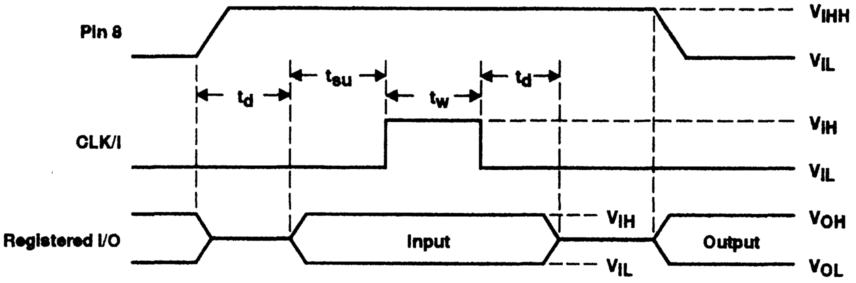


Figure 2. Preload Waveforms

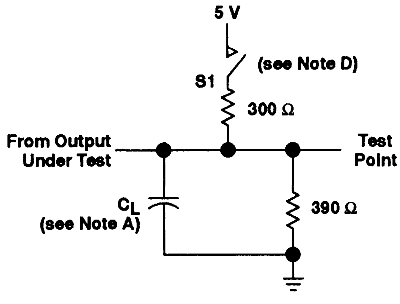
NOTES: 2. Pin numbers shown are for the JTL and NT packages only. If chip-carrier socket adapter is not used, pin numbers must be changed accordingly.
3. $t_d = t_{su} = t_w$ = 100 ns to 1000 ns. V_{IHH} = 10.25 V to 10.75 V.

programming information

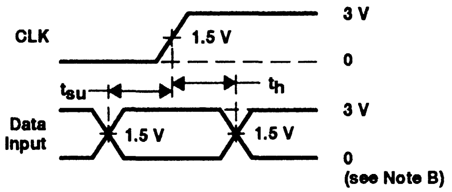
Texas Instruments programmable logic devices can be programmed using widely available software and inexpensive device programmers.

Complete programming specifications, algorithms, and the latest information on hardware, software, and firmware are available upon request. Information on programmers capable of programming Texas Instruments programmable logic is also available, upon request, from the nearest TI field sales office, local authorized TI distributor, or by calling Texas Instruments at (214) 997-5666.

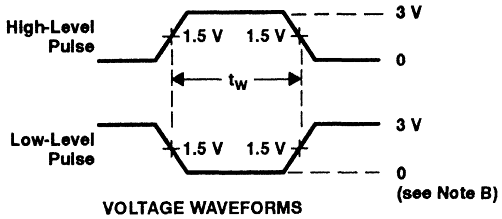
PARAMETER MEASUREMENT INFORMATION



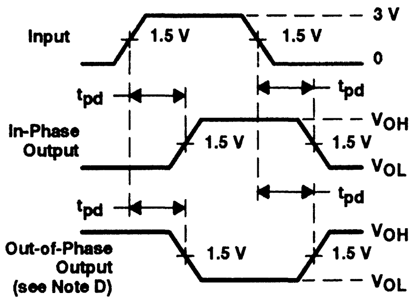
LOAD CIRCUIT FOR
3-STATE OUTPUTS



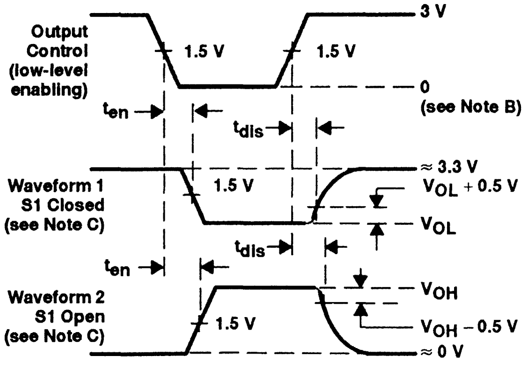
VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PULSE DURATIONS



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS

NOTES: A. C_L includes probe and jig capacitance and is 50 pF for t_{pd} and t_{en}, 5 pF for t_{dis}.
B. All input pulses have the following characteristics: PRR ≤ 1 MHz, $Z_O = 50\ \Omega$, $t_r = t_f = 2$ ns, duty cycle = 50%.
C. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
D. When measuring propagation delay times of 3-state outputs, switch S1 is closed.
E. Equivalent loads may be used for testing.

Figure 3. Load Circuit and Voltage Waveforms

special design features

True CMOS Outputs: Each TICPAL22V10Z output is designed with a P-channel pull-up transistor and an N-channel pull-down transistor, a true CMOS output with rail-to-rail output switching. This provides direct interface to CMOS logic, memory, or ASIC devices without the need for a pull-up resistor. The CMOS output has 16-mA drive capability, which makes the TICPAL22V10Z an ideal substitute for bipolar PLDs. The electrical characteristics of this device show the output under both CMOS and TTL conditions.

Simultaneous Switching: High-performance CMOS devices often have output glitches on nonswitched outputs when a large number of outputs are switched simultaneously. This glitch is commonly referred to as "ground bounce" and is most noticeable on outputs held at V_{OL} (low-level output voltage). Ground bounce is caused by the voltage drop across the inductance in the package lead when current is switched ($dv \alpha I x di/dt$).

One solution is to restrict the number of outputs that can switch simultaneously. Another solution is to change the device pinout such that the ground is located on a low-inductance package pin. TI opted for a third option in order to maintain pinout compatibility and eliminate functional constraints. This option controls the output transistor turn-on characteristics and puts a limit on the instantaneous current available to the load, much like the I_{OS} resistor in a TTL circuit.

Wake-Up Features: The TICPAL22V10Z employs input signal transition detection techniques to power up the device from the standby-power mode. The transition detector monitors all inputs, I/Os, and feedback paths. Whenever a transition is sensed, the detector activates the power-up mode. The device will remain in the power-up mode until the detector senses that the inputs and outputs have been static for about 40 ns; thereafter, the device returns to the standby mode.

Turbo Mode or Zero-Power Mode: When the turbo cell is programmed, the device will be set to the power-up mode. Therefore, the delay associated with its transition detection and power up will be eliminated. This is how the faster propagation delays and shorter setup times are obtained in the turbo mode. The turbo mode and the associated speed increase can be effectively simulated with the turbo cell erased, if a series of adjacent input, I/O, or feedback edges occur with an interval of about 25 ns or less between these adjacent edges. Under these conditions, the TICPAL22V10Z will never have the opportunity to power down due to the frequency of the adjacent edges.

Power Up: The TICPAL22V10Z device configuration bits (power mode, and macrocell configuration) are read at the first input transition after a monotonic power up. When completed, the TICPAL22V10Z is in its designed configuration. The use of an initializing device reset is necessary in applications where registered feedback is used to ensure the TICPAL22V10Z is in a known state at the beginning of system operation.

Power Dissipation: Power dissipation of the TICPAL22V10Z is defined by three contributing factors, and the total power dissipation is the sum of all three.

Standby Power: The product of V_{CC} and the standby I_{CC}. The standby current is the reverse current through the diodes that are reversed biased. This current is very small, and for circuits that remain in static condition for a long time, this low amount of current can become a major performance advantage.

Dynamic Power: The product of V_{CC} and the dynamic current. This dynamic current flows through the device only when the transistors are switching from one logic level to the other. The total dynamic current for the TICPAL22V10Z is dependent upon the users' configuration of the device and the operating frequency. Output loading can be a source of additional power dissipation.

Interface Power: The product of I_{CC} (interface) and V_{CC}. The total interface power is dependent on the number of inputs at the TTL V_{OH} level. The interface power can be eliminated by the addition of a pull-up resistor.

Even though power dissipation is a function of the user's device configuration and the operating frequency, the TICPAL22V10Z is a lower powered solution than either the quarter-powered or half-powered bipolar devices. The virtually zero standby power feature makes the TICPAL22V10Z the device of choice for low-duty-cycle applications.

programming and erasability

Programming of the TICPAL22V10Z is achieved through floating-gate avalanche injection techniques. The charge trapped on the floating gate remains after power has been removed, allowing for the nonvolatility of the programmed data. The charge can be removed by exposure to light with wavelengths of less than 400 nm (4000 Å). The recommended erasure wavelength is 253.7 nm (2537 Å), with erasure time of 60 to 90 minutes, using a light source with a power rating of 12000 μW/cm^2 placed within 2.5 cm (one inch) of the device.

The TICPAL22V10Z is designed for programming endurance of 1000 write/erase cycles with a data retention of ten years. To guarantee maximum data retention, the window on the device should be covered by an opaque label. The fluorescent light in a room can erase a unit in three years or, in the case of a direct sunlight, erasure can be complete in one week.

TYPICAL CHARACTERISTICS

OUTPUT CURRENT
vs
OUTPUT VOLTAGE

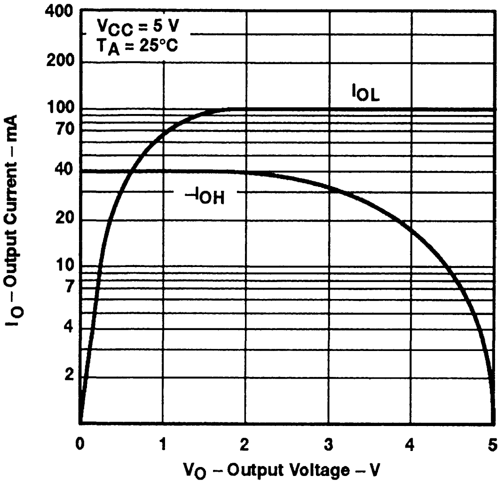


Figure 4

NORMALIZED SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE
(10-BIT COUNTER)

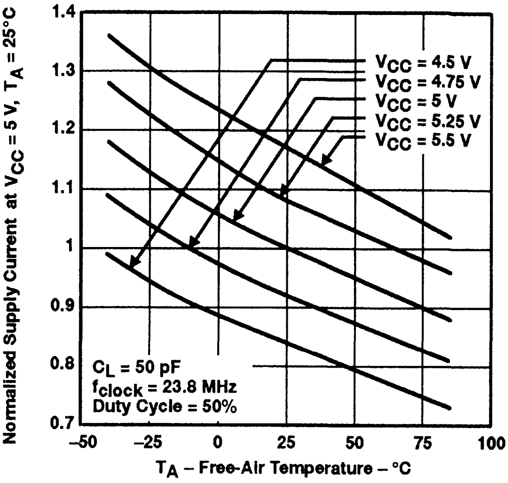


Figure 5

SUPPLY CURRENT
vs
CLOCK FREQUENCY
(10-BIT COUNTER)

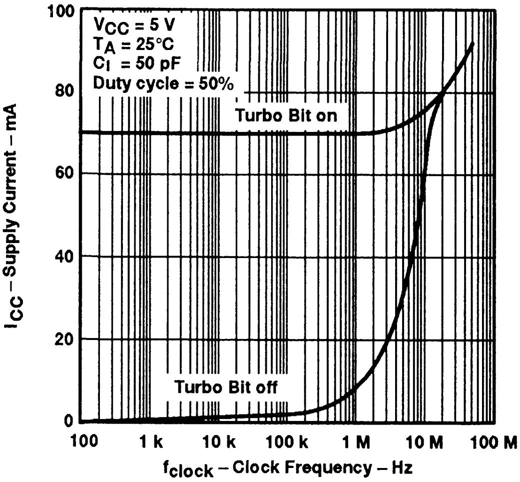


Figure 6

NORMALIZED PROPAGATION DELAY TIME
vs
SUPPLY VOLTAGE

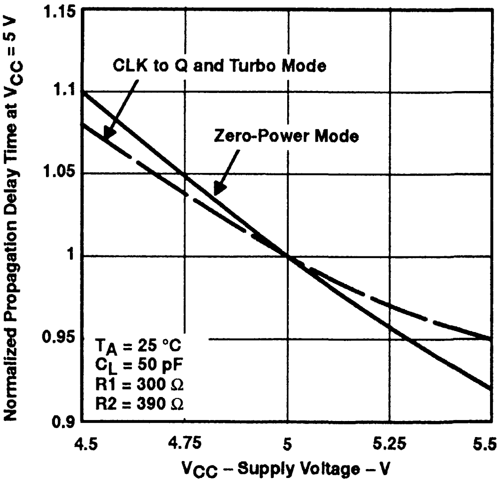


Figure 7

TYPICAL CHARACTERISTICS

NORMALIZED PROPAGATION DELAY TIME vs FREE-AIR TEMPERATURE

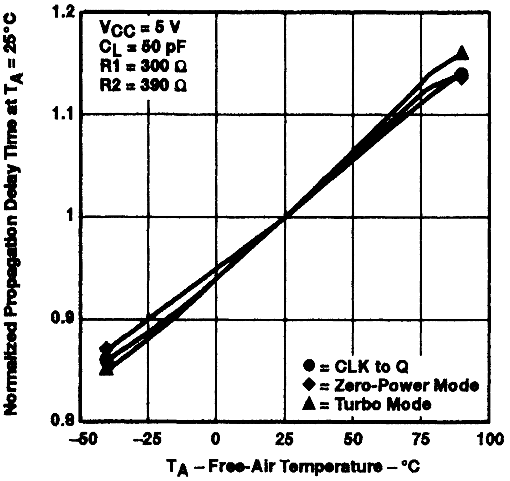


Figure 8

CHANGE IN PROPAGATION DELAY TIME vs LOAD CAPACITANCE

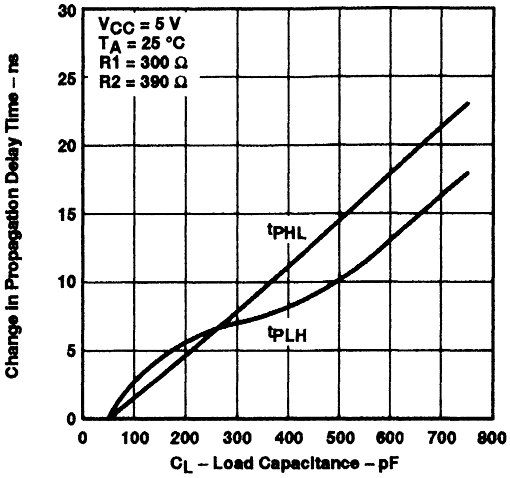


Figure 9

CHANGE IN PROPAGATION DELAY TIME vs NUMBER OF OUTOUTS SWITCHING

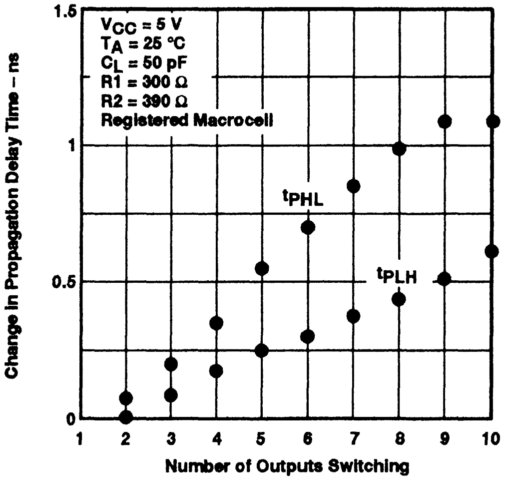


Figure 10

Introduction to Designing with Programmable Logic

TEXAS
INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to current specifications in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Please be aware that TI products are not intended for use in life-support appliances, devices, or systems. Use of TI product in such applications requires the written approval of the appropriate TI officer. Certain applications using semiconductor devices may involve potential risks of personal injury, property damage, or loss of life. In order to minimize these risks, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards. Inclusion of TI products in such applications is understood to be fully at the risk of the customer using TI devices or systems.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Copyright © 1992, Texas Instruments Incorporated

Contents

Figures

Tables

Introduction to Designing with Programmable Logic

Introduction

The purpose of this report is to provide the first time user of programmable logic with a basic understanding of this powerful technology. The term Programmable Logic Device (PLD), refers to any device supplied with an uncommitted logic array, which the user programs to his own specific function.

Programmable Logic Advantages

Programmable logic devices (PLDs) offer many advantages to the system designer who presently is using several standard catalog SSI and MSI functions. Listed below are just a few of the benefits which are achievable when using programmable logic.

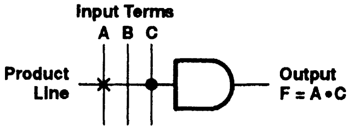
- Package Count Reduction: Several MSI/SSI functions can be replaced with one PLD. This reduces system power requirements.
- PC Board Area Reduced: Fewer devices consume less PC board space.
- Circuit Flexibility: Programmability allows for minor circuit changes without changing PC boards.
- Improved Reliability: With fewer PC interconnects, overall system reliability increases.
- Shorter Design Cycle: When compared with standard-cell or gate-array approaches, custom functions can be implemented much more quickly.
- Proprietary Design Protection (fuse protection): Circuit can be protected by blowing the security fuse.

The PLD will fill the gap between standard logic and large scale integration. The versatility of these devices provide a very powerful tool for the system designer.

Symbology for PLDs

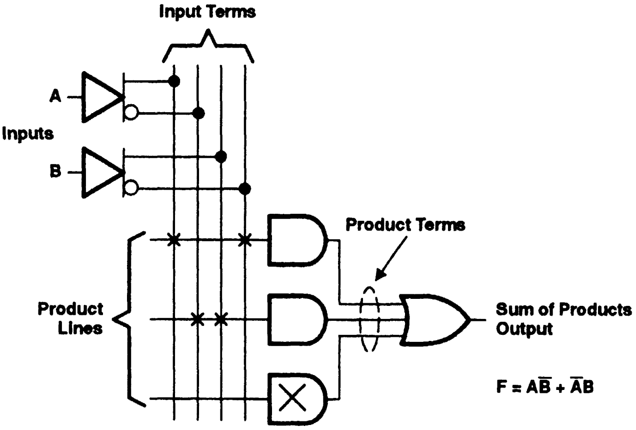
In order to keep the PLDs easy to understand and use, a special convention has been adopted. Figure 1 is the representation for a 3-input AND gate. Note that only one line is shown as the input to the AND gate. This line is commonly referred to as the product line. The inputs are shown as vertical lines, and at the intersection of these lines are the programmable fuses. An X represents an intact fuse. This makes that input, part of the product term. No X represents a blown fuse. This means that input will not be part of the product term (in Figure 1, input B is not part of the product term). A dot at the intersection of any line represents a hard-wire connection.

Figure 1. Basic Symbology



In Figure 2, we will extend the symbology to develop a simple 2-input programmable AND array feeding an OR gate. Notice that buffers have been added to the inputs, which provide both true and complement outputs to the product lines. The intersection of the input terms form a 4 x 3 programmable AND array. From the above symbology, we can see that the output of the OR gate is programmed to the following equation, $A\overline{B} + \overline{A}B$. Note that the bottom AND gate has an X marked inside the gate symbol. This means that all fuses are left intact, which results in that product line not having any effect on the sum term. In other words, the output of the AND gate will be a logic 0. When all the fuses are blown on a product line, the output of the AND gate will always be a logic 1. This has the effect of locking up the output of the OR gate to a logic level 1.

Figure 2. Basic Symbology Example

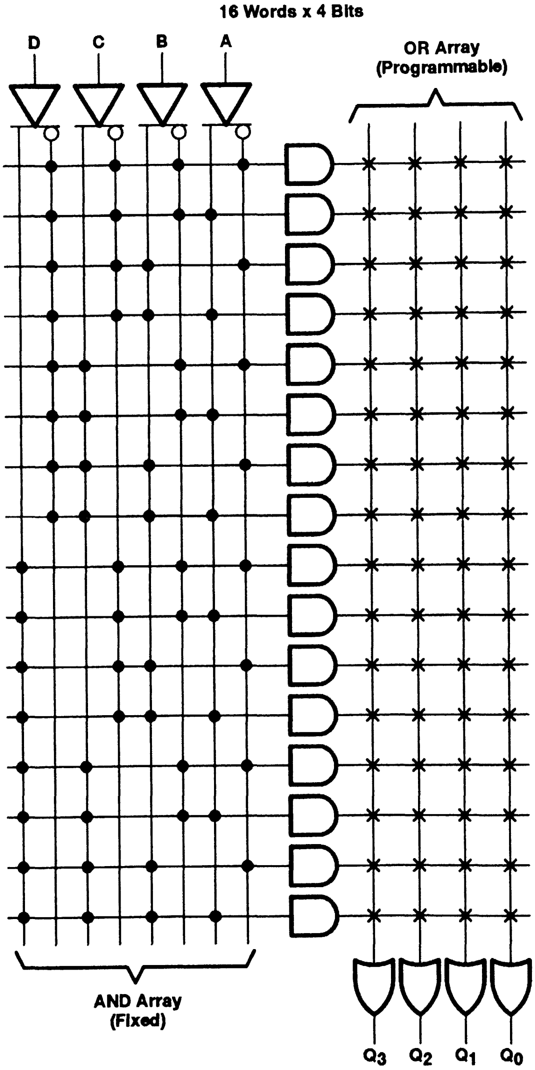


Family Architectures

The PROM was the first widely used programmable logic family. Its basic architecture is an input decoder configured from AND gates, combined with a programmable OR matrix on the outputs. As shown in Figure 3, this allows every output to be programmed individually from every possible input combination. In this example, a PROM with 4 inputs has 2^4, or 16 possible input combinations. With the output word width being 4 bits, each of the 16 x 4 bit words can be programmed individually. Applications such as data storage tables, character generators, and code converters are just a few design examples which are ideally suited for the

PROM. In general, any application which requires every input combination to be programmable is a good candidate for a PROM. However, PROMs have difficulty accommodating large numbers of input variables. Eventually, the size of the fuse matrix will become prohibitive because for each input variable added, the size of the fuse matrix doubles.

Figure 3. *PROM Architecture*



To overcome the limitation of a restricted number of inputs, the PLD utilizes a slightly different architecture as shown in Figure 4. The same AND-OR implementation is used as with PROMs, but now the input AND array is programmable instead of the output OR array. This has the effect of restricting the output OR array to a fixed number of input AND terms. The trade-off is that now, every output is not programmable from every input combination, but more inputs can be added without doubling the size of the fuse matrix. For example, if we were to expand the inputs on the PLD shown in. Figure 4 to ten and on the PROM in Figure 3 to ten, we would see that the fuse matrix required for the PLD would be 20 x 16 (320 fuses) versus 4 x 1024 (4096 fuses for the PROM). It is important to realize that not every application requires every output to be programmable from every input combination. This makes the PLD a viable product family.

The FPLA goes one step further in offering both a programmable AND array and a programmable OR array (Figure 5). This feature makes the FPLA the most versatile device of the three, but often impractical in most low complexity applications. For applications in which complex timing control is required, Texas Instruments (TI) offers several programmable state machines based on the FPLA architecture. Several of these devices incorporate internal state registers or on-chip binary counters to aid in generating complex timing sequences.

Another type of programmable logic device (PLD) is the erasable programmable logic device (EPLD). Based on the traditional PLD architecture, these devices typically offer a higher level of flexibility in the input and output configuration, register selection, and clocking options. CMOS EPLDs provide a higher level of density over standard PLDs and have lower power dissipation characteristics than bipolar PLDS. All programmable logic approaches discussed have their own unique advantages and limitations. The best choice depends on the complexity of the function being implemented and the current cost of the devices themselves. It is important to realize that a circuit solution may exist for more than one of these logic families.

Figure 4. *PLD Architecture*

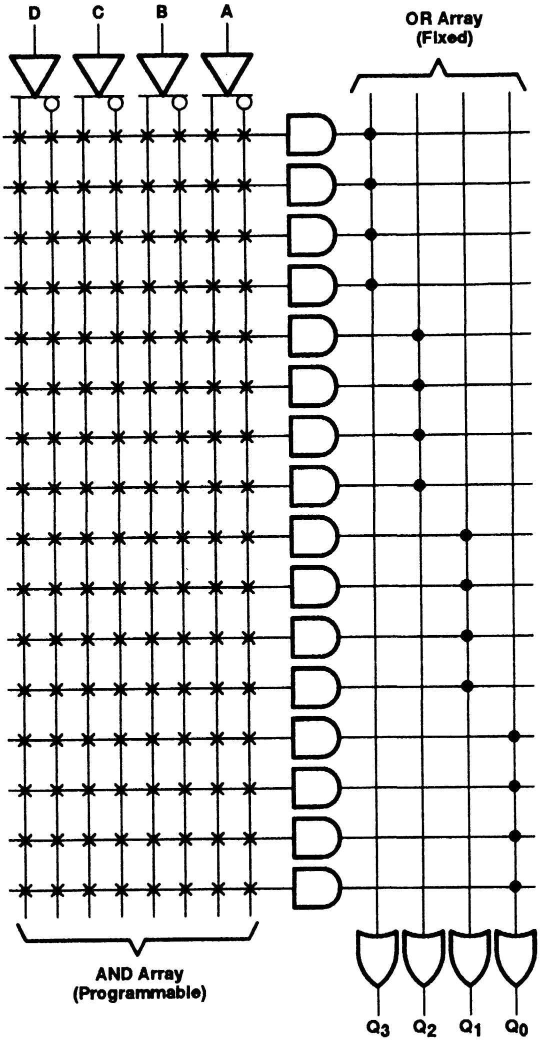
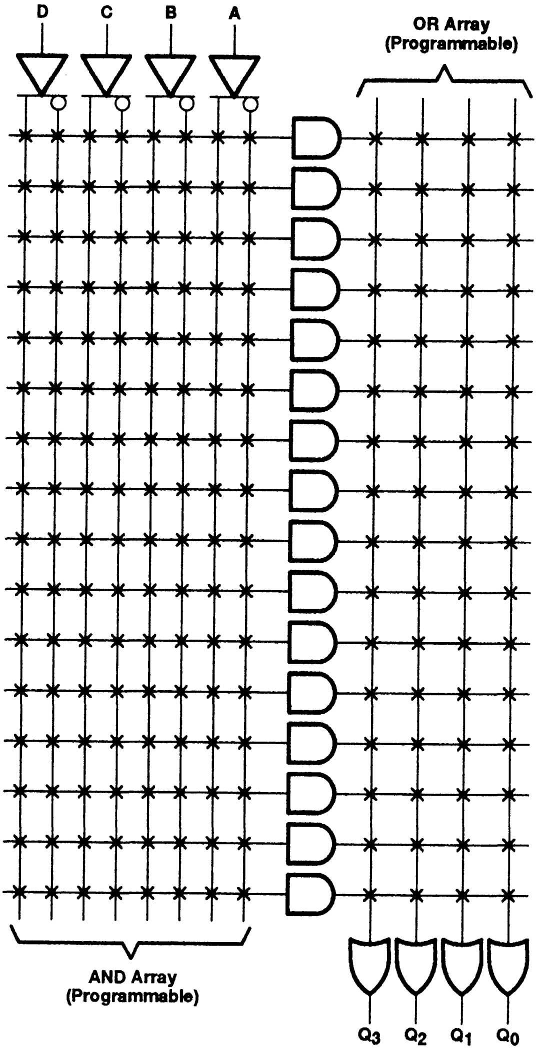


Figure 5. FPLA Architecture



PLD Options

Figure 6 shows the logic diagram of the popular TIBPAL16L8. Its basic architecture is the same as discussed in the previous section, but with the addition of some special circuit features. First, notice that the PLD has ten simple inputs. In addition, six of the outputs operate as I/O ports. This allows feedback into the AND array. One AND gate in each product term controls each 3-state output. The architecture used in this PLD makes it very useful in generating all sorts of combinational logic.

Another important feature about the logic diagram and all other block diagrams supplied from individual datasheets are that there are no Xs marked at every fuse location. From the previous convention, we stated that everywhere there was an intact fuse, there was an X. However, in order to make the logic diagram useful when generating specific functions, it is supplied with no Xs. This allows the user to insert the Xs wherever an intact fuse is desired.

The basic concept of the TIBPAL16L8 can be expanded further to include D-type flip-flops on the outputs. An example of this is shown in Figure 7, with the TIBPAL16R8. This additional feature allows the device to be configured as a counter, simple storage register, or similar clocked function.

Circuit variations which are available for other members of the TI PLD family are explained in the following paragraphs.

Figure 6. TIBPAL16L8 Logic Diagram

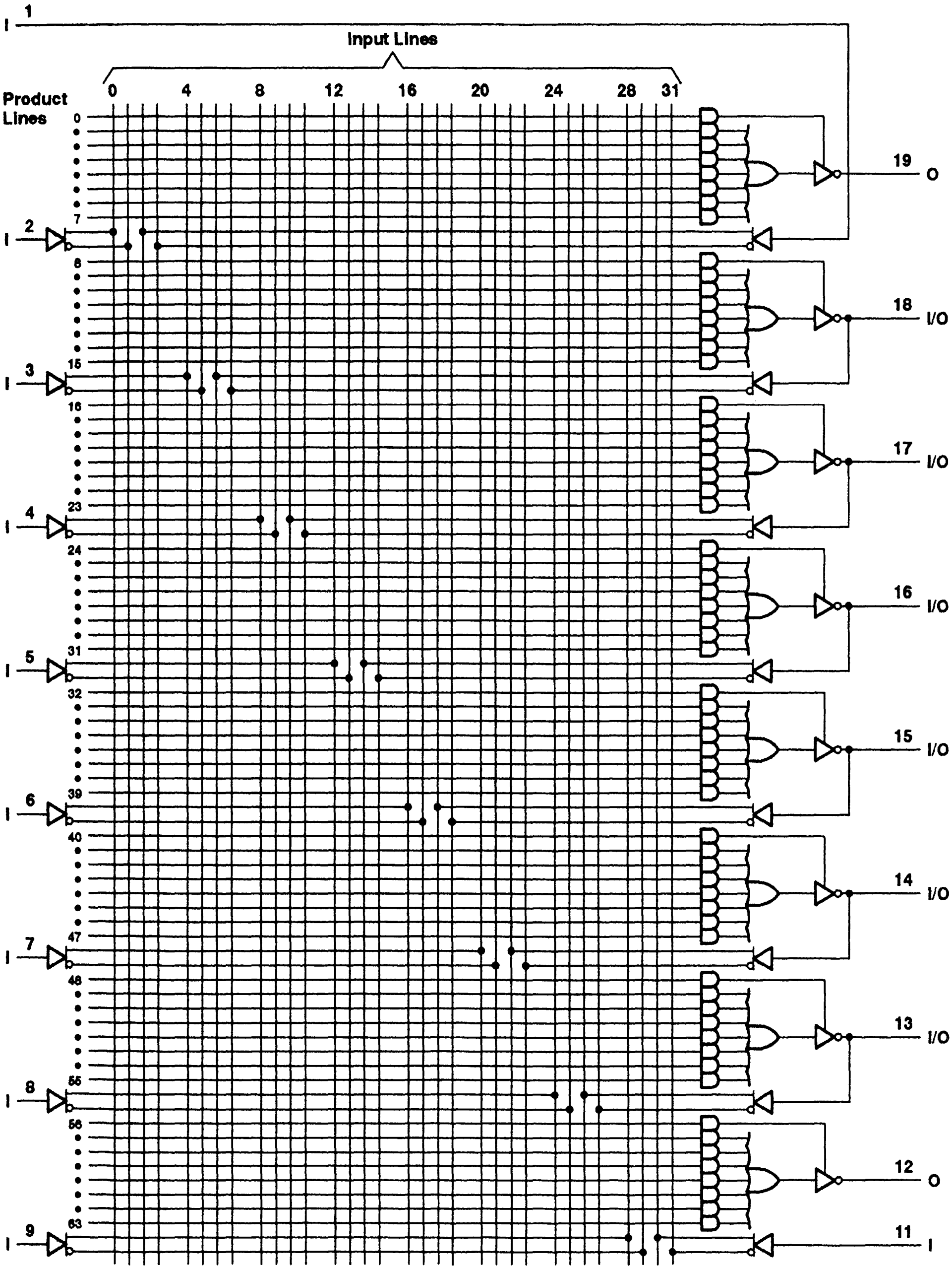
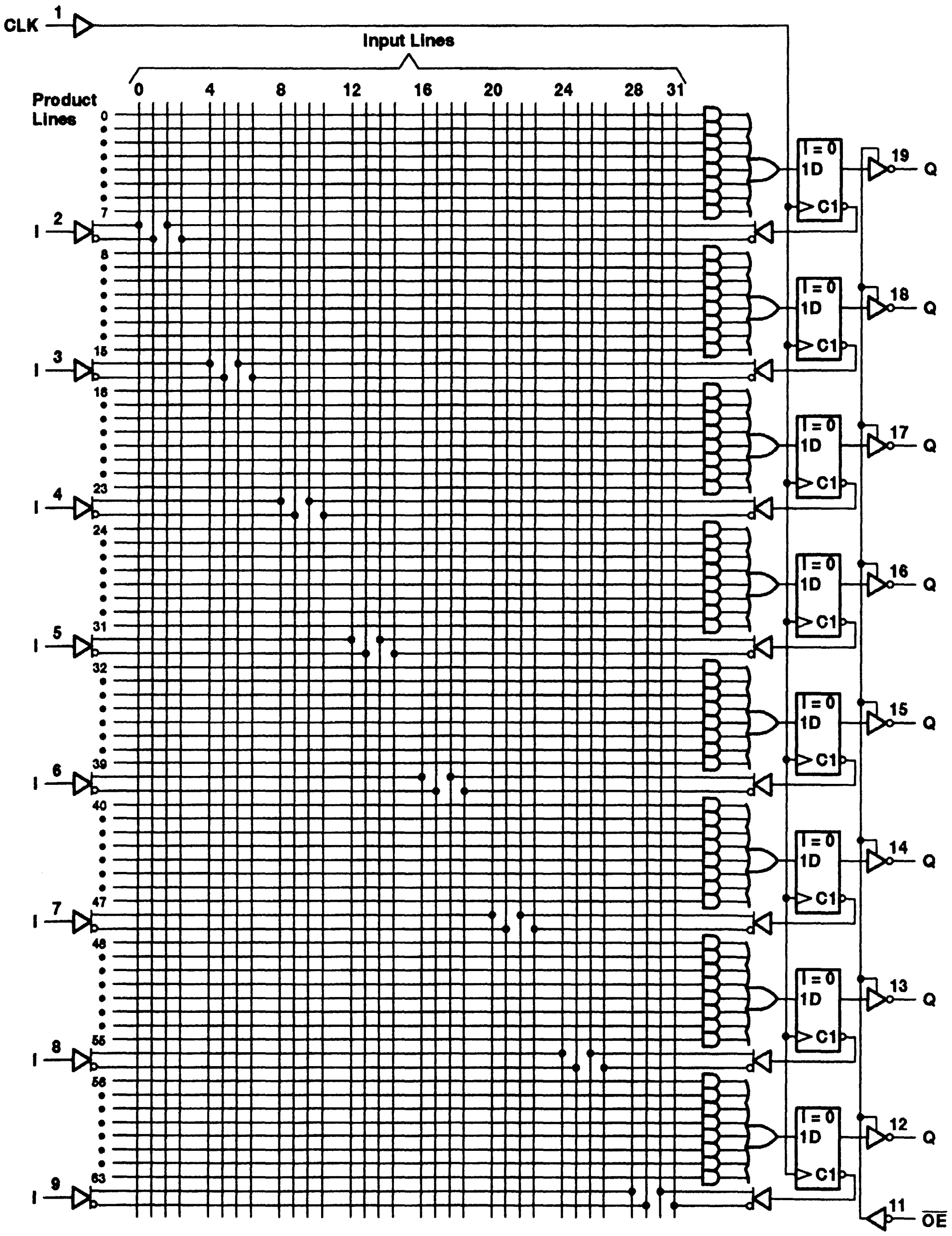


Figure 7. TIBPAL16R8 Logic Diagram



Output Macrocell

PLDs equipped with the output macrocell offer total output flexibility. Figures 8 and 9 show examples of these types of features as implemented in the TIBPAL22V10 device. Fuses S0 and S1 allow selection between registered or combinational outputs as well as output polarity. Figure 10 illustrates the user options.

The user options are as follows:

4) Clock Polarity Select. The clock signal can be inverted via a clock polarity select fuse. This allows the transition of the register outputs to be on either the positive or negative edge of the clock pulse.

5) Internal-State Registers. Several devices offer internal-state registers, which are often called buried registers. With the internal-state register, the output of the register is fed back into the AND array rather than to an output pin. This feature can be used for timing control sequences.

6) Variable Product Terms. Some PLD device architectures vary the number of product terms associated with each output pin. This allows better utilization of the programmable array.

Figure 8. Polarity Selection

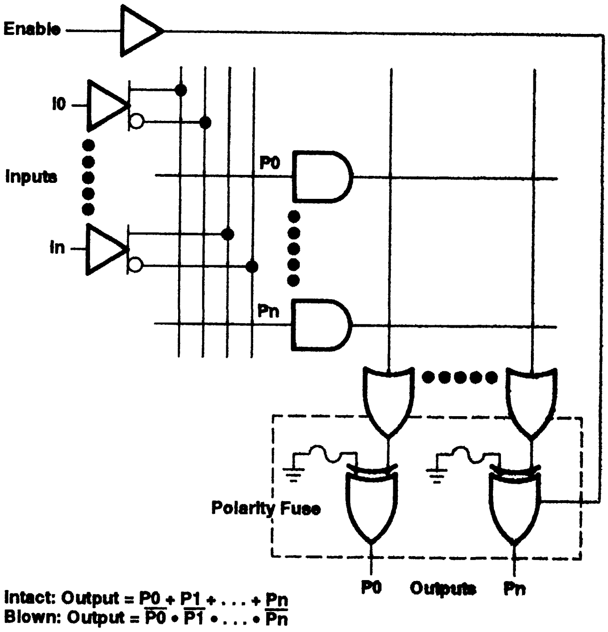


Figure 9. *Output Macrocell Diagram*

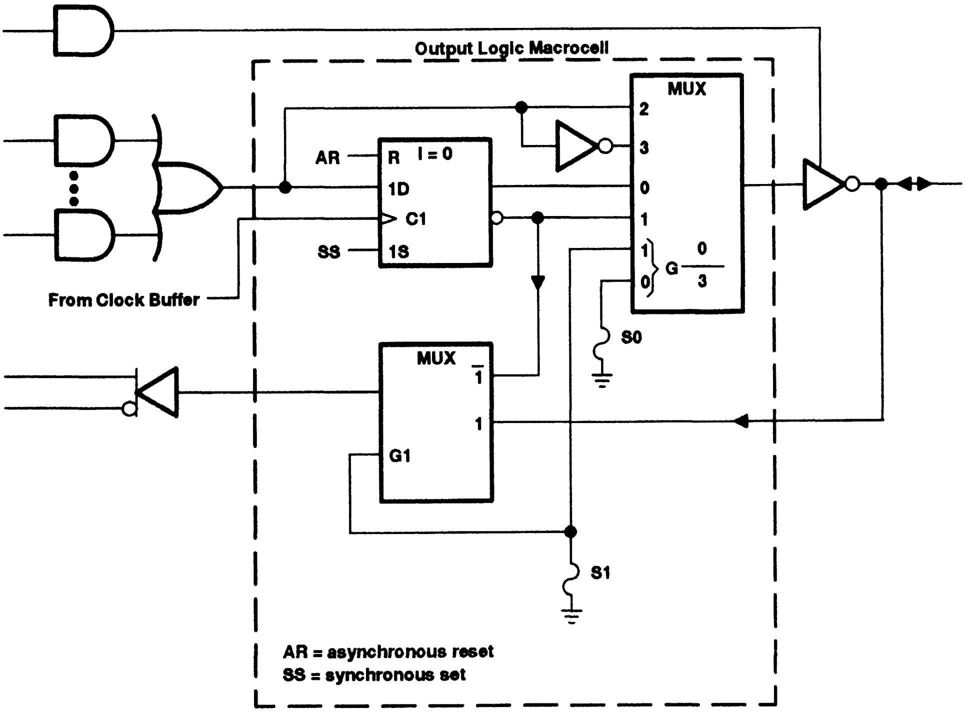
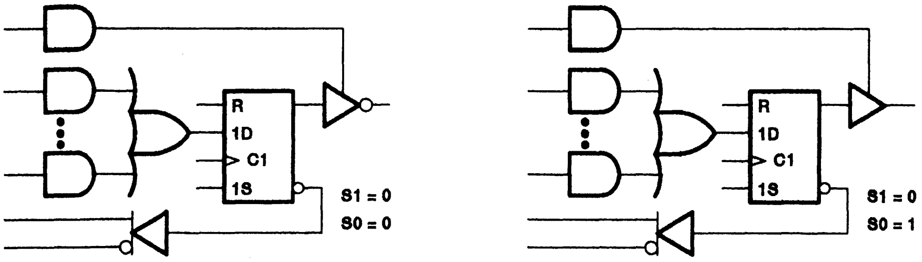
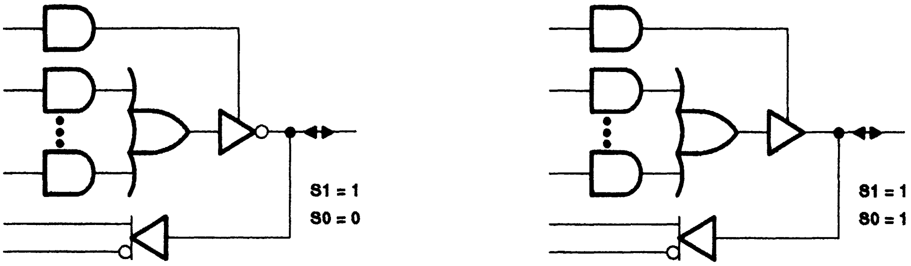


Figure 10. Resultant Macrocell Feedback and Output Logic After Programming



REGISTER FEEDBACK, REGISTERED, ACTIVE-LOW OUTPUT

REGISTER FEEDBACK, REGISTERED, ACTIVE-HIGH OUTPUT



I/O FEEDBACK, COMBINATIONAL, ACTIVE-LOW OUTPUT

I/O FEEDBACK, COMBINATIONAL, ACTIVE-HIGH OUTPUT

MACROCELL FEEDBACK AND OUTPUT FUNCTION TABLE

FUSE SELECT		FEEDBACK AND OUTPUT CONFIGURATION		
S1	S0			
0	0	Register feedback	Registered	Active low
0	1	Register feedback	Registered	Active high
1	0	I/O feedback	Combinational	Active low
1	1	I/O feedback	Combinational	Active high

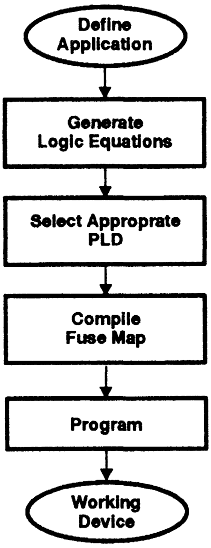
0 = unblown fuse, 1 = blown fuse

S1 and S0 are select-function fuses as shown in the output logic macrocell diagram.

Design Example

The best way to demonstrate the unique capabilities of the PLD is through a design example. Through this example, the user will gain the basic understanding needed to apply a PLD application. In some cases, this goal may only be to reduce existing logic, but the overall approach will be the same.

Figure 11. PLD Process Flow Diagram



Example Requirements

This example will generate a 4-bit binary counter which is fed by one of four clocks. There are two lines available for selecting the clocks, SEL1 and SEL0. Table 1 shows the required input for the selection of the clocks. In addition, it is desired that the counter be able to switch from binary to decade count. This feature is controlled by an input called BD. When BD is high, the counter will count in binary. When low, the counter will count in decade.

Table 1. Clock Selection

SEL1	SEL0	OUTPUT
0	0	CLKA
0	1	CLKB
1	0	CLKC
1	1	CLKD

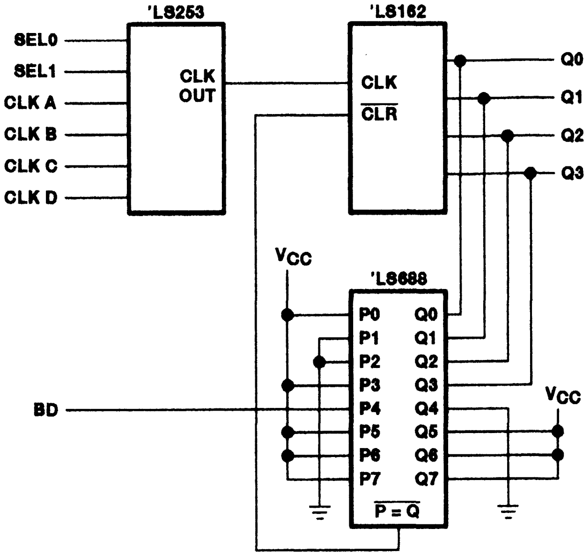
Figure 12 shows this example is implemented using standard logic. As shown, three MSI functions are required. The 'LS162 is used to generate the 4-bit counter while the clock selection is handled by the 'LS253. The 'LS688 is an 8-bit comparator which is used for selecting either the binary or decade count. In this example, only five of the eight comparator inputs are used. Four are used for comparing the counter outputs, while the other is used for the BD input. The comparator is hard wired to go low whenever the BD input is low and the counter output is count nine. The $\overline{P = Q}$ output is then fed back to the synchronous clear input of the 'LS162. This will reset the counter to zero whenever this condition occurs.

PLD Implementation

As stated before, the problem in programming a PLD is not in programming the fuses, but rather what fuses need to be programmed to generate a particular function. Fortunately, this problem has been greatly simplified by computer software. Before we examine these techniques, it is beneficial to explore the methods used in generating the logic equations. This will help develop an understanding and appreciation for these advanced software packages.

From digital logic theory, we know that almost any type of logic can be implemented in either AND-OR-INVERT or AND-NOR form. This is the basic concept used in the PLD. This allows classical techniques, such as Karnaugh Maps[1] to be used in generating specific logic functions. As with the separate component example (see Figure 12), it is easier to break it into separate functions. The first one that we will look at is the clock selector, but remember that the overall goal will be to reduce this design example into one PLD.

Figure 12. Counter implementation with Standard Logic



PLD Selection

Before proceeding with the design for the clock selector, the first question which needs to be addressed is which PLD to use. As discussed earlier, there are several different types of output architectures. Looking at our example, we can see that four flip-flops with feedback will be required in the 4-bit counter, plus input clock and clear lines. In addition, seven inputs plus two simple outputs will be required in the clock selector and comparator. With this information in hand, we can see that the TIBPAL16R4 (Figure 13) will handle our application.

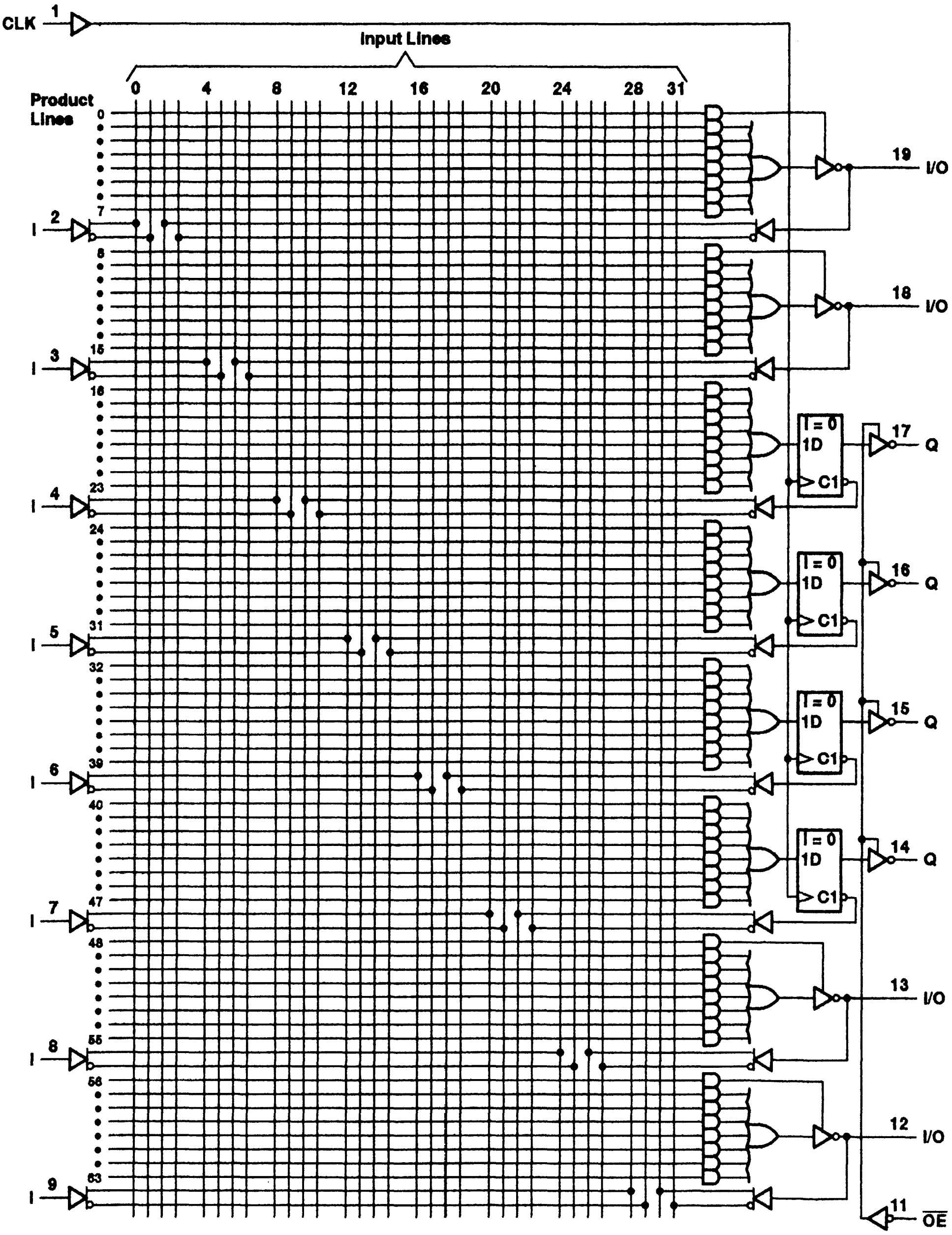
Clock Selector Details

The first step in determining the logic equation for the clock selector is to generate a function table with all the possible input combinations. This is shown in Table 2. From this table, the Karnaugh map can be generated and is shown in Figure 14. The minimized equation for CLKOUT comes directly from this.

Table 2. Function Table

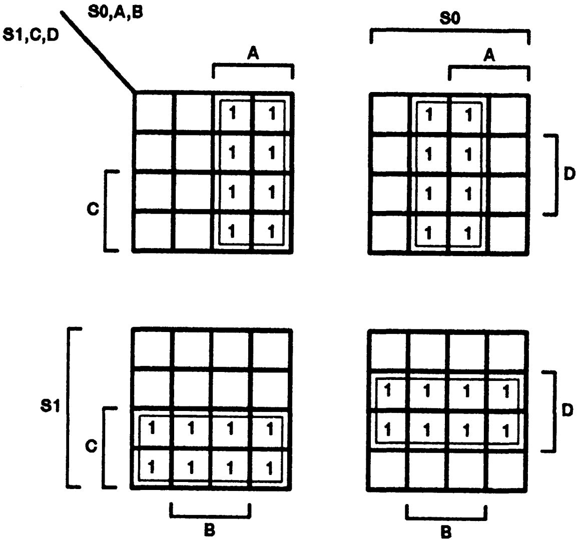
SEL1	SEL0	CLKA	CLKB	CLKC	CLKD	CLKOUT	SEL1	SEL0	CLKA	CLKB	CLKC	CLKD	CLKOUT
0	0	0	0	0	0	0	1	0	0	0	0	0	0
0	0	0	0	0	1	0	1	0	0	0	0	1	0
0	0	0	0	1	0	0	1	0	0	0	1	0	1
0	0	0	0	1	1	0	1	0	0	0	1	1	1
0	0	0	1	0	0	0	1	0	0	1	0	0	0
0	0	0	1	0	1	0	1	0	0	1	0	1	0
0	0	0	1	1	0	0	1	0	0	1	1	0	1
0	0	0	1	1	1	0	1	0	0	1	1	1	1
0	0	1	0	0	0	1	1	0	1	0	0	0	0
0	0	1	0	0	1	1	1	0	1	0	0	1	0
0	0	1	0	1	0	1	1	0	1	0	1	0	1
0	0	1	0	1	1	1	1	0	1	0	1	1	1
0	0	1	1	0	0	1	1	0	1	1	0	0	0
0	0	1	1	0	1	1	1	0	1	1	0	1	0
0	0	1	1	1	0	1	1	0	1	1	1	0	1
0	0	1	1	1	1	1	1	0	1	1	1	1	1
0	1	0	0	0	0	0	1	1	0	0	0	0	0
0	1	0	0	0	1	0	1	1	0	0	0	1	1
0	1	0	0	1	0	0	1	1	0	0	1	0	0
0	1	0	0	1	1	0	1	1	0	0	1	1	1
0	1	0	1	0	0	1	1	1	0	1	0	0	0
0	1	0	1	0	1	1	1	1	0	1	0	1	1
0	1	0	1	1	0	1	1	1	0	1	1	0	0
0	1	0	1	1	1	1	1	1	0	1	1	1	1
0	1	1	0	0	0	0	1	1	1	0	0	0	0
0	1	1	0	0	1	0	1	1	1	0	0	1	1
0	1	1	0	1	0	0	1	1	1	0	1	0	0
0	1	1	0	1	1	0	1	1	1	0	1	1	1
0	1	1	1	0	0	1	1	1	1	1	0	0	0
0	1	1	1	0	1	1	1	1	1	1	0	1	1
0	1	1	1	1	0	1	1	1	1	1	1	0	0
0	1	1	1	1	1	1	1	1	1	1	1	1	1

Figure 13. TIBPAL16R4 Logic Diagram



It is important to notice that the equation derived from the Karnaugh map is stated in AND-OR notation. The PLD that we have selected is implemented in AND-NOR logic. This means we either have to do DeMorgan's theorem on the equation or solve the inverse of the Karnaugh map. Figure 15 shows the inverse of the Karnaugh map and the resulting equation. This equation can be easily implemented in the TIBPAL16R4.

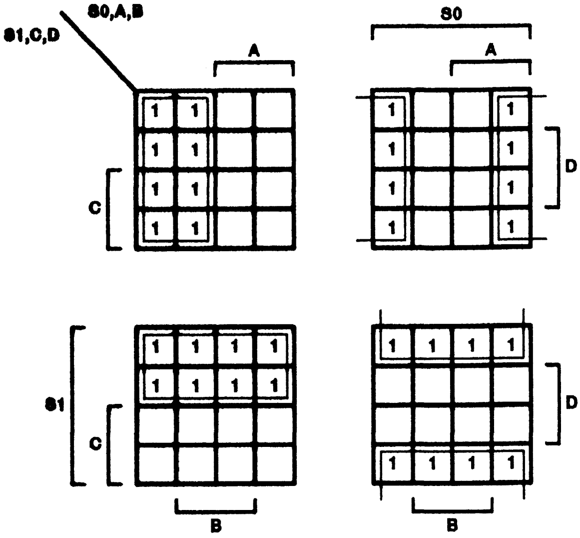
Figure 14. Karnaugh Map for CLKOUT



$$\mathrm{CLKOUT} = \overline{\mathrm{S1}}\,\overline{\mathrm{S0}}\mathrm{A}\cancel{\mathrm{B}}\cancel{\mathrm{C}}\cancel{\mathrm{D}} + \overline{\mathrm{S1}}\mathrm{S0}\cancel{\mathrm{A}}\mathrm{B}\cancel{\mathrm{C}}\cancel{\mathrm{D}} + \mathrm{S1}\overline{\mathrm{S0}}\cancel{\mathrm{A}}\cancel{\mathrm{B}}\mathrm{C}\cancel{\mathrm{D}} + \mathrm{S1}\mathrm{S0}\cancel{\mathrm{A}}\cancel{\mathrm{B}}\cancel{\mathrm{C}}\mathrm{D}$$

$$\mathrm{CLKOUT} = \overline{\mathrm{S1}}\,\overline{\mathrm{S0}}\mathrm{A} + \overline{\mathrm{S1}}\mathrm{S0B} + \mathrm{S1}\overline{\mathrm{S0}}\mathrm{C} + \mathrm{S1S0D}$$

Figure 15. Kamaugh Map for $\overline{CLKOUT}$



$\overline{CLKOUT} = \overline{S1}\,\overline{S0}A\cancel{B}\cancel{C}\cancel{D} + \overline{S1}S0\cancel{A}\overline{B}\cancel{C}\cancel{D} + S1\overline{S0}\cancel{A}\cancel{B}\overline{C}\cancel{D} + S1S0\cancel{A}\cancel{B}\cancel{C}\overline{D}$

$\overline{CLKOUT} = \overline{S1}\,\overline{S0A} + \overline{S1}S0\overline{B} + S1\overline{S0C} + S1S0\overline{D}$

4-Bit Binary Counter Details

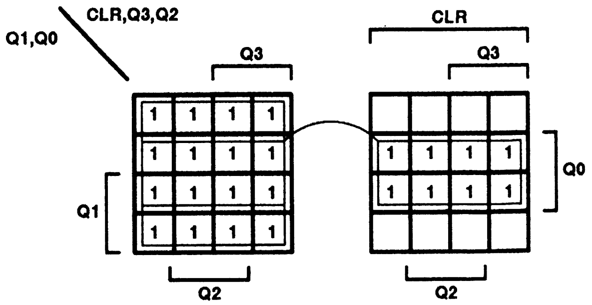
The same basic procedure used in determining the equations for the clock selector is used in determining the equations for the 4-bit counter. The only difference is that now we are dealing with a present state, next state situation. This means a D-type flip-flop will be required in actual circuit implementation. As before, the truth table is generated first and is shown in Table 3.

Table 3. Truth Table

	PRESENT STATE				NEXT STATE			
CLR	Q3	Q2	Q1	Q0	Q3	Q2	Q1	Q0
0	X	X	X	X	0	0	0	0
1	0	0	0	0	0	0	0	1
1	0	0	0	1	0	0	1	0
1	0	0	1	0	0	0	1	1
1	0	0	1	1	0	1	0	0
1	0	1	0	0	0	1	0	1
1	0	1	0	1	0	1	1	0
1	0	1	1	0	0	1	1	1
1	0	1	1	1	1	0	0	0
1	1	0	0	0	1	0	0	1
1	1	0	0	1	1	0	1	0
1	1	0	1	0	1	0	1	1
1	1	0	1	1	1	1	0	0
1	1	1	0	0	1	1	0	1
1	1	1	0	1	1	1	1	0
1	1	1	1	0	1	1	1	1
1	1	1	1	1	0	0	0	0

From the truth table, the equations for each output can be derived from the Karnaugh map. This is shown in Figure 16. Note that the inverse of the truth table is being solved so that the equation will come out in AND-NOR logic form.

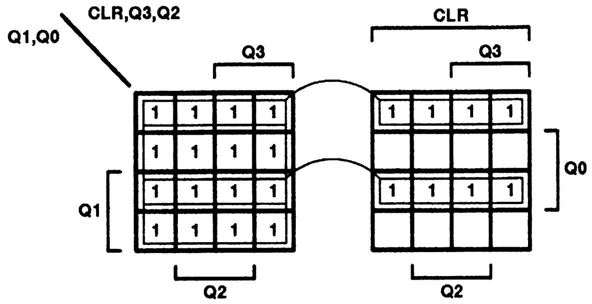
Figure 16. Karnaugh Maps



$$\overline{Q0} = \overline{CLR}\cancel{Q3}\cancel{Q2}\cancel{Q1}\cancel{Q0} + \cancel{CLR}\cancel{Q3}\cancel{Q2}\cancel{Q1}Q0$$

$$\overline{Q0} = \overline{CLR} + Q0$$

(a) Karnaugh Map for $\overline{Q0}$

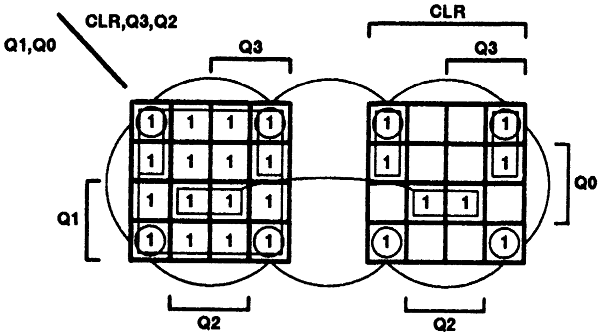


$$\overline{Q1} = \overline{CLR}\cancel{Q3}\cancel{Q2}\cancel{Q1}\cancel{Q0} + \cancel{CLR}\cancel{Q3}\cancel{Q2}\overline{Q1}\,\overline{Q0} + \cancel{CLR}\cancel{Q3}\cancel{Q2}Q1Q0$$

$$\overline{Q1} = \overline{CLR} + \overline{Q1}\,\overline{Q0} + Q1Q0$$

(b) Karnaugh Map for $\overline{Q1}$

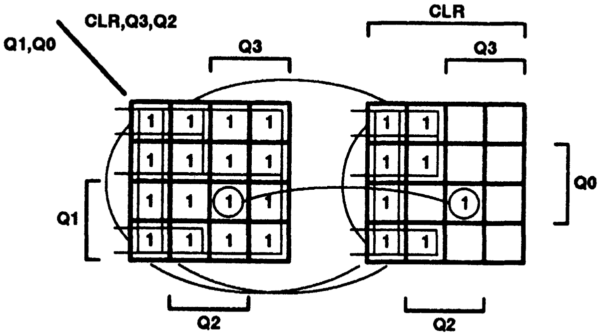
Figure 16. Karnaugh Maps (Continued)



$$\overline{Q2} = \overline{CLR}\cancel{Q3}\cancel{Q2}\cancel{Q1}\cancel{Q0} + \cancel{CLR}\cancel{Q3}\overline{Q2}\,\overline{Q1}\cancel{Q0} + \cancel{CLR}\cancel{Q3}Q2Q1Q0 + \cancel{CLR}\cancel{Q3}\overline{Q2}\cancel{Q1}\overline{Q0}$$

$$\overline{Q2} = \overline{CLR} + \overline{Q2}\,\overline{Q1} + Q2Q1Q0 + \overline{Q2}\,\overline{Q0}$$

(c) Karnaugh Map for $\overline{Q2}$



$$\overline{Q3} = \overline{CLR}\cancel{Q3}\cancel{Q2}\cancel{Q1}\cancel{Q0} + \cancel{CLR}\overline{Q3}\,\overline{Q2}\cancel{Q1}\cancel{Q0} + \cancel{CLR}\overline{Q3}\cancel{Q2}\overline{Q1}\cancel{Q0}$$
$$+ \cancel{CLR}\overline{Q3}\cancel{Q2}\cancel{Q1}\overline{Q0} + \cancel{CLR}Q3Q2Q1Q0$$

$$\overline{Q3} = \overline{CLR} + \overline{Q3}\,\overline{Q2} + \overline{Q3}\,\overline{Q1} + \overline{Q3}\,\overline{Q0} + Q3Q2Q1Q0$$

(d) Karnaugh Map for $\overline{Q3}$

Binary/Decade Count Details

Recalling from the example requirements that the counter should count in decade whenever the BD input is low, we can again generate a truth table for this function (Table 4). Since the counter is already designed to count in binary, we can use this feature to simplify our design. What we desire is a circuit whose output goes low, whenever the BD input is equal to a logic level 0, and the counter output is equal to count nine. This output can then be fed back to the CLR input of the counter so that it will reset whenever the BD input is low. Whenever the BD input is high, the output of the circuit should be a high since the counter will automatically count in binary. Notice that $\overline{Q}$ shown in the truth table is the function we desire.

Table 4. Truth Table

BD	Q3	Q2	Q1	Q0	Q	$\overline{Q}$	BD	Q3	Q2	Q1	Q0	Q	$\overline{Q}$
0	0	0	0	0	0	1	1	0	0	0	0	0	1
0	0	0	0	1	0	1	1	0	0	0	1	0	1
0	0	0	1	0	0	1	1	0	0	1	0	0	1
0	0	0	1	1	0	1	1	0	0	1	1	0	1
0	0	1	0	0	0	1	1	0	1	0	0	0	1
0	0	1	0	1	0	1	1	0	1	0	1	0	1
0	0	1	1	0	0	1	1	0	1	1	0	0	1
0	0	1	1	1	0	1	1	0	1	1	1	0	1
0	1	0	0	0	0	1	1	1	0	0	0	0	1
0	1	0	0	1	0	1	1	1	0	0	1	0	1
0	1	0	1	0	0	1	1	1	0	1	0	0	1
0	1	0	1	1	0	1	1	1	0	1	1	0	1
0	1	1	0	0	0	1	1	1	1	0	0	0	1
0	1	1	0	1	0	1	1	1	1	0	1	0	1
0	1	1	1	0	0	1	1	1	1	1	0	0	1
0	1	1	1	1	0	1	1	1	1	1	1	0	1

In this particular example, a Karnaugh map is not required because the equation cannot be further simplified. The resulting equation is given below.

$$\overline{\text{BD OUT}} = \overline{\text{BD}}\text{Q3}\overline{\text{Q2Q1}}\text{Q0}$$

Fuse Map Details

Now that the logic equations have been defined, the next step will be to specify which fuses need to be programmed. Before we do this however, we first need to label the input and output pins of the TIBPAL16R4. By using Figure 12 as a guide, we can make the following pin assignments in Figure 17.

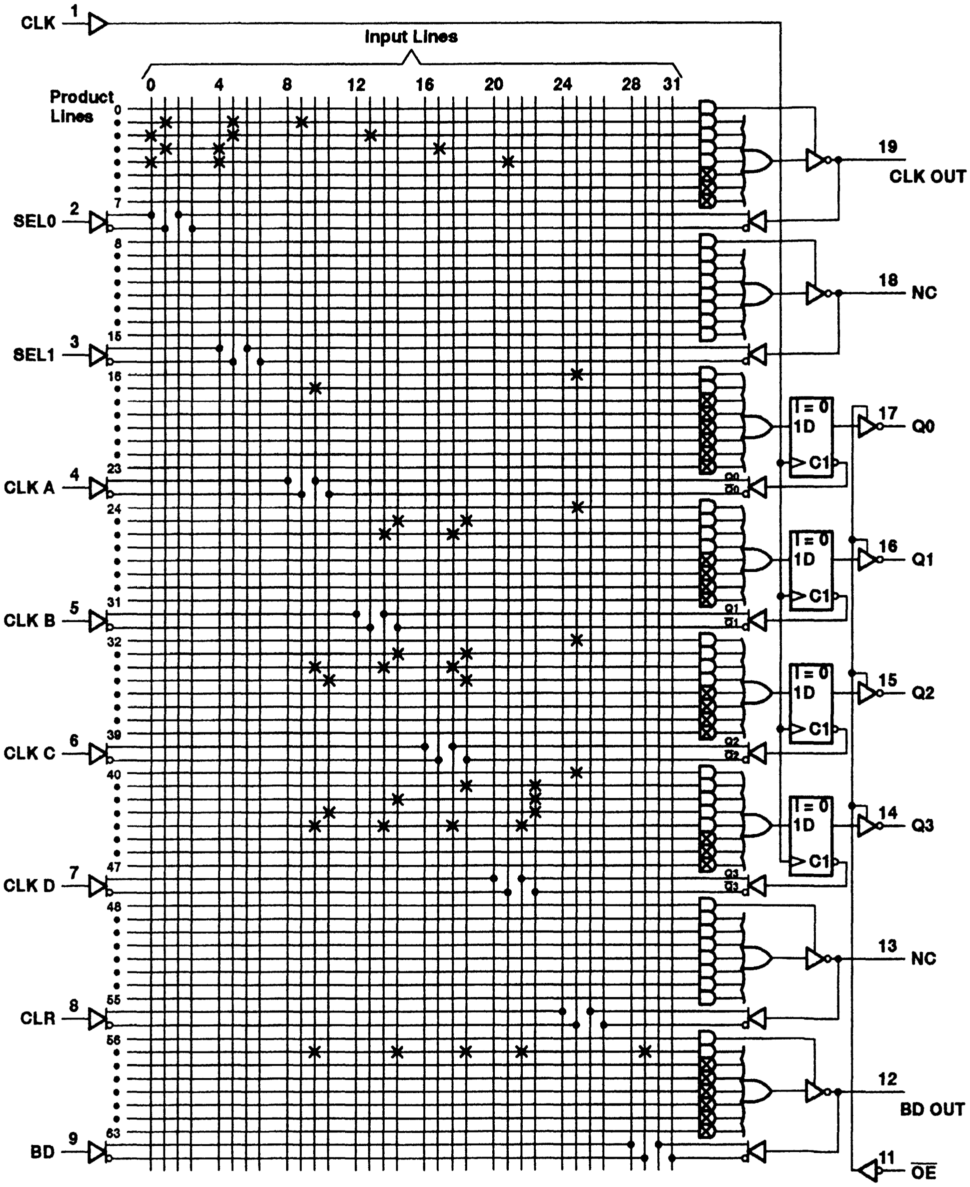
PIN:

1	CLK	20	V_{CC}
2	SEL0	19	CLKOUT
3	SEL1	18	NC
4	CLKA	17	Q0
5	CLKB	16	Q1
6	CLKC	15	Q2
7	CLKD	14	Q3
8	CLR	13	NC
9	BD	12	BD OUT
10	GND	11	OE

With this information defined, we now need to insert the logic equations into the logic diagram as shown in Figure 17.

It is now obvious that inserting the logic equations into the logic diagram is a tedious operation. Fortunately, several software programs are available to perform this task automatically. All that is required is to statewhich device has been selected and defining the input and output pins with their appropriate logic equations. The program will then generate a fuse map for the device selected. This information can then be down loaded into the selected device programmer.

Figure 17. Programmed TIBPAL16R4



PLD Design Software

Software packages such as ABEL™, CUPL™, and proLogic™ not only generate the fuse map, but they also help in developing the logic equations. In most cases, they can generate the logic equations from simply providing the program with either a truth table or state diagram. In addition, they can test the logic equations against a set of test vectors. This helps to ensure that the designer gets the desired function.

As an example, we will approach our previous design utilizing DATA I/O's ABEL package. The purpose here is not to train the reader how to use ABEL, but rather to give them a basic overview of this powerful software package. Figure 18 shows the source file required by ABEL. Note that the 4-bit counter has been described with a state diagram table. When the ABEL program is compiled, the logic equations will be generated. The equations for CLK OUT and BD OUT are given in their final form to demonstrate how ABEL will handle these. Also notice that test vectors are included for checking the logic equations. This is especially important when only the logic equations are given.

Figure 19 shows some of the output documentation generated by the program. Notice that the equations generated for the counter match the ones generated by the Karnaugh maps. A pinout for the device has also been generated and displayed. The fuse map for the device has not been shown; however, the standard JEDEC fuse map thus generated can be down loaded into the device programmer to program the selected PLD.

ABEL is a trademark of Data I/O Corporation
CUPL is a trademark of LOGICAL DEVICES, INC.
proLogic is a trademark of proLogic Systems Inc.

Figure 18.   Source File for ABEL

```
module BD_COUNT flag '-r2'
title '4-bit binary/decade counter

      IC1 device 'P16R4':

"  pin assignments and constant declarations
      CLK_IN,SEL0,SEL1,CLKA      pin 1,2,3,4;
      CLKB,CLKC,CLKD             pin 5,6,7;
      CLR,BD_IN,OE               pin 8,9,11;
      BD_OUT,CLK_OUT             pin 12,19;
      Q3,Q2,Q1,Q0                pin 14,15,16,17;
      CK, L, H, X, Z   =         .C., 0 , 1 , .X. , .Z.;
      OUTPUT                     [Q3,Q2,Q1,Q0];

"  counter states
      S0=^b0000;    S4=^b0100;    S8=^b1000;    S12=^b1100;
      S1=^b0001;    S5=^b0101;    S9=^b1001;    S13=^b1101;
      S2=^b0010;    S6=^b0110;   S10=^b1010;    S14=^b1110;
      S3=^b0011;    S7=^b0111;   S11=^b1011;    S15=^b1111;

equations
"  clock selector
      CLK_OUT = CLKA & !SEL0 & !SEL1 # CLKB & !SEL1 & SEL0
                # CLKC & SEL1 & !SEL0 # CLKD & SEL1 & SEL0;

"  count nine indicator for decade counting
      BD_OUT = !(!BD_IN & Q3 & !Q2 & !Q1 & Q0);

state_diagram [Q3,Q2,Q1,Q0]
       State  S0:  IF CLR == 0 THEN S0 ELSE  S1;
       State  S1:  IF CLR == 0 THEN S0 ELSE  S2;
       State  S2:  IF CLR == 0 THEN S0 ELSE  S3;
       State  S3:  IF CLR == 0 THEN S0 ELSE  S4;
       State  S4:  IF CLR == 0 THEN S0 ELSE  S5;
       State  S5:  IF CLR == 0 THEN S0 ELSE  S6;
       State  S6:  IF CLR == 0 THEN S0 ELSE  S7;
       State  S7:  IF CLR == 0 THEN S0 ELSE  S8;
       State  S8:  IF CLR == 0 THEN S0 ELSE  S9;
       State  S9:  IF CLR == 0 THEN S0 ELSE S10;
       State S10:  IF CLR == 0 THEN S0 ELSE S11;
       State S11:  IF CLR == 0 THEN S0 ELSE S12;
       State S12:  IF CLR == 0 THEN S0 ELSE S13;
       State S13:  IF CLR == 0 THEN S0 ELSE S14;
       State S14:  IF CLR == 0 THEN S0 ELSE S15;
       State S15:  IF CLR == 0 THEN S0 ELSE  S0;

test_vectors   'clock selector'
     ([CLKA, CLKB, CLKC, CLKD, SEL1, SEL0] -> CLK_OUT)
      [ L  ,  X  ,  X ,  X ,   L ,   L ] ->    L;
      [ H  ,  X  ,  X ,  X ,   L ,   L ] ->    H;
      [ X  ,  L  ,  X ,  X ,   L ,   H ] ->    L;
      [ X  ,  H  ,  X ,  X ,   L ,   H ] ->    H;
      [ X  ,  X  ,  L ,  X ,   H ,   L ] ->    L;
      [ X  ,  X  ,  H ,  X ,   H ,   L ] ->    H;
      [ X  ,  X  ,  X ,  L ,   H ,   H ] ->    L;
      [ X  ,  X  ,  X ,  H ,   H ,   H ] ->    H;
```

Figure 18 Source File for ABEL(Continued)

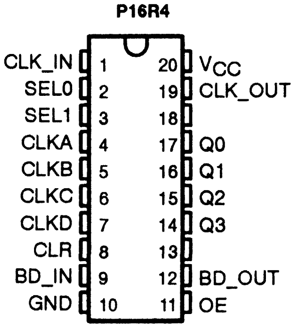
```
test_vectors   'counter'
     ([CLK_IN, OE, CLR, BD_IN] -> [OUTPUT, BD_OUT])
      [  CK,    L ,  L,     X  ] -> [  S0,   H ];
      [  CK,    L ,  H,     X  ] -> [  S1,   H ];
      [  CK,    L ,  H,     X  ] -> [  S2,   H ];
      [  CK,    L ,  H,     X  ] -> [  S3,   H ];
      [  CK,    L ,  H,     X  ] -> [  S4,   H ];
      [  CK,    L ,  H,     X  ] -> [  S5,   H ];
      [  CK,    L ,  H,     X  ] -> [  S6,   H ];
      [  CK,    L ,  H,     X  ] -> [  S7,   H ];
      [  CK,    L ,  H,     X  ] -> [  S8,   H ];
      [  CK,    L ,  H,     L  ] -> [  S9,   L ];
      [  CK,    L ,  H,     X  ] -> [ S10,   H ];
      [  CK,    L ,  H,     X  ] -> [ S11,   H ];
      [  CK,    L ,  H,     X  ] -> [ S12,   H ];
      [  CK,    L ,  H,     X  ] -> [ S13,   H ];
      [  CK,    L ,  H,     X  ] -> [ S14,   H ];
      [  CK,    L ,  H,     H  ] -> [ S15,   H ];
      [  CK,    L ,  H,     X  ] -> [  S0,   H ];
      [   X,    H ,  X,     X  ] -> [  Z ,   H ];
end BD_COUNT
```

Figure 19. ABEL Output Documentation

```
                                                           Page 1
ABEL(tm) Version 1.00 - Document Generator
4-bit binary/decade counter

Equations for Module BD_COUNT

Device IC1

     Reduced Equations:

        CLK_OUT = !((SEL1 & SEL0 & !CLKD
                   # (SEL1 & !SEL0 & !CLKC
                   # (!SEL1 & SEL0 & !CLKB
                   # !SEL1 & !SEL0 & !CLKA))));

        BD_OUT = !(Q3 & !Q2 & !Q1 & Q0 & !BD_IN);

        Q3 := !((Q3 & Q2 & Q1 & Q0
              # (!Q3 & !Q2
              # (!Q3 & !Q1
              # (!Q3 & !Q0
              # !CLR)))));

        Q2 := !((Q2 & Q1 & Q0 # (!Q2 & !Q1 # (!Q2 & !Q0 # !CLR))));

        Q1 := !((Q1 & Q0 # (!Q1 & !Q0 # !CLR)));

        Q0 := !((Q0 # !CLR));
```

Figure 19 ABEL Output Documentation (Continued)

```
                                                          Page 2
ABEL(tm) Version 1.00     Document Generator
4-bit binary/decade counter

Chip diagram for Module BD_COUNT

Device IC1
```



```
end of module BD_COUNT
```

Reference

1) H. Troy Nagle, Jr., B.D. Carroll, and David Irwin, *An Introduction to Computer Logic.* New Jersey: Prentice-Hall. Inc., 1975

Programmable Logic Device Design Software Support

TEXAS INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to current specifications in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Please be aware that TI products are not intended for use in life-support appliances, devices, or systems. Use of TI product in such applications requires the written approval of the appropriate TI officer. Certain applications using semiconductor devices may involve potential risks of personal injury, property damage, or loss of life. In order to minimize these risks, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards. Inclusion of TI products in such applications is understood to be fully at the risk of the customer using TI devices or systems.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Copyright © 1992, Texas Instruments Incorporated

TRADEMARKS

ABEL is a trademark of Data I/O Corporation.
CUPL is a trademark of LOGICAL DEVICES, INC.
PLDesigner is a trademark of MINC INCORPORATED.
proLogic is a trademark of proLogic Systems Inc..
IBM and PC-DOS are trademarks of International Business Machines.
MS-DOS is a trademark of Microsoft Corporation.

Programmable Logic Device Design Software Support

Introduction

There are a number of software products available to make logic designs easier and less cumbersome. With these software products, complex designs can be described using Boolean equations, truth tables, state machine diagrams and schematic capture methods available on most CAD systems.

The ultimate function of these software products is to generate a JEDEC file of the original design and to program the targeted Programmable Logic Device (PLD). However, most software vendors provide more than a JEDEC file as an output from the software. This section will describe the attributes of a few of the popular logic design products. We recommend that the reader contact the specific manufactures to obtain the latest and most comprehensive information available.

ABEL™ — Advanced Boolean Expression Language by DATA I/0 Corporation:

ABEL consists of a special-purpose, high-level language that is used to describe logic designs, and a language processor that converts logic descriptions to programmer load files — or JEDEC files. These files contain the information necessary to program and test programmable logic devices.

Features of ABEL design language:

- ❑ Universal Syntax for all PLDs
- ❑ High-Level, Structured Design Language
- ❑ Flexible Forms for Logic Description
    - Boolean Equations
    - Truth Tables
    - State Diagrams
- ❑ Test Vectors for Simulation and Functional Testing of Programmed Parts
- ❑ Time-Saving Macros and Directives

Some powerful features of the ABEL language processor:

- Syntax Checking
- Verification That a Design can be Implemented with a Chosen Part
- Logic Reduction
- Design Simulation
- Automatic Design Documentation
- Creation of Programmer Load Files in JEDEC Format

Between the ABEL design language and the language processor it becomes rather easy to design and test logic functions to be implemented with a PLD. For example, a three-input AND function with the inputs Q, R, and S and an output P could be designed using the following truth table:

```
truth_table "3-input AND gate"
 ([ Q, R, S ] -> P)

 [ 0, .X.,.X.] -> 0 :

 [ X, .0.,.X.] -> 0 :
 [ X, .X.,.0.] -> 0 :

 [ 1, 1, 1 ] -> 1 :
```

The `.X.` in the table indicate don't care conditions, and the output `P` is set to 1 only when all three inputs equal 1. The output could also be specified in simple Boolean operators and achieve the same result. In the following example `&` is the logical AND operator:

```
P = Q & R & S;
```

More Boolean Operators

Operator	Example	Description
!	!A	NOT: ones complement
&	A & B	AND
#	A # B	OR
$	A $ B	XOR: exclusive OR
!$	A !$ B	XNOR: exclusive NOR

ABEL allows designs to be described in the best possible manner to suit the logic to be implemented or in a manner suitable to the logic designer. In most cases the same description can be used for many different devices simply by changing the device specified.

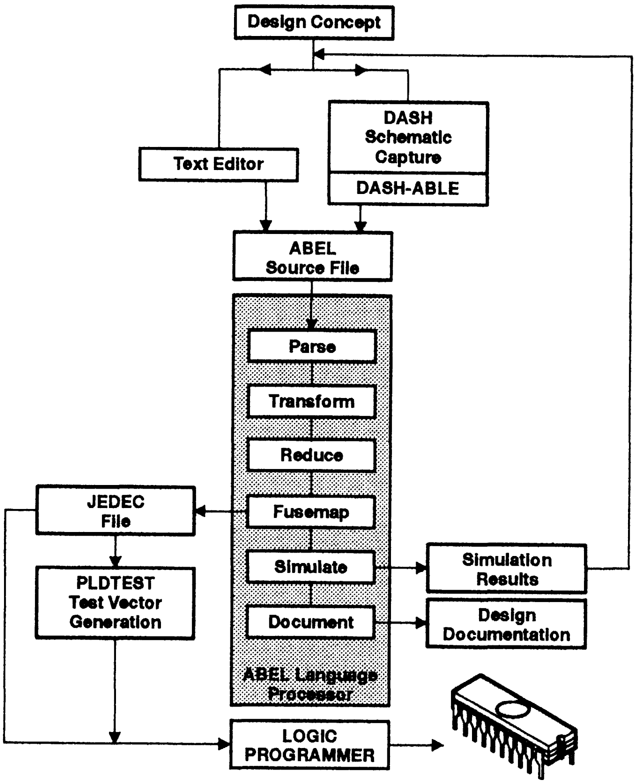
The logic design process using ABEL is shown in Figure 1. Beginning with the design concept, the designer creates the ABEL source file required by the language processor in order for it to generate the programmer load file. With the help of a text editor, the designer can create the source file which contains complete description of the logic design. The source file may also be created using DASH-ABEL to convert a DASH-generated schematic of a design.

Logic Design Steps:

The source file is presented to the language processor which performs several functions to produce a programmer load file (in JEDEC) format and the required design documentation (see Figure 1).

PARSE	Checks the syntax of the source file and flags any errors.
TRANSFORM	Converts the logic description to an intermediate form.
REDUCE	Performs logic reduction.
FUSEMAP	Creates the (JEDEC) programmer load file, which can then be downloaded to the logic programmer to program parts, or used to generate test vectors.
DOCUMENT	Generates a listing of the source file, a drawing of the logic device pin assignments, and a listing of the programmer load file.

Figure 1. Logic Design Steps with ABEL



Design Examples

The following design examples highlight two design entry methods, Boolean equations and State Diagrams.

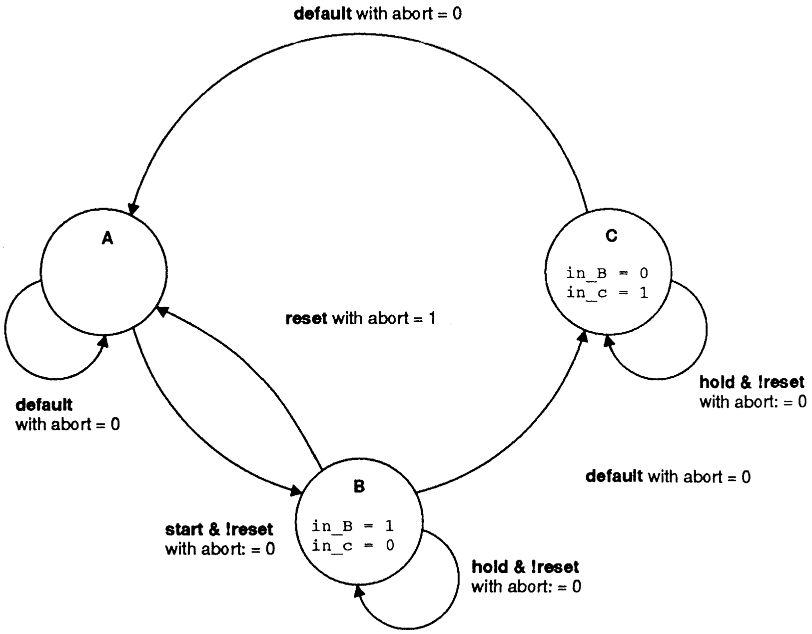
Three-State Sequencer

The following design is a simple sequencer which demonstrates the use of ABEL state diagrams. The design is implemented in a TIBPAL16R4-10 device (P16R4). There is no limit to the number of states that can be processed by ABEL, but the number of transitions and the path of the transitions is limited.

Figure 2 shows the sequencer design, with a bubble diagram showing the transitions and the desired outputs. The state machine starts in state A and remains in that state until the `start` input becomes high. It then transitions from state A to state B, from state B to state C, and back to state A. It remains in state A until the `start` input is high again. If the `reset` input is high, the state machine returns to state A at the next clock cycle. If this reset to state A occurs during state B, an `abort` synchronous output goes high, and remains high until the machine is again started.

During states B and C, asynchronous outputs `in_B` and `in_C` become high to indicate the current state. Activation of the `hold` input will cause the machine to hold in state B or C until `hold` is no longer high or `reset` becomes high.

Figure 2. State Machine Bubble Diagram



Design Methodology

The sequencer is described by using a `state_diagram` section in the ABEL source file. The ABEL source file for the sequencer is shown in Figure 3. In this example, the design is given a title, the target device is specified, and pin declarations are made. The `flag` statement is used to select the level of reduction required. Constants are declared to simplify the state diagram notation. The two state registers are grouped into a set called `sreg`. The three states A, B, and C are declared with appropriate values specified for each.

For larger state machines with more state bits, careful numbering of states can dramatically reduce the logic required to implement the design. Using constant declarations to specify state values saves time when later changes to these values are made.

The state diagram begins with the `state_diagram` statement that names the set of signals to be used for the state register. The set to be used is `sreg`.

Within the `state_diagram`, `IF-THEN-ELSE` statements are used to indicate the transitions between states, and the input conditions that cause each transition. In addition, equations are written in each state that indicate the outputs required for each state or transition.

For example, state A reads:

```
State A:
  in_B = 0;
  in_C = 0;
  if (start & !reset) than B with abort := 0;
  else A with abort := 0;
```

This means that if the machine is in state A and `start` is high, but `reset` is low, then the machine will advance to state B, but in another input condition the machine will remain in state A.

The equations for `in_B` and `in_C` indicate that those outputs should remain low while the machine is in state A, while the equations for `abort`, specified with the `with` keyword, indicate that `abort` should go low if the machine transitions to state B, but should remain at its previous value if the machine stays in state A.

Test Vectors

The specification of the test vectors for this design is similar to those of other synchronous designs. The first vector puts the machine into a known state (state A), and the following vectors exercise the functions of the machine. The A, B, and C constants are used in the vectors to indicate the value of the current state, thus improving the readability of the vectors.

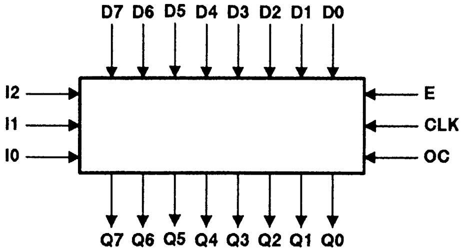
Figure 3. The ABEL Source File for Sequencer

```
title '8-bit barrel shifter
Gerrit Barrere    Data I/O Corp  Redmond WA        17 Oct 1987'
module sequence        flag '-r3'
title 'State machine example             D. B. Pellerin - Data I/O';
           dl          device        'p16r4';
           q1,q0                                  pin          14,15;
           clock,enab,start,hold,reset            pin          1,11,4,2,3;
           abort                                  pin          17;
           in_B,in_C                              pin          12,13;
           sreg                                      =         [q1,q0];
       "State Values ...
           A = 0;                    B = 1;                    C = 2;
state_diagram sreg;
           State A:                  " Hold in state A until start is active,
             in_B = 0;
             in_C = 0;
             IF (start & !reset) THEN B WITH abort := 0;
             ELSE A WITH abort := abort;
           State B:               " Advance to state C unless reset is active
             in_B = 1;            " or hold is active. Turn on abort indicator
             in_C = 0;            " if reset.
             IF (reset) THEN A WITH abort := 1;
             ELSE IF (hold) THEN B WITH abort := 0;
             ELSE C WITH abort := 0;
           State C:               " Go back to A unless hold is active
             in_B = 0;            " Reset overrides hold.
             in_C = 1;
             IF (hold & !reset) THEN C WITH abort := 0;
             ELSE A WITH abort := 0;
   [q0, q1] = !RESET
test_vectors([clock,enab,start,reset,hold]->[sreg.abort,in_B,in_C])
             [ .c. ,  0 ,  0  ,  0  ,  0 ]->[   A ,  0  ,  0 ,  0 ];
             [ .c. ,  0 ,  0  ,  0  ,  0 ]->[   A ,  0  ,  0 ,  0 ];
             [ .c. ,  0 ,  1  ,  0  ,  0 ]->[   B ,  0  ,  1 ,  0 ];
             [ .c. ,  0 ,  0  ,  0  ,  0 ]->[   C ,  0  ,  0 ,  1 ];

             [ .c. ,  0 ,  1  ,  0  ,  0 ]->[   A ,  0  ,  0 ,  0 ];
             [ .c. ,  0 ,  1  ,  0  ,  0 ]->[   B ,  0  ,  1 ,  0 ];
             [ .c. ,  0 ,  0  ,  1  ,  0 ]->[   A ,  1  ,  0 ,  0 ];
             [ .c. ,  0 ,  0  ,  0  ,  0 ]->[   A ,  1  ,  0 ,  0 ];

             [ .c. ,  0 ,  1  ,  0  ,  0 ]->[   B ,  0  ,  1 ,  0 ];
             [ .c. ,  0 ,  0  ,  0  ,  1 ]->[   B ,  0  ,  1 ,  0 ];
             [ .c. ,  0 ,  0  ,  0  ,  1 ]->[   B ,  0  ,  1 ,  0 ];
             [ .c. ,  0 ,  0  ,  0  ,  0 ]->[   C ,  0  ,  0 ,  1 ];
end
```

8-Bit Barrel Shifter

This design example highlights the use of Boolean equations as design entry format using ABEL. It is an 8-bit barrel shifter that includes a shift amount selector, an output control, and a device enable. The target device for this design is the TIBPAL20R8-XX. This design is described by only one Boolean equation. Figure 4 shows a block diagram of the design.

Figure 4. Block Diagram: 8-Bit Barrel Shifter



Design Specification

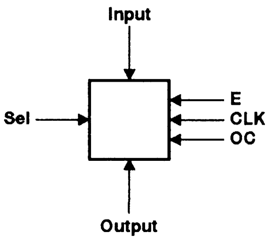
As shown in the block diagram above, the barrel shifter has 8 inputs (D0-D7), eight outputs (Q0-Q7), three select lines (I0-I2), a clock (CLK), an output control (OC), and an enable (E). On each clock pulse when E is high, the outputs show the inputs shifted by n bits to the right, where n is specified by the select lines. The bit shifted out of the barrel shifter on the right is shifted in on the left, actually performing a rotate. When E is low, the shifter outputs are then preset to 1.

The output control, when high, sets all outputs to high impedance, without affecting the shift. This means that if a shift is selected while the output control is high, the shift still occurs, but it is not seen at the outputs. If the OC is then set low, the shifted data will appear on the outputs.

Design Methodology

Figures 5 and 6 show a simplified block diagram and the source file listing of the design respectively. Pins have been assigned so that the shifter outputs can be associated with the registered outputs of the targeted PLD. The inputs, outputs, and select lines are then assigned to sets which simplify notation.

Figure 5. Simplified Block Diagram: 8-Bit Barrel Shifter



One Boolean equation is used to describe the entire function of the barrel shifter. The equation is expressed in the sum of products form and assigns a value to the output set. Each product in the equation corresponds to one of the possible shifts and defines the outputs for that shift.

Thus, the product term,

```
(Sel==0) & ![D7,D6,D5,D4,D3,D2,D1,D0]
```

defines that for a shift of 0, the inputs are transferred without a shift directly to the outputs. Similarly, the product term,

```
(Sel==5) & ![D4,D3,D2,D1,D0,D7,D6,D5]
```

defines that for a shift of 5, output Q7 gets the value of input D4, Q6 gets D3 and so on, corresponding to the correct shift of five places. Notice that the low-order input bits have been wrapped around, shifted out of the right side and into the left side.

`Sel` can have only one value at a time, thus only one of the `Sel ==` relational statements can be true at a given time, and only one of the product terms contributes to the sum of products. The OR of all the product terms is ANDed with the enable E so that when E is low, all the outputs are preset to 1.

Both the output sets on the left side of the equation and the inputs on the right side of the equation are expressed as negative logic, which, in effect, gives active high logic. This is done to compensate for the 'PAL20R8s inverted outputs. The inverse of the inputs is available on the device.

Figure 6. ABEL Source File for the 8-Bit Barrel Shifter

```
module     barrel
title '8-bit barrel shifter
Gerrit Barrere    Data I/O Corp  Redmond WA        17 Oct 1987'
           P7095       device    'P20R8';

           D7,D6,D5,D4,D3,D2,D1,D0                Pin 2,3,4,5,6,7,8,9;
           Q7,Q6,Q5,Q4,Q3,Q2,Q1,Q0                Pin 15,16,17,18,19,20,21,22;
           Clk,OC,E,I2,I1,I0                      Pin 1,13,23,10,11,14;

           Input                     = [D7,D6,D5,D4,D3,D2,D1,D0];
           output                    = [Q7,Q6,Q5,Q4,Q3,Q2,Q1,Q0];
           Sel                       = [I2,I1,I0];
           H,L,C,Z                   = 1,0,.C.,.Z.;
equations
           !Output := E & (  (Sel == 0) & ![D7,D6,D5,D4,D3,D2,D1,D0]
                                  # (Sel == 1) & ![D0,D7,D6,D5,D4,D3,D2,D1]
                                  # (Sel == 2) & ![D1,D0,D7,D6,D5,D4,D3,D2]
                                  # (Sel == 3) & ![D2,D1,D0,D7,D6,D5,D4,D3]
                                  # (Sel == 4) & ![D3,D2,D1,D0,D7,D6,D5,D4]
                                  # (Sel == 5) & ![D4,D3,D2,D1,D0,D7,D6,D5]
                                  # (Sel == 6) & ![D5,D4,D3,D2,D1,D0,D7,D6]
                                  # (Sel == 7) & ![D6,D5,D4,D3,D2,D1,D0,D7]) ;
 test_vectors
            ([Clk,OC, E, Sel,   Input]    ->    output)
             [ C,  L, H,  0, ^b10000000]  -> ^b10000000; ″ Shift   0
             [ C,  L, H,  1, ^b10000000]  -> ^b01000000; ″ Shift   1
             [ C,  L, H,  2, ^b10000000]  -> ^b00100000; ″ Shift   2
             [ C,  L, H,  3, ^b10000000]  -> ^b00010000; ″ Shift   3
             [ C,  L, H,  4, ^b10000000)  -> ^b00001000; ″ Shift   4
             [ C,  L, H,  5, ^b10000000]  -> ^b00000100; ″ Shift   5
             [ C,  L, H,  6, ^b10000000]  -> ^b00000010: ″ Shift   6
             [ C,  L, H,  7, ^b10000000]  -> ^b00000001; ″ Shift   7

             [ C,  L, H,  0, ^b01111111]  -> ^b01111111; ″ Shift   0
             [ C,  L, H,  1, ^b01111111]  -> ^b10111111; ″ Shift   1
             [ C,  L, H,  3, ^b01111111]  -> ^b11101111; ″ Shift   3
             [ C,  L, H,  7, ^b01111111]  -> ^b11111110; ″ Shift   7

             [ C,  L, H,  1, ^b00000001]  -> ^b10000000; ″ Shift   1/Wrap
             [ C,  L, H,  1, ^b11111110]  -> ^b01111111; ″ Shift   1/Wrap
             [ C,  L, L,  0, ^b00000000]  -> ^b11111111: ″ Preset
             [ C,  H, H,  0, ^b00000000]  ->      Z;     ″ Test High Z

end
```

Other PLD Design Software Products

Below is a short list of some of the popular PLD design software products available to logic designers. They are all PC based and can be installed on your IBM PC™ or compatible.

CUPL™ — by Logical Devices Inc.

PLDesigner™ — by MINC Inc.

proLogic™ — by proLogic Systems Inc.

CUPL

CUPL, like ABEL, is a universal Computer Aided Design (CAD) tool that supports PLDs. It has utility files that facilitate conversion of designs done in other design software environment to the CUPL design environment. CUPL also produces a standard programmer load file in JEDEC format, thus making it compatible with logic programmers that accept JEDEC files.

Features of CUPL design language:

☐ Flexible Forms for Design Description

  Boolean Equations
  Truth Tables
  State Diagrams

☐ Expression Substitutions or Time Saving Macros

  This involves the assignment of names to equations and having the software do the substitution any time the assigned name is encountered during the compile process.

☐ Shorthand Features Offered by CUPL

  List Notation; This nested directive

```
[A4,A3,A2,A1,A0]
```

  can be represented as

```
[A4..0]
```

  Bit Fields; A group of bits may be assigned to a name as in

```
FIELD ADDR = [A4..01]
```

  Also available in CUPL are the use of Distributive property
  where

```
A & (B # C)
```

  is replaced with

```
A & B # A & C
```

  DeMorgans Theorem
  where

```
(A & B)
```

  is replaced with

```
!A # !B
```

Some Features of the CUPL Language Processor:

CUPL provides design templates which allow designers to just fill-in-the-blanks when originating a design. Free form comments can also be used throughout the design.

Error checking with detailed error messages directs designers to the source of problems during debugging.

Logic Reduction Capabilities available on CUPL offers a choice of several minimization levels from just fitting a design into a target device to the absolute minimum.

Design Simulation is accomplished using the CSIM feature. This feature allows designers to check the workability of their designs before a part is programmed. Functional simulation can be done at the programmer when test vectors are provided.

PLDesigner

The PLDesigner is a universal logic design synthesis tool for designing with PLDs. It features:

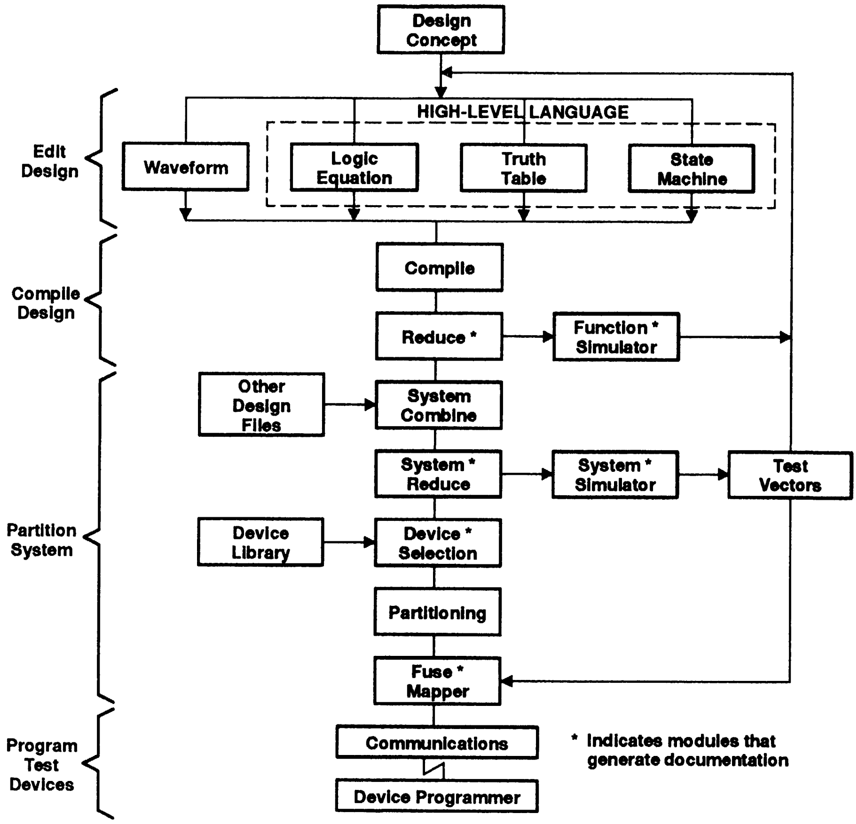
- ❏ A High-Level Behavioral Language
- ❏ Algorithmic Design Entry for State Machine Designs
- ❏ Waveform Design Entry for Glue Logic
- ❏ Design Simulation With Automatic Test Vector Generation
- ❏ Automatic Device Selection and Design Partitioning Across Multiple Device Architectures
- ❏ A Device Library of Over 2,000 Devices.

A fundamental difference between PLDesigner and other products is that the design phase is separate from the device selection phase. You can complete a design before a device, or devices, are selected. This allows you to concentrate on design and simulation. No longer is it necessary to limit your design to a single device, or to select a device before starting the design.

System Requirements

PLDesigner operates on an IBM PC or compatible with an MS-DOS™ or PC-DOS™ operating system, Version 2.0 or later. A hard disk and 640K RAM memory are recommended. A CGA, EGA, Hercules, or monochrome display may be used. A mouse and printer are optional.

Figure 7. Logic design Steps with PLDesigner



proLogic

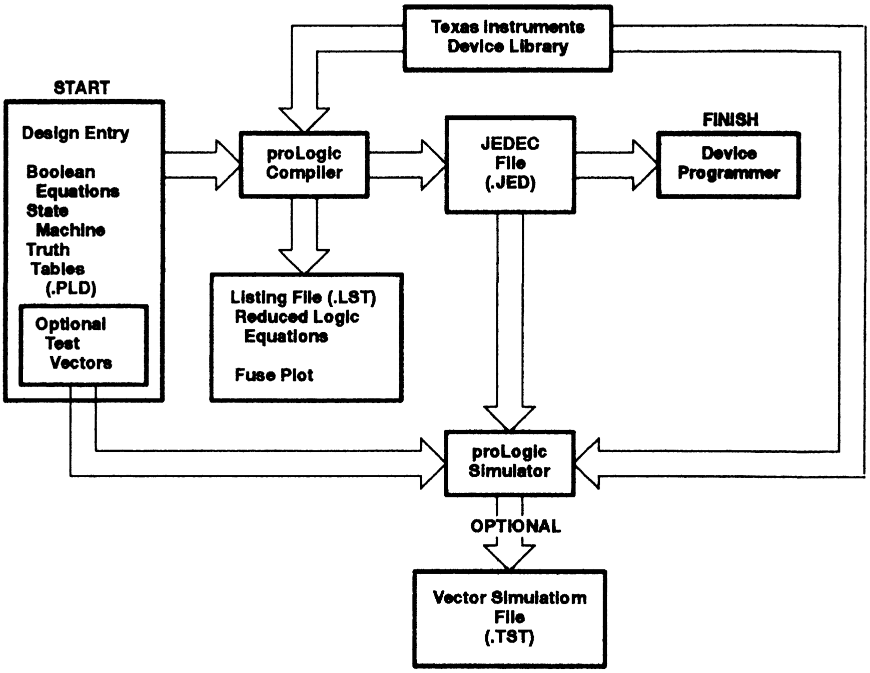
ProLogic is a logic design software tool from Texas Instruments used to design and program PLDs. This design software development package quickly converts your logic design to a programmer load file in the standard JEDEC format. prologic has the flexibility to allow you to describe the logic design in any of the following formats:

- ☐ Boolean Equations
- ☐ Truth Table
- ☐ State Diagrams

It should be noted here that, not only can a design be entered in any of the above methods, you can design various sections of the design in any of the three formats shown above, and proLogic has the ability to unify the various sections and process them as one design.

The proLogic compiler is capable of performing functional simulation when test vectors are provided. The simulator uses the fuse list portion from the JEDEC file to create a functional device model. It can then execute the simulation vectors against this model. The results are automatically placed in a file for evaluation.

Figure 8. PLD Design Flow using proLogic Design Software



Programming Texas Instruments Programmable Logic Devices

TEXAS INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to current specifications in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Please be aware that TI products are not intended for use in life-support appliances, devices, or systems. Use of TI product in such applications requires the written approval of the appropriate TI officer. Certain applications using semiconductor devices may involve potential risks of personal injury, property damage, or loss of life. In order to minimize these risks, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards. Inclusion of TI products in such applications is understood to be fully at the risk of the customer using TI devices or systems.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Copyright © 1992, Texas Instruments Incorporated

Programming Texas Instruments Programmable Logic Devices

This report is intended to introduce the user to the fuse technologies used in Texas Instruments (TI) Programmable Logic Devices (PLDs), the measures taken by TI to provide devices with the highest possible programming yields, and the steps users can take to ensure good programmability.

How a Fuse Is Programmed

Programming Algorithm

Each programmable logic device family requires a unique algorithm for fuse programming and verification on commercial programming equipment. The algorithm is a combination of voltage and timing required for addressing and programming fuses in the user array.

The PLD's programming circuitry is enabled by pulsing one or more pins to a super voltage level (10.5 volts). Once the programming circuitry is enabled, inputs become addressing nodes for the input and product lines within the PLD. The actual fuse link is at the intersection of the input and product lines. Once the fuse is addressed, the fuse can be programmed by pulsing the output associated with the location of the fuse link. A fuse can be verified to be programmed by enabling the programming circuitry, supplying the fuse address to the device's inputs, and reading the level of the device's output.

Bipolar Fuse Technology

Figure 1 shows a top and side view of a fuse in a bipolar PLD before it is programmed. Titanium-Tungsten (TiW) is used for the fuse or metal link programming element. The ideal thickness for this programming element is about 500 angstroms. Titanium-tungsten is also used as a barrier metal over contacts to prevent direct aluminum contact to silicon. To prevent aluminum diffusion during high-temperature processing, the ideal thickness of the barrier metal is about 2000 Angstroms. TI's two-step link process allows both the barrier thickness and the fuse thickness to be at the ideal. The net result is a higher reliability and better programming yields.

When a device is programmed, the fuse location is selected. The fuse element at the selected location is then opened by the programmer passing a current through the titanium-tungsten fuse element that violates the current density limit for the element. This current flow heats the fuse element to approximately 2,100°C at which point the element is in a molten state. The metal migration which results from the heat of this out-of-limit current stress causes a gap in the fuse element.

As shown in Figure 2, the high temperature at the fuse element's gap causes two actions to occur. The fuse element's TiW material oxidizes so as to leave the metal on both sides of the gap non-conductive. Also, the heat associated with programming, causes the Silicon Dioxide (SiO_2) above the fusing element to flow into the gap. This proven fuse technology has eliminated the fears of fuse grow back as a failure mechanism in PLDs.

Figure 1. Before Programming

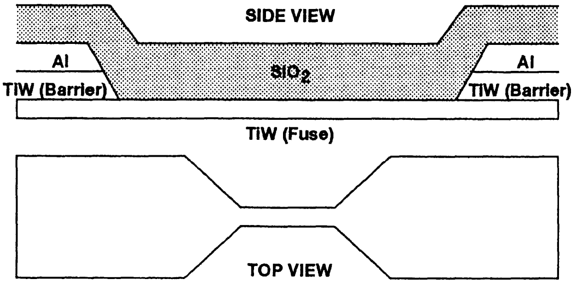
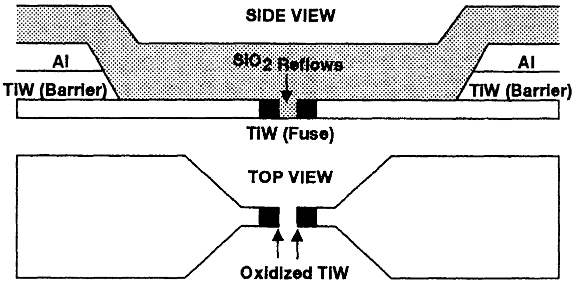


Figure 2. After Programming



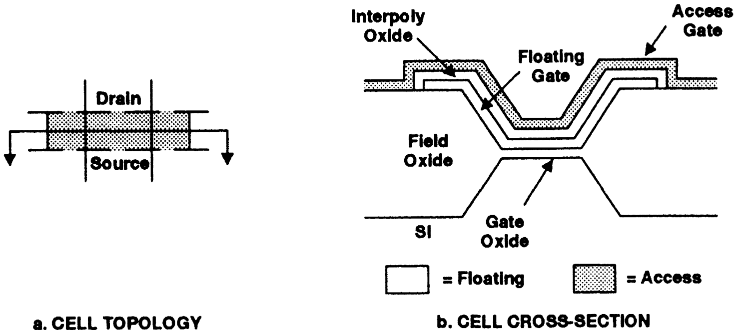
EPLD Programming Technology

Texas Instruments CMOS PLDs employ a process technology similar to EPROM devices. When compared to the bipolar fusible link technology, the FAMOS (Floating-gate, Avalanche-Injection MOS) transistor used by EPROMs replaces the fusible link. This permits the programmability function in the same way as the fuse.

The FAMOS transistor resembles an ordinary MOS transistor except for the addition of a floating gate buried in the insulator between the substrate and the ordinary select-gate electrode as shown in Figure 3. The programming of the FAMOS structure is performed by capacitively coupling the select gate in series with the floating gate. Hot electron injection onto the floating gate occurs by pulling the select gate to the programming voltage and the drain of the FAMOS transistor to the programming voltage minus several threshold drops. As shown in Figure 4, this serves to alter the threshold voltage of the select gate.

Once programmed, the FAMOS transistor retains the electron charge or data pattern, until exposed to an integrated dose of ultraviolet light with a wavelength of 2,537 angstroms. This uv light will erase the charge by giving the electrons enough energy to scatter from the floating gate. This returns the threshold voltage of the select gate back to its original value or unprogrammed state. After erasure, the device is ready for reprogramming. The reprogrammablity feature of Erasable PLDs allows the devices to be used for many programming iterations which are often required in the user's design and prototype stages.

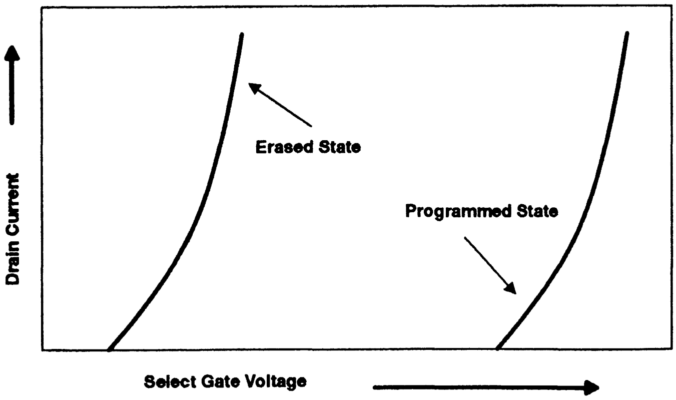
Figure 3. Views of an Floating Gate EPROM Cell



a. CELL TOPOLOGY

b. CELL CROSS-SECTION

Figure 4. Drain Current verses Gate Voltage



The threshold voltage determines whether it is sensed as the nonconducting programmed state or erased. The charge in threshold corresponds to the shift down in the select-gate voltage to drain current transfer characteristic.

Programmer Approval

Programming Algorithm Specifications

In order to achieve satisfactory programming yields for PLDs, it is critical that device programmers adhere to the programming algorithm specifications as defined by Texas Instruments. Each specification contains detailed step-by-step programming procedures, input and product line addressing procedures, waveform diagrams, and minimum and maximum voltage and timing tables. Because of the complexity of the programming algorithms and the need to control and update the specifications, Texas Instruments maintains programming algorithms in a specification system separate from the PLD Data Book.

TI currently sends specifications and specification updates to most programmer and software manufacturers, and challenges each to work with TI to provide our mutual customer with approved programming support to guarantee them with the best possible programming yield.

Texas Instruments reserves the right to approve programming algorithms contained in commercial programming equipment, and recommends that customers only use approved programming support.

Approved programming support means that TI has evaluated the programming algorithm, has verified critical timing paths and voltage levels, and has performed yield analysis testing. Approvals are granted by device and are thoroughly documented.

These measures are taken to ensure that TI's customers receive the best possible programming yields when using TI PLDs.

Evaluation and Approval Methods

Programmers are evaluated by TI's programmable logic applications. The evaluation includes the following:

- ☐ Measure Voltage Levels for Accuracy and Repeatability
- ☐ Measure Critical Timing Paths
- ☐ Evaluate System Power Supply and Grounding
- ☐ Yield Analysis

Templates and oscilloscope printouts are used to document all measurements and are maintained permanently on file. Approvals are granted by device or algorithm and documented by letter to the programmer manufacturer.

Approved Programmer Support

Approved programmer support is documented in the *TI Programming Reference Guide*, and on the TI PLD Bulletin Board (214) 997-5665. To subscribe to the Programming Reference Guide, simply contact the TI PLD Hotline (214) 997-5666 or your local TI field sales representative.

Texas Instruments recommends that customers use only approved programming support. Approved programming support ensures the user..

- ☐ The best possible programming yield is being achieved because the programming algorithms were evaluated and closely scrutinized.
- ☐ TI guarantees 100% programming yield if approved programmers are used, any fallout can be returned for full credit.
- ☐ TI applications engineers are available to interface with programmer manufacturers for you on any programming issues or concerns.

Helpful Hints for Good Programmability

1) Follow accepted standards for ESD protection — remember the additional handling requirements in customizing PLDs make them more susceptible to ESD damage.

   Equipment, personnel and work surfaces should be grounded

   Air ionization is recommended when handling static sensitive devices outside of protective containers.

2) Misaligned connectors and worn sockets can contribute to poor programming yield. Be aware of the manufacturers specification for number of insertions and be sure sockets are replaced frequently to ensure proper contact.

3) Ensure you are using the latest update. Most programmer manufacturers offer update and repair services to their users. The cost of the service is typically not much more than the cost of a single update and the manufacturer may update four or more times per year. TI recommends the user subscribe to this service.

   Revisions could improve yield. TI continuously works with programmer manufacturers on yield improvement.

   New devices may be supported.

4) Programming equipment should be calibrated. Calibration is typically included with the update and repair services previously discussed. TI recommends no less than two calibrations per year.

   Highest possible yields

   Avoid device damage

5) Verify the correct family pinout codes or device entry codes are being used. It is important to understand that different algorithms may be needed for different speed versions of the same function.

6) Use only TI evaluated and approved programming equipment to ensure the highest possible programming yield and quality level.

Test Considerations for PLDs

TEXAS INSTRUMENTS

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to current specifications in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Please be aware that TI products are not intended for use in life-support appliances, devices, or systems. Use of TI product in such applications requires the written approval of the appropriate TI officer. Certain applications using semiconductor devices may involve potential risks of personal injury, property damage, or loss of life. In order to minimize these risks, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards. Inclusion of TI products in such applications is understood to be fully at the risk of the customer using TI devices or systems.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Copyright © 1992, Texas Instruments Incorporated

TRADEMARKS

Logic Fingerprint is a trademark of Data I/O Corporation.

IMPACT is a trademark of Texas Instruments Incorporated.

Test Considerations for PLDs

Programmable Logic Device (PLD) architecture establishes some unique characteristics. Because PLDs do not have the functional needs for address pins as found in a PROM, the array must be addressed for programming through the use of super voltages (10. 5 volts). Since the programming and verification circuitry are not the same as the functional circuitry, verification of the array fuses does not ensure total functionality. For this reason, there are two customer yield points to be considered for a PLD, 1) programmability yield, and 2) functionality after programming. Texas Instruments (TI) thoroughly tests PLDs in its factory; however, many users find the need to test after programming to achieve the highest quality levels.

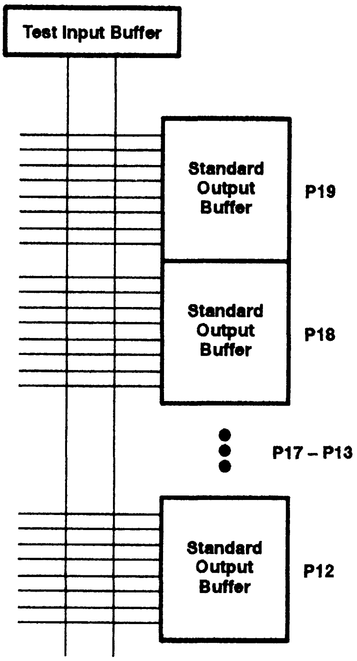
The objective of this report is to provide the PLD user with an insight as to what kind of testing is performed at TI prior to shipment of programmable logic devices, and to assist you in the evaluation of your testing alternatives after programming.

Designed-In Factory Testability

Texas Instruments has designed testability into its bipolar PLDs through the addition of test input and test product lines. Utilizing the same circuitry as the main array fuses, a test pattern is programmed into the test array fuses which address and program at least one fuse in each input and product line. In addition to verification of the main fuse array, the test lines provide a further programmability checkpoint for each device. These same test lines enable TI to perform functional, static (dc), and dynamic (ac) parametric testing on every packaged device.

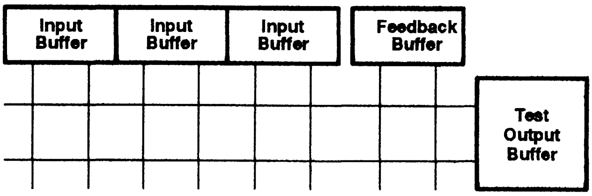
Figures 1 and 2 are simplified diagrams of the test circuitry for the TIBPAL16XX series devices. Note that the test lines allow testing of actual input and output circuitry; therefore, all guaranteed specifications can be tested. Dynamic testing through the test circuitry is closely correlated to worst case paths and should eliminate the need for ac testing at the customers incoming inspection.

Figure 1. *Additional Input lines*



By using the test input lines, all outputs may be toggled and the speed can be checked from one input to all outputs.

Figure 2. *Additional Product Lines*



By using the test product lines TI can check every input and implement dynamic test from every input to one output.

User Testability Features

In addition to the designed-in testability features used in factory testing, features were also added to simplify user testability. Table 1 lists user testability features offered on TI programmable logic devices and associated software products available to assist the user with testing PLDs.

Register Preload

This feature allows the user to preload the output registers to known states prior to applying data at inputs and/or I/Os and clocking.

Preload can be implemented by writing preload vectors in more popular logic compilers following logic equations or can be automatically generated by using automatic vector generation software. Most commercial programmers used for functional test support the use of preload vectors.

The real advantage of register preload is that it allows the user to fully test the more complex codes.

Power-Up Clear, Set or Reset

Power-up clear, set, or reset enables the user to know the state of the register at power up. Again, this is a key feature for testability as it allows the user writing test vectors or the automatic vector generation software with a starting point for register intensive designs. Table 1 shows the power-up state of the register and resulting state at the output.

The user can also contribute to the testability of the design by utilizing other features of the PLD.

Unused Inputs / Product Lines

Unused inputs and product lines can be used to implement set, reset, clear, etc... functions to register intensive designs which are often hard to test. Often register designs have unused input pins, as well as product lines available for implementing these functions.

Enable on Combinational Outputs

Combinational outputs have one product line available for implementing the enable/disable function. The key advantage can be seen during board testing where devices need to be isolated from each other. By disabling the output of the PLD, the user can force input conditions from the external source to the devices being driven by the PLD.

Table 1. User Testability Features

						VECTOR GENERATION SOFTWARE SUPPORT	
DEVICE FAMILY	**SPEED DESIGNATOR**	**REGISTERED PRELOAD**	**REGISTERED OUTPUTS**	**POWER-UP AT REGISTER**	**POWER-UP AT OUTPUT**	**AVIL ATG**	**DATA I/O PLDTEST+**
TIBPAL16L8	-5/-7/-10	NA	0	NA	NA	2.23	1.0
TIBPAL16R4	-5/-7/-10	YES	4	L	H	2.23	1.0
TIBPAL16R6	-5/-7/-10	YES	6	L	H	2.23	1.0
TIBPAL16R8	-5/-7/-10	YES	8	L	H	2.23	1.0
TIBPAL16L8	-15/-25	NA	0	NA	NA	2.23	1.0
TIBPAL16R4	-15/-25	–	4	H	L	2.23	1.0
TIBPAL16R6	-15/-25	–	6	H	L	2.23	1.0
TIBPAL16R8	-15/-25	–	8	H	L	2.23	1.0
TIBPAL20L8	-5/-7/-10	NA	0	NA	NA	2.23	1.0
TIBPAL20R4	-5/-7/-10	YES	4	L	H	2.23	1.0
TIBPAL20R6	-5/-7/-10	YES	6	L	H	2.23	1.0
TIBPAL20R8	-5/-7/-10	YES	8	L	H	2.23	1.0
TIBPAL20L8	-15/-25	NA	0	NA	NA	2.23	1.0
TIBPAL20R4	-15/-25	YES	4	L	H	2.23	1.0
TIBPAL20R6	-15/-25	YES	6	L	H	2.23	1.0
TIBPAL20R8	-15/-25	YES	8	L	H	2.23	1.0
TIBPAL22V10	/A	YES	10*	L	H/L	2.23	1.0
TIBPAL22V10	-5	YES	10*	L	H/L	–	–
TIBPAL22V10	-7/-10	YES	10*	L	H/L	2.23	1.0
TIBPAL22V10	-15B	YES	10*	L	H/L	2.23	1.0
TIBPAL22VP10	-20	YES	10*	L	H/L	2.23	–
TICPAL16L8	-55	NA	0	NA	NA	2.23	1.0
TICPAL16R4	-55	YES	4	NA	NA	2.23	1.0
TICPAL16R6	-55	YES	6	NA	NA	2.23	1.0
TICPAL16R8	-55	YES	8	NA	NA	2.23	1.0
TICPAL22V10Z	-25/-30	YES	10*	–	–	2.23	1.0
TIB82S105	B	–	8	H	H	2.23	–
TIB82S167	B	–	6	H	H	2.23	–
TIBPLS506	–	–	8*	L	H	2.23	–
TIB82S167	–	–	8*	L	H	2.23	–
EP330	-12/-15/-25	–	8*	NA	NA	2.23	–
EP630	-15/-20/-25	–	16*	NA	NA	2.23	–
EP1830	-20/-25/-30	–	48*	NA	NA	2.23	–

* = User Configured
NA = Not Applicable
All CMOS PLDs are erasable for repeated programmability.

Pld Testing Options

Fuse Verification / Checksum

Checksum testing verifies array fuses to be intact or blown. Each fuse location is assigned a value of 1, 2, 4, 8, 16, 32, 64, or 128. The checksum is the sum (in hexadecimal) of the values of positions with blown fuses. As previously discussed, checksum testing or fuse verification only tests for the state of the fuse and exercises programming circuitry only. The functional circuitry is not tested.

Structured Vector Testing

Structured vector testing, utilizing the software packages shown in Table 1 or generated manually at design conception, allow the user to apply structured test vectors (see Figure 3) to the device either on device programmers or testers. Figure 4 shows how to implement preload into your vector test.

Fault coverage of structured vectors is graded and documented so the user knows how much coverage is used for the design. A fault is simply a potential for device failures. Faults graded include logic faults as well as fuse faults.

Logic Faults — Check affected gates for S-A-0, or stuck low, and S-A-1, or stuck high. Figure 5 Illustrates logic faults. Fuse Faults — Check each fuse for intact or blown.

Structured vectors are generic so they can be applied to all manufacturers PLDs of like function (e.g. 16L8, 22V10, etc ...). Structured vector testing ensures the functionality of the design, and can be performed on the device programmer. Structured vector testing should be considered the minimum amount of testing required prior to application.

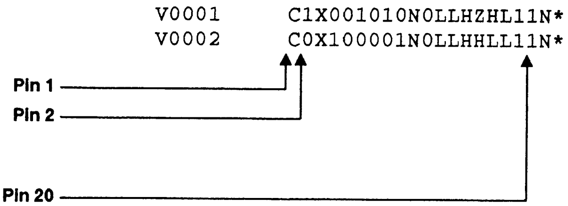
Signature Analysis / Logic Fingerprint™ / Random Vector Test

Signature analysis or fingerprint testing is sometimes seen as an alternative to structured vector testing. The test applies a predetermined or pseudo-random vector set to the inputs of a known good device and memorizes the output responses. Subsequent devices are tested against the master. Potential problems exist with this type of testing.

- Master device could be defective resulting in the acceptance of bad devices and/or rejection of good devices.
- Registered devices may never initialize
- Outputs may never be put in the correct states to ensure correct feedback (only structured vectors ensure correct feedback)
- Oscillating conditions not controlled (structured vectors can void oscillations)
- Different manufacturers use different power up / preload conditions
- Percent of coverage is unknown

The best case could yield an adequate functional test while the worst case may test little or nothing.

Figure 3. *Test Vectors (standard JEDEC form)*

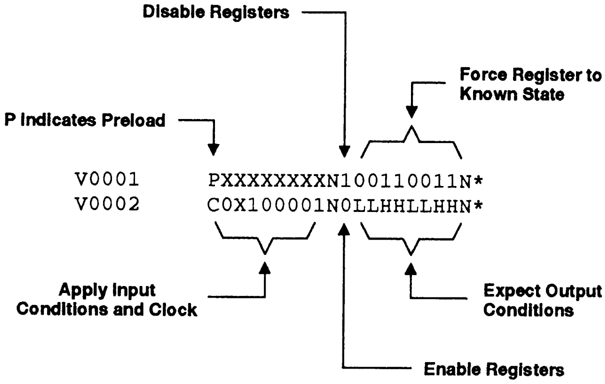


```
V0001     C1X001010N0LLHZHL11N*
V0002     C0X100001N0LLHHLL11N*
```

SYMBOLOGY

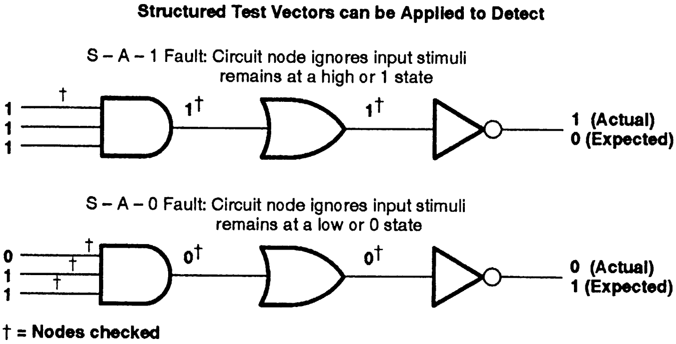
C = Clock
0 = Drive Low
1 = Drive High
N = No Connect
H = Expect High
L = Expect Low
Z = High-Impedance
X = Don't Care

Figure 4. *Preload Implementation — '16R8*



```
V0001     PXXXXXXXXN100110011N*
V0002     C0X100001N0LLHHLLHHN*
```

Figure 5. *Fault Grading*



Static (dc) Parametric Testing

Static parametric testing includes structured vector or functional testing as described previously plus the testing of critical current/voltage parameters to ensure they meet the specifications prescribed by the TI data book.

The testing of dc parametrics, such as input and I/O leakage currents, output high and low voltages under static loading, power supply current, etc... will only improve the quality of the PLD going into the application by ensuring that devices which are functional were not damaged due to ESD (electrostatic discharge) or EOS (electrical overstress) during the customization process.

Static parametric testing can not presently be performed on device programmers and therefore requires the use of automatic test equipment (ATE). Static parametric testing coupled with structured vector testing should provide the user an optimum test with a medium investment.

Dynamic (ac) Testing

Dynamic testing ensures that the PLD meets all the speed requirements of the design. A good ac test measures propagation delay time through all possible paths and, when coupled with functional and dc parametric testing, provides the ultimate PLD test.

There are two types of ac testing to be considered: functional ac and measurement ac testing. Functional ac testing becomes a popular test method for PLDs. This method applies structured test vectors and sets strobes to ensure transitions occur with proper timing. Functional ac testing performs a good job of simulating the actual design if structured vectors with good coverage are used.

In contrast, measurement ac testing tests and measures all speed parameters utilizing all possible input and output combinations. This type of testing is typically only available from the factory as it requires another level of vector grading and dedicated engineering resources.

Dynamic testing usually requires a large investment by the user in not only hardware, but also in engineering time in the development of extensive test programs, bench to tester correlation, load boards, vector software, etc...

Texas Instruments performs extensive worst case code characterization prior to device release. Each device shipped from TI undergoes ac testing using the device's test rows and test columns. Many users find post programming ac test does not justify the payback in terms of a higher level of quality.

Why Test After Programming?

As previously discussed, verification of the fuse array following programming does not ensure total functionality; therefore, the user must determine what amount of testing is required after programming. The following concerns should be considered.

Programming

Programming exposes the device to super voltages (up to 10.75 volts) and currents high enough to overstress devices. TI PLDs are designed to withstand these conditions, however, all leakage current parameters should be tested to eliminate the risk of electrical overstress.

An uncalibrated programmer can expose devices to voltages/currents outside specified ranges.

Handling

In addition to programming, most users designate their custom function which was programmed into the PLD through labeling or marking. The added handling required to program and customize the PLD increases the chances for ESD (electro-static discharge) damage unless strict adherence to ESD protection procedures is observed.

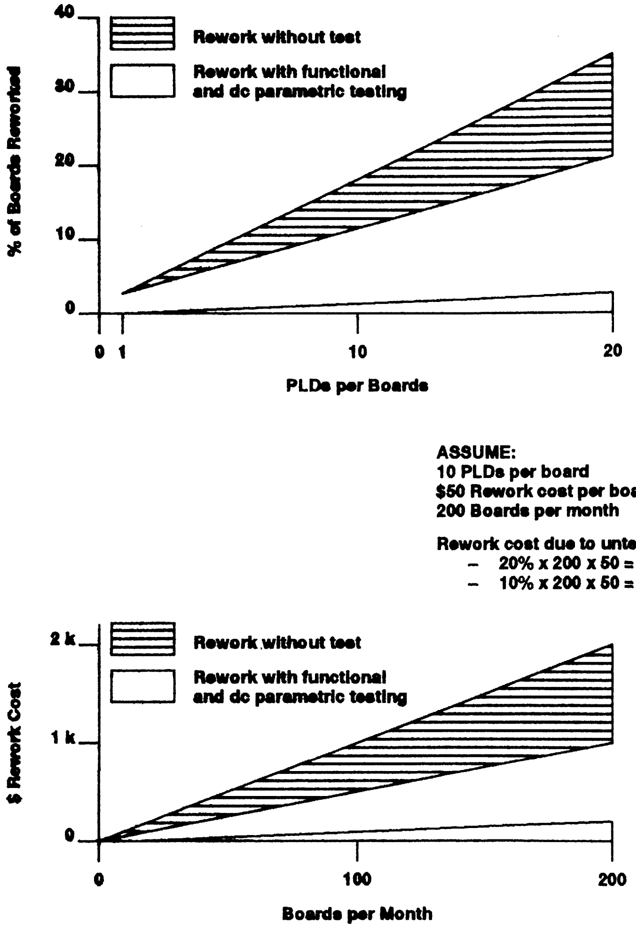
Custom Function

TI goes to extreme measures to ensure device functionality and performance, however, each user design is a custom function and should be treated as such during final testing prior to application.

Test vs Rework

Figure 6 compares the impact of testing on board rework and, consequently, manufacturing cost. This illustration compares no testing vs. functional and dc parametric testing. Using conservative figures for rework cost, the data shows rework cost due to untested PLDs can exceed one dollar per PLD used. A similar analysis of the user's application may show a cost savings which would result from testing after programming.

Figure 6. Test verses Rework



ASSUME:
10 PLDs per board
$50 Rework cost per board
200 Boards per month

Rework cost due to untested PLDs:
- **20% x 200 x 50 = $2000**
- **10% x 200 x 50 = $1000**

TI Programming And Test Services

What services are offered by your PLD manufacturer? Texas Instruments provides its customers with a three phase service program which provides for programmed and tested PLDs of the highest quality (see Figure 7) direct from the factory or through TI's authorized distributors.

Factory Programmed and Tested PLDs

TI has the capability to support run rates greater than 1 000 parts per code per month with factory programmed and tested PLDs. TI generates structured test vectors and performs 100% functional, dc parametric, and ac testing on PLDs programmed to your custom logic function. Custom symbolization is also included in the factory programmed PLD flow, thereby delivering ship-to-stock and/or ship-to-WIP product.

Impact Design and Services Centers

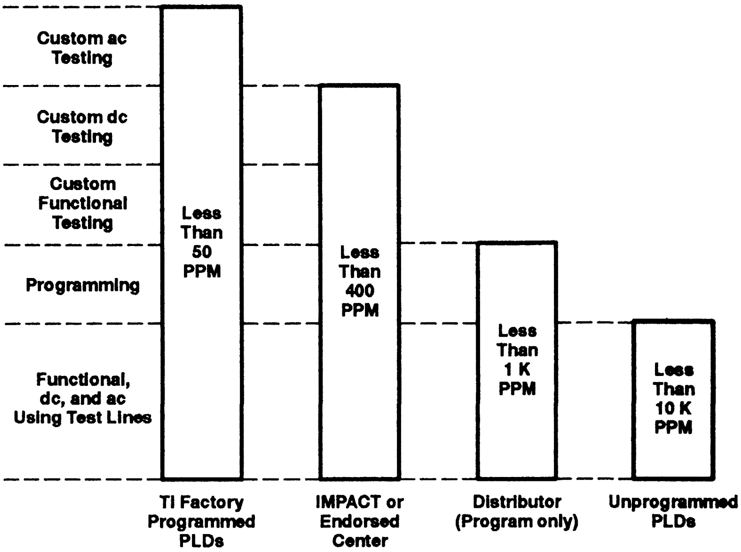
Texas Instruments took the leadership role in the provision of program and test services to its customers by implementing the Impact Center approach in 1986. The Impact Centers offer the customer a local quick turn production resource with factory quality programming, marking, and testing on TI owned and maintained equipment. Strict adherence to TI's ESD protection guidelines is maintained. Production specifications remain under TI control and operations are continuously audited by TI.

Endorsed Program and Test Centers

An extension of the Impact Center philosophy, an endorsed center is a distributor funded program and test facility which meets or exceeds TI specifications. Each center has the capability to program, mark, and test PLDs. Production flows are approved to guarantee the user receives devices of ship-to-stock quality. The centers are audited biannually to ensure compliance.

Tables 2 lists the TI Impact Centers. An updated listing for Endorsed Centers may be obtained through the TI PLD Bulletin Board (214) 997-5665, the TI PLD Hotline (214) 997-5666 or your local TI Sales Representative.

Figure 7. TI Programming Logic Services



TI Impact Design and Service Centers

Design and programming assistance is offered by Texas Instruments IMPACT™ Design and Service Centers. The centers are equipped with the latest in software and hardware tools for design, debugging, creating prototypes, and production on a local basis. Supported by a professional engineering staff, the centers provide complete code development, device programming, symbolization, functional and static (dc) parametric testing.

Anthem Electronics, Inc.
1160 Ridder Park Drive
San Jose, CA 95131
(408) 453-2200

Arrow/Schweber Electronics, Inc.
17822 Gillett Avenue
Irvine, CA 92714
(714) 587-0404

Arrow/Schweber Electronics, Inc.
4250 River Green Parkway
Suite E
Duluth, GA 30131
(404) 497-1300

Hall-Mark Electronics Corp.
1 Mauchly
Irvine, CA 92715
(714) 727-6000

Hall-Mark Electronics Corp.
6 Cook Street
Pinehurst Park
Billerica, MA 01821
(508) 667-0902

Anthem Electronics, Inc.
373 Inverness Drive South
Englewood, CO 80112
(303) 790-4500

Arrow/Schweber Electronics, Inc.
1180 Murphy Avenue
San Jose, CA 95131
(408) 441-9700

Arrow/Schweber Electronics, Inc.
665 Spice Island Drive
Sparks, NV 89431
(800) 777-Arrow

Hall-Mark Electronics Corp.
2105 Lundy Avenue
San Jose, CA 95131
(408) 432-4000

Hall-Mark Electronics Corp.
11420 Pagemill Road
Dallas, TX 75243
(214) 553-4300

TI Impact Design and Service Centers (Continued)

Marshall Industries
9320 Telestar
El Monte, CA 91731
(818) 307-6208

Marshall Industries
33 Upton Drive
Wilmington, MA 01887
(508) 658-0810

Wyle Electronics Marketing Group
5191 Oceanus
Huntington Beach, CA 92649
(714) 863-9953

Wyle Electronics Marketing Group
452 East 124th Avenue
Thornton, CO 80241
(303) 457-9953

Marshall Industries
336 Los Coches Street
Milpitas, CA 95035
(408) 942-4600

Marshall Industries
2045 Chenault Street
Carrollton, TX 75008
(214) 233-5200

Wyle Electronics Marketing Group
3000 Bowers Avenue
Santa Clara, CA 95051
(408) 727-2500

Wyle Electronics Marketing Group
1810 Greenville Avenue
Dallas, TX 75081
(214) 235-9953

Programmable Logic Devices
Qualification Data
1992

Texas Instruments

IMPORTANT NOTICE

Texas Instruments Incorporated (TI) reserves the right to make changes to its products or to discontinue any semiconductor product or service without notice, and advises its customers to obtain the latest version of relevant information to verify, before placing orders, that the information being relied on is current.

TI warrants performance of its semiconductor products and related software to current specifications in accordance with TI's standard warranty. Testing and other quality control techniques are utilized to the extent TI deems necessary to support this warranty. Specific testing of all parameters of each device is not necessarily performed, except those mandated by government requirements.

Please be aware that TI products are not intended for use in life-support appliances, devices, or systems. Use of TI product in such applications requires the written approval of the appropriate TI officer. Certain applications using semiconductor devices may involve potential risks of personal injury, property damage, or loss of life. In order to minimize these risks, adequate design and operating safeguards should be provided by the customer to minimize inherent or procedural hazards. Inclusion of TI products in such applications is understood to be fully at the risk of the customer using TI devices or systems.

TI assumes no liability for applications assistance, customer product design, software performance, or infringement of patents or services described herein. Nor does TI warrant or represent that any license, either express or implied, is granted under any patent right, copyright, mask work right, or other intellectual property right of TI covering or relating to any combination, machine, or process in which such semiconductor products or services might be or are used.

Copyright © 1992, Texas Instruments Incorporated

TRADEMARKS

PAL is a registered trademark of Advanced Micro Devices Inc.
IMPACT-X is a trademark of Texas Instruments Incorporated.
EPIC is a trademark of Texas Instruments Incorporated.

TABLE OF CONTENTS

CONTENTS **PAGE**

Introduction

Texas Instruments (TI) is pleased to provide pertinent information to assist in qualifying your TI Programmable Logic Devices (PLDs). Included is information on the steps TI takes to ensure quality of the PLD products. The following pages contains characterization data, packaging information, process, and die information for TI PLDs.

The TI IMPACT-X™ family includes both 20- and 24-pin standard architectures available in three speed selections. The TIBPAL22V10-15C and programmable sequencers are also manufactured with IMPACT-X™ technology. The TIBPAL22V10-15C provides a more flexible architecture than the standard PLDs and has become a standard of its own. The programmable sequencers, TIBPSG507AC and TIBPLS506AC, offer a unique architecture suited for large state machines and complex timing generators.

The Texas Instruments High-Speed 1-µm CMOS technology is used for a zero power version of the popular '22V10 architecture as well as our EPLD series which includes the EP330, EP630, and EP1830. These devices offer high-speed performance, low-power consumption, and superior design flexibility.

All TI bipolar devices use a titanium-tungsten (TiW) fuse technology developed at TI in 1970 to improve programming reliability. Proven TiW construction essentially eliminates the tendency of a fuse to grow back by insulating it with a layer of titanium oxide. The CMOS products employ an EPROM type technology, using a FAMOS transistor as the programmable element.

For more information on TI's programmable logic family contact your local TI Field Sales Office, Authorized Distributor, or by calling Texas Instruments at (214) 997-5666.

PLD Average Outgoing Quality

The quality of a product is its degree of conformance to its specified parameters. It pertains to the probability of defective units existing in a given lot of devices when received by the user. Although zero defects is the goal, the probability of some level of defective units still exists in any lot of mass produced items. The number of defective units received by the user is a function of the average outgoing quality achieved by the supplier. TI's outgoing quality is the index that quantifies the average number of defective components in all the products supplied. Average outgoing quality is expressed in number of defective parts per million (ppm).

TI monitors Average Outgoing Quality (AOQ) by the standard formula :

$$\text{AOQ} = \frac{\#\ \text{rejections}}{\text{total}\ \#\ \text{tested}} \times (1 - \text{LRR})$$

where LRR is the Lot Rejection Ratio

Each outgoing lot receives 100% static (dc), dynamic (ac), and functional guardbanded testing at room and high temperature prior to being lot acceptance (L/A) sampled and tested for conformance to published data book parameters. This L/A testing generates the AOQ results discussed above. Contact the factory for the latest information to determine the current AOQ of programmable logic devices.

Quality and Reliability Assurance Programs

Texas Instruments is committed to providing quality and reliable products and goes to great length to ensure this. This process includes full device characterization, qualification of new and changed processes, qualification of package and individual devices, full production testing, statistical sample lot accept, and a reliability monitor program.

The characterization of a new device is performed on at least three different die lots of material. The bipolar characterization includes material of extreme resistor tolerance as well as nominal values. These tests are over worst case conditions and test static (dc) parametrics, dynamic (ac) parametrics, programmability, and worst case ac code evaluation.

Device fabrication, chip mounting materials, handling procedures, and leadframe construction all effect device reliability. These and many other areas of product manufacturing are continuously investigated and refined. A qualification must be performed on a new or changed manufacturing process, a new package or assembly process, as well as on each individual device type. This qualification procedure include the following reliability tests.

Operating Life Test

This is a test in which the devices are subjected to a high-temperature environment under bias. The temperature is usually 125°C to 150°C. The bias can be either dynamic in which case the inputs and outputs are toggling; or static, where a constant voltage is applied to some or all of the pins. This test is used to accelerate failure mechanisms which are time and temperature dependent. In a short period of time it can simulate long term device operation and determine early and intrinsic device failure rates. Some of the common failure mechanisms are surface charge accumulation, charge injection, dielectric breakdown, and intermetallic growth.

Biased Humidity

In this environmental test the subject device is exposed to high humidity and temperature conditions while having electrical bias applied to the circuit. This procedure is designed to measure the device's susceptibility to electrolysis and electrolytic corrosion. Failure mechanisms enhanced as a result of bias humidity include: corrosion of the aluminum metallization on the die; silver, tin, or gold migration from the leadframe; and parametric failures related to ionic conduction at the die/package interface. The actual temperature and humidity combinations used can vary but one of the industry standards is 85°C and 85% relative humidity and is referred to as "85/85". With the recent agreement within the electronic industry of JEDEC Standard No. 22-A110 for Highly-Accelerated Temperature and Humidity Stress Test (HAST), the use of temperature accelerated (100°C to 140°C) humidity biased tests has become more prominent. These extreme conditions require special chambers and greatly accelerate the failure mechanisms. TI commonly uses the 130°C - 85% relative humidity HAST test for qualification. This test has a 20 to 1 acceleration factor over the more common "85/85" biased humidity test.

Autoclave

This environmental test of device reliability involves exposing the subject part to an atmosphere of high-temperature saturated steam under pressure (121°C, 100% relative humidity at 15 psig). Unlike the biased humidity test, no electrical bias is applied to the device and the test durations somewhat shorter. It indicates the susceptibility of the device to galvanic corrosion and therefore electromotive forces of the elements involved are of great concern. The chemical instability of the encapsulating material and its tendency to form electrolytes influence the number of failures that result from this test.

Temperature Cycling / Thermal Shock

These reliability test are used to determine the thermomechanical compatibility of the materials used in device construction. These tests require cycling of the ambient temperature of the environment from a low point of −65°C to a high temperature of 150°C. These temperature extremes are not intended to simulate actual operation, but rather to exaggerate any faults that might exist. No bias is applied to the device. Temperature cycling uses a gas environment and thermal shock uses a liquid environment.

Storage Life

This test consist of storing units unbiased at 150°C for a period of time. The primary failure mechanism accelerated by this test is Kirkendal Voiding.

Electrostatic Discharge (ESD) Test

The ESD test is used to determine the electrostatic discharge sensitivity threshold of a device. The test consist of applying current pulses of known intensity and duration to individual pins of a device. The pin combinations stressed are in accordance with Mil-Std-883C Condition 3015.7 Notice 8. The units are electrically tested to determine the threshold voltage at which the parts are ESD sensitive.

Data Retention

This test is run on CMOS EPLD devices to test the integrity of the FAMOS transistors. Initially the FAMOS transistors of the units are injected with a charge to bring them up to a certain voltage threshold. The units are then stored at 200°C for 1000 hours. The transistor threshold voltage is then measured for charge loss. Due to the high temperature this is performed on ceramic devices only.

The following chart shows the minimum testing required for a standard qualification program of a new device in a qualified plastic encapsulated package per TI QSS 009-003. The minimum electrical endpoints for these test are the 25°C ac/dc data book limits.

TEST	CONDITIONS	DURATION	SS/F
Operating Life	Dynamic or Static,125°C	1000 HRS	129/0
Storage Life	Unbiased,150°C	1000 HRS	45/0
Biased Humidity	85°C / 85% RH	1000 HRS	76/0
Temperature Cycle	−65°C / 150°C	1000 CYC	76/0
Thermal Shock	−65°C / 150°C	200 CYC	45/0
Autoclave	121°C / 15 PSIG	240 HRS	45/0
ESD	Mil-Std-883C, Cond 3015.7 Notice 8. Human Body Model	2 kV	3/0
Data Retention†	200°C	1000 HRS	76/0
Latchup†		250 mA, 2 X V_{CC} max	5/0

† CMOS Products Only

Texas Instruments has implemented an accelerated qualification program in order to maintain a high standard of quality and provide its customers with timely introduction of new devices. This program flow can be used if the technology and package for a new device has been qualified through the standard flow.

The following chart shows the minimum tests, conditions, endpoints, and sample size/accepted failures of an accelerated qualification. When this flow is used the test are normally run to standard qualification endpoints for additional information.

TEST	CONDITIONS	DURATION	SS/F
Operating Life	Dynamic or Static,150°C	416 HRS	129/0
Operating Life	Dynamic or Static,125°C	168 HRS	129/0
HAST	130°C / 85% RH	100 HRS	76/0
Thermal Shock	−65°C / 150°C	200 CYC	45/0
ESD	Mil-Std-883C, Cond 3015.7 Notice 8. Human Body Model	2 kV	3/0
Latchup†		250 mA, 2 X V_{CC} max	5/0

† CMOS Products Only

In order to monitor the reliability of current released products, samples are pulled on a monthly basis from representative device families. These samples are stressed and tested on the following four reliability tests :

125°C Operating Life
85°C/85% RH Biased Humidity
−65°C/150°C Temperature Cycling
Autoclave

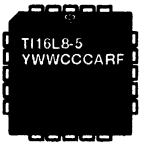
The results of testing and failure analysis of any failures is compiled and reported on a quarterly basis. For the current reliability information, please contact your local TI sales office or the TI technical support line at (214) 007-5666.

Package Symbolization

The top-side symbolization of each TI device includes more than just a part number. Additional information, including the date of assembly, the die revision code, wafer lot number or tracer code, as well as manufacturing and assembly site information. This traceability, combined with wafer lot history and TI's ongoing reliability monitoring programs helps assure our customers of our commitment to produce the highest quality and most reliable programmable logic devices available today.

The following symbolization diagrams show how to interpret the information on each package.

PLCC PACKAGES



Y = YEAR
WW = WEEK
CCC = TRACE CODE
A = ASSEMBLY SITE
R = DIE REVISION
F = WAFER FAB

DIP PACKAGES

ZZZZZ = DIE LOT NO.
Y = YEAR
WW = WEEK
# = DIE REVISION
(X = NO REVISION)
L = WAFER FAB CODE

Process Information

IMPACT-X
(Implanted Advanced Composed Mask Technology)

1.	Process Technology :	Trench-Isolated Bipolar, 1.5 μm minimum feature size, 4 μm metal pitch
2.	Wafer Fabrication:	Houston Fab 1 (HFAB1)
3.	Assembly Location :	TI-Malaysia (DIP), TI-Philippines (PLCC), TI-Taiwan (CDIP)
4.	Test Location :	TI-Malaysia (DIP), TI-Philippines (PLCC), TI-Taiwan (CDIP)
5.	Number of Metal Layers :	Two
6.	Content of Metallization :	1st level - TiW, 2% Cu/Al 2nd level - TiW-Al
7.	Metal Thickness :	1st level - 0.75 μm 2nd level - 1.5 μm
8.	Minimum Line/Spacing Width :	2 μm width, 2 μm spacing
9.	Contact Dimensions (via's) :	3 μm
10.	Passivation Material :	Low stress compressive nitride
11.	Passivation Thickness :	10,000 Angstroms
12.	ESD Protection :	2000 Volts

CMOS

1.	Process Technology :	CMOS EPROM 1.0 μm Double Level Metal
2.	Wafer Fabrication:	Lubbock (LMOS)
3.	Assembly Location :	TI-Malaysia (DIP), TI-Philippines (PLCC), TI-Taiwan (CDIP)
4.	Test Location :	TI-Malaysia (DIP), TI-Philippines (PLCC), TI-Taiwan (CDIP)
5.	Number of Metal Layers :	Two
6.	Content of Metallization :	1st level - Ti,TiW, 2% Cu/Al 2nd level - TiW-2% Cu/Al
7.	Metal Thickness :	1st level - 0.8 μm 2nd level - 1.05 μm
8.	Minimum Line/Spacing Width :	1 μm width, 1 μm spacing
9.	Contact Dimensions (via's) :	0.5 μm
10.	Passivation Material :	PECVD oxy-nitride
11.	Passivation Thickness :	12,000 Angstroms
12.	ESD Protection :	2000 Volts

20-pin 5-ns IMPACT-X PLDs

Devices included in this section:

TIBPAL16L8-5C
TIBPAL16R4-5C
TIBPAL16R6-5C
TIBPAL16R8-5C

DEVICE INFORMATION
20-pin 5-ns IMPACT-X PLDs

1. Technology .... IMPACT-X
2. Package Types : .... 20-pin plastic DIP,
   20-pin plastic PLCC
3. Last Die Revision .... X (None)
4. Bar Size : .... 16L8 : 85 x 107 mils
   16R4 : 93 x 107 mils
   16R6 : 93 x 107 mils
   16R8 : 93 x 107 mils
5. Still Air Thermal Impedance :

	PDIP	PLCC
$R_{\theta JA}$	66.7	105.1
$R_{\theta JC}$	28.7	29.4

6. $R_{\theta JA}$ with Air Flow :

FPM	PDIP	PLCC
0	87.5	103.5
100	75.5	82.2
250	61.0	64.6
500	48.3	51.7
750	42.6	
1000	40.3	

QUALIFICATION INFORMATION

The TIBPAL16XX-5 devices are qualified using the accelerated qualification program.The following summaries give the required tests and results for each device and any additional test performed for additional data. With this particular device family, the TIBPAL16XX and the TIBPAL20XX parts are essentially the same die so the data for these two families are the same.

16L8-5 and 20L8-5

Required Tests and Results for TIBPAL16L8-5 and TIBPAL20L8-5

Device Type:	20L8-5
Package Type:	24 pin PDIP
Date Code:	944XF
Die Lot Number:	361

TEST	SS/F	ENDPOINT	RESULTS	EXTENDED READPOINT	RESULTS
150°C Dynamic Op-Life	129/1	416 HRS	129/0		
125°C Dynamic Op-Life	129/1	168 HRS	128/0[1]	1000 HRS	128/0
130°C/85% RH HAST	76/0	500 HRS	76/0		
–65°C/150°C Thermal Shock	129/1	500 CYC	129/0		
ESD	3/0	2000 V	3/0		

Additional Qualification Tests and Results for TIBPAL16L8-5 and TIBPAL20L8-5

Device Type:	20L8-5
Package Type:	24 pin PDIP
Date Code:	009XF
Die Lot Numbers:	02332, 29314, and 35505

TEST	ENDPOINT	RESULTS
150°C Dynamic Op-Life	416 HRS	201/2[2]
125°C Dynamic Op-Life	1000 HRS	201/0
130°C/85% RH HAST	200 HRS	201/0
–65°C/150°C Thermal Shock	1000 CYC	201/0
ESD	2000 V	3/0

16R4-5 and 20R4-5

Required Tests and Results for TIBPAL16R4-5 and TIBPAL20R4-5

Device Type:	20R4-5
Package Type:	24 pin PDIP
Date Code:	048XF
Die Lot Number:	28933

Required Tests and Results for TIBPAL16R4-5 and TIBPAL20R4-5 (continued)

TEST	SS/F	ENDPOINT	RESULTS	EXTENDED READPOINT	RESULTS
125°C Dynamic Op-Life	129/1	1000 HRS	128/1[3]	2000 HRS	128/0
130°C/85% RH HAST	129/1	100 HRS	129/0		
–65°C/150°C Thermal Shock	129/1	1000 CYC	129/0		
ESD	3/0	2000 V	6/0		

16R6-5 and 20R6-5

Required Tests and Results for TIBPAL16R6-5 and TIBPAL20R6-5

Device Type:	20R6-5
Package Type:	24 pin PDIP
Date Code:	9122
Die Lot Number:	1127109

TEST	SS/F	ENDPOINT	RESULTS	EXTENDED READPOINT	RESULTS
125°C Dynamic Op-Life	129/1	1000 HRS	129/0		
130°C/85% RH HAST	129/1	100 HRS	127/0[4]		
–65°C/150°C Thermal Shock	129/1	1000 CYC	129/0		
–65°C/150°C Temp Cycle	129/1	1000 CYC	129/0		
ESD	3/0	2000 V	3/0		

16R8-5 and 20R8-5

Required Tests and Results for TIBPAL16R8-5 and TIBPAL20R8-5

Device Type:	20R8-5
Package Type:	24 pin PDIP
Date Code:	048XF
Die Lot Number:	0289233

TEST	SS/F	ENDPOINT	RESULTS	EXTENDED READPOINT	RESULTS
150°C Dynamic Op-Life	129/1	416 HRS	129/0	1000 HRS	129/0
125°C Dynamic Op-Life	129/1	168 HRS	129/0	1000 HRS	129/0
130°C/85% RH HAST	129/1	200 HRS	129/0		
–65°C/150°C Thermal Shock	129/1	200 CYC	129/0		
–65°C/150°C Temp Cycle	129/1	1000 CYC	129/0		
ESD	3/0	2000 V	3/0		
Autoclave	76/0	240 HRS	76/0		

Additional Qualification Tests and Results for TIBPAL16R8-5 and TIBPAL20R8-5

Device Type:	20R8-5
Package Type:	24 pin PDIP
Date Code:	106XF
Die Lot Numbers:	0289233, 0310676, and 1 011759

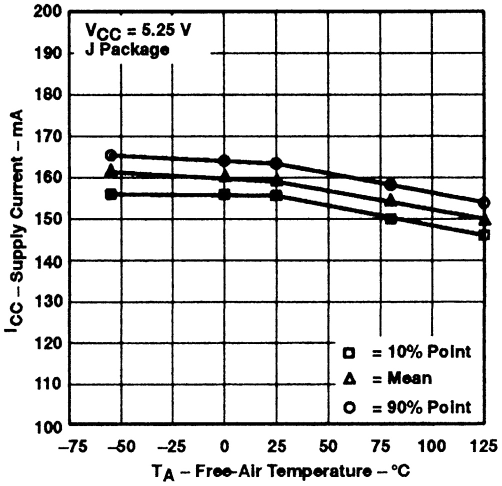
TEST	**ENDPOINT**	**RESULTS**
150°C Dynamic Op-Life	416 HRS	400/1[3]
125°C Dynamic Op-Life	1000 HRS	400/0
85°C/85% RH Biased Humidity	1000 HRS	201/0
–65°C/150°C Temp Cycle	1000 CYC	201/1[4]
ESD	2000 V	3/0

1. 1 unit received EOS damage due to reverse socket insertion - removed from population.
2. Failure determined to be caused by ESD/EOS, source unknown. TI FA Report # D12-00531
3. Failure determined to be caused by reverse socketing. TI FA Report # D12-00662
4. 2 units mechanically damaged beyond repair – unable to test – removed from sample.
5. Failure caused by mechanical damage of 1st level metal. TI FA Report # D13-00004
6. Failure analysis results conclude interlevel oxide crack caused metal-1 to metal-2 short. TI FA Report # D13-00010

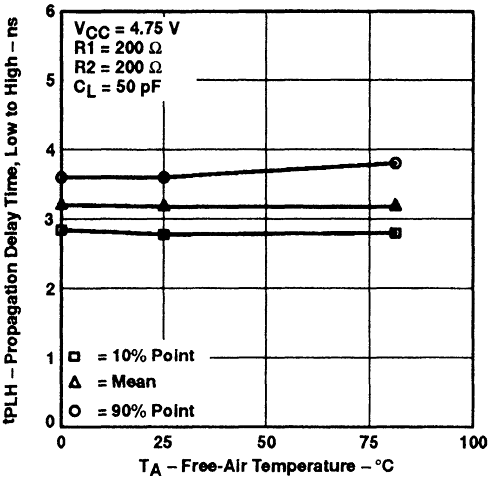
CHARACTERIZATION INFORMATION

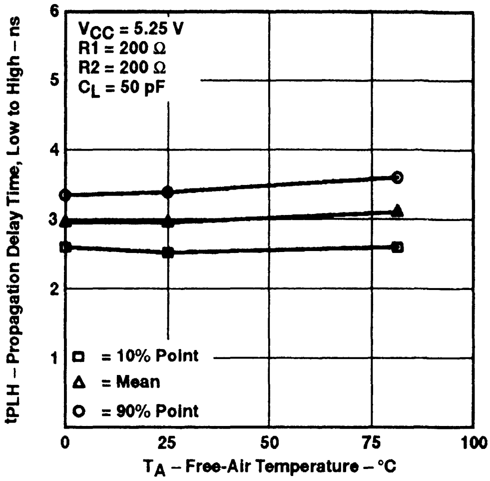
TIBPAL16L8-5C
TIBPAL16R8-5C

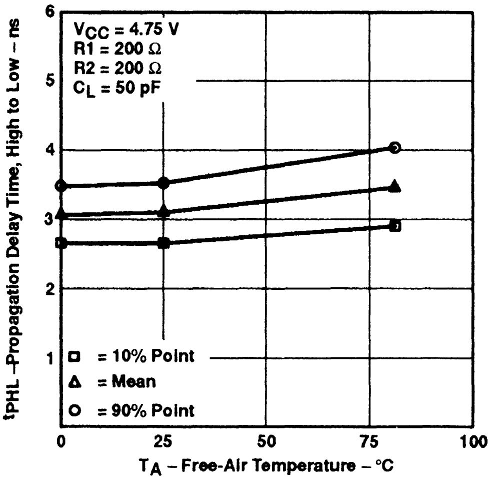
SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

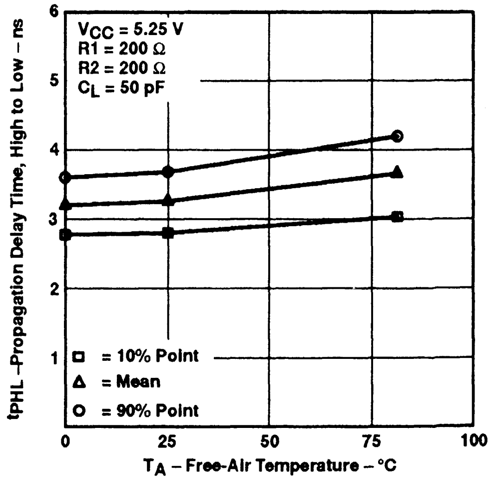


TIBPAL16L8-5C (continued)


PROPAGATION DELAY TIME
(t_{PLH} from I, I/O to O, I/O)
vs
FREE-AIR TEMPERATURE

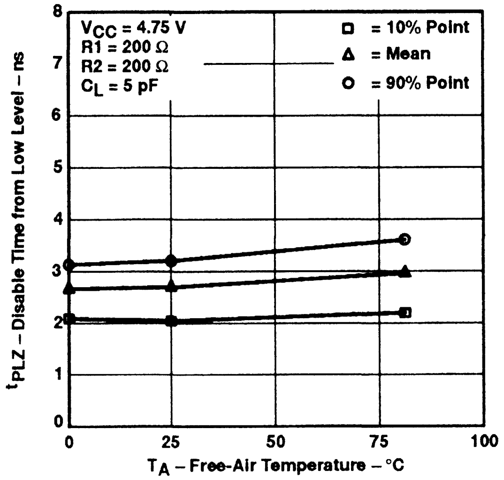

PROPAGATION DELAY TIME
(t_{PLH} from I, I/O to O, I/O)
vs
FREE-AIR TEMPERATURE


PROPAGATION DELAY TIME
(t_{PHL} from I, I/O to O, I/O)
vs
FREE-AIR TEMPERATURE

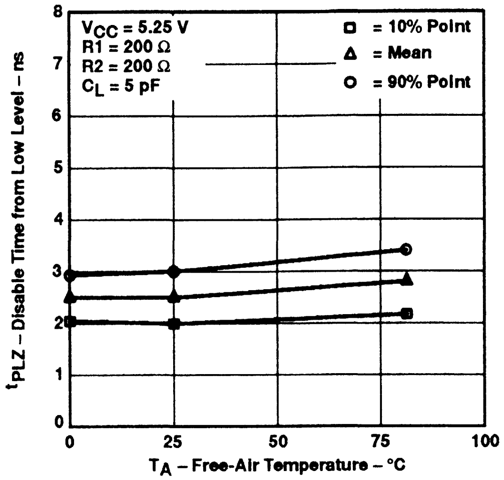

PROPAGATION DELAY TIME
(t_{PHL} from I, I/O to O, I/O)
vs
FREE-AIR TEMPERATURE

TIBPAL16L8-5C (continued)

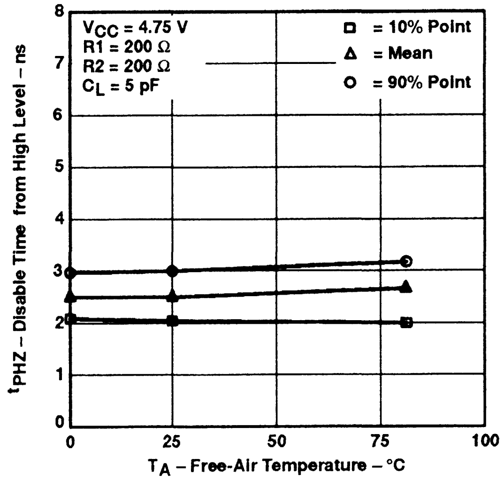
DISABLE TIME
(t_{PLZ} from I, I/O to O, I/O)
vs
FREE-AIR TEMPERATURE



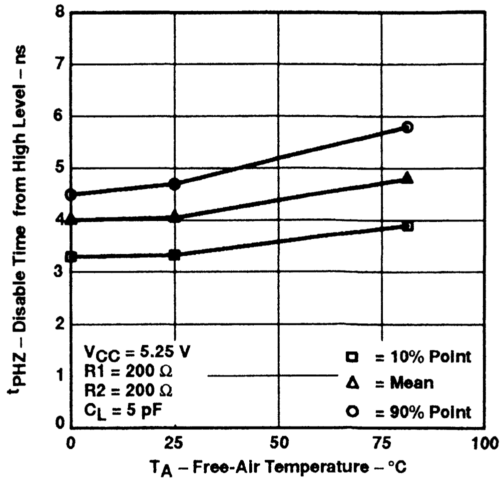
DISABLE TIME
(t_{PLZ} from I, I/O to O, I/O)
vs
FREE-AIR TEMPERATURE



DISABLE TIME
(t_{PHZ} from I, I/O to O, I/O)
vs
FREE-AIR TEMPERATURE

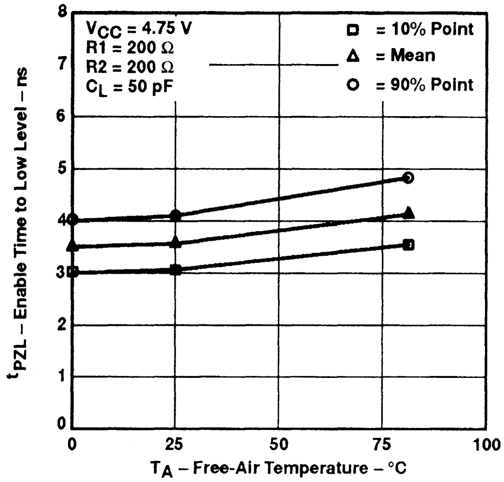


DISABLE TIME
(t_{PHZ} from I, I/O to O, I/O)
vs
FREE-AIR TEMPERATURE

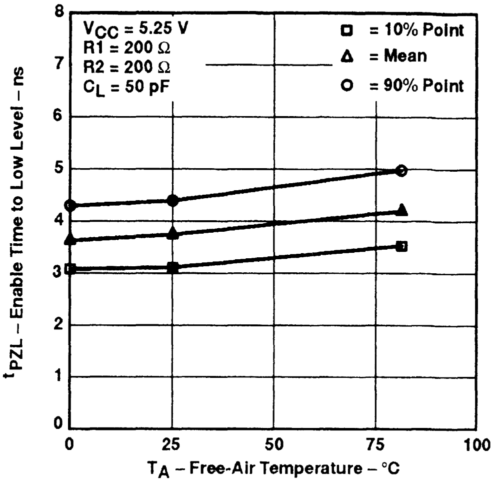


TIBPAL16L8-5C (continued)

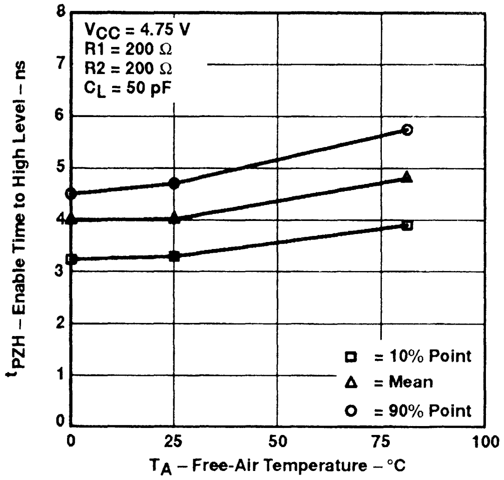
ENABLE TIME
(t_{PZL} from I, I/O to O, I/O)
VS
FREE-AIR TEMPERATURE



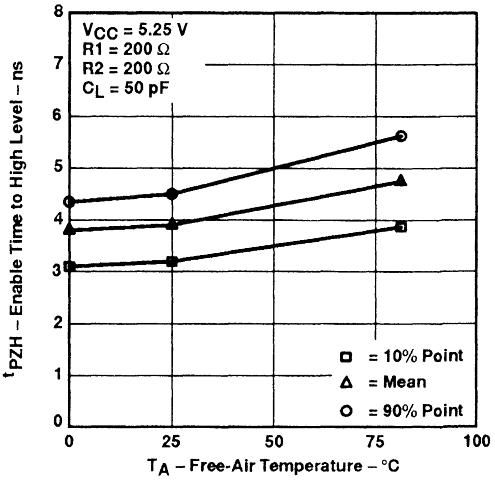
ENABLE TIME
(t_{PZL} from I, I/O to O, I/O)
VS
FREE-AIR TEMPERATURE



ENABLE TIME
(t_{PZH} from I, I/O to O, I/O)
VS
FREE-AIR TEMPERATURE

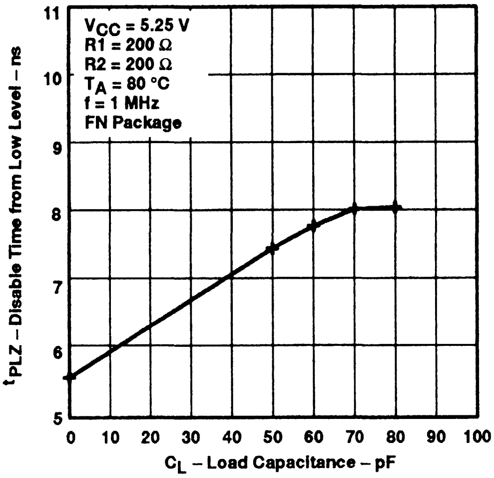


ENABLE TIME
(t_{PZH} from I, I/O to O, I/O)
VS
FREE-AIR TEMPERATURE

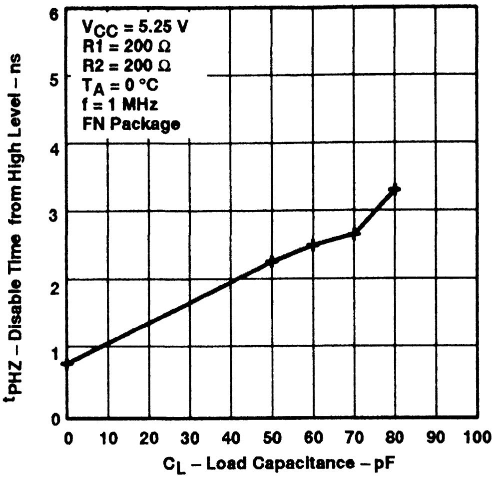


TIBPAL16R8-5C

DISABLE TIME (t_{PLZ})
$\overline{OE}$↑ to Q with 8 Outputs Switching In Phase
vs
LOAD CAPACITANCE

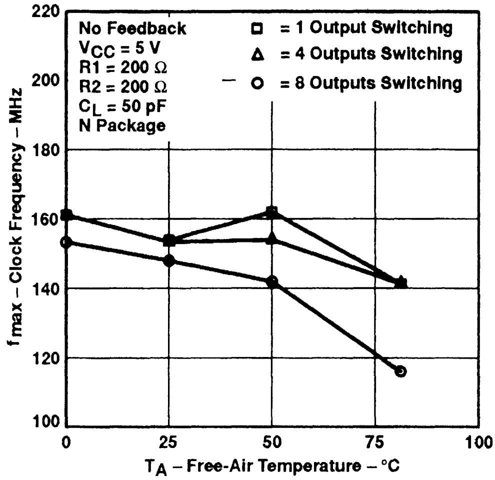


DISABLE TIME (t_{PHZ})
$\overline{OE}$↑ to Q with 1 Output Switching
vs
LOAD CAPACITANCE

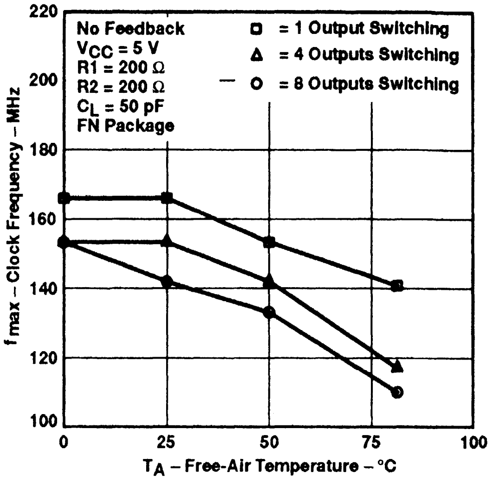


TIBPAL16R8-5C (continued)

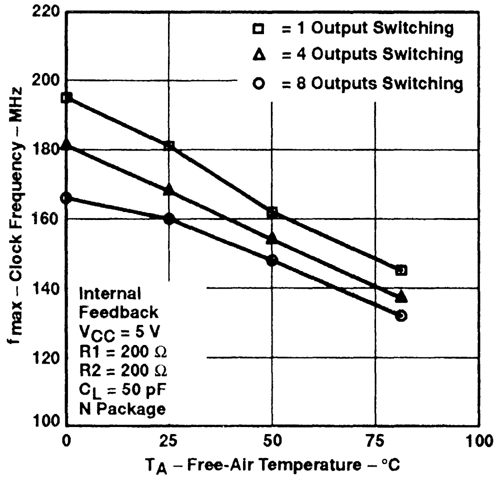
CLOCK FREQUENCY,
(Outputs Switching In Phase)
vs
FREE-AIR TEMPERATURE



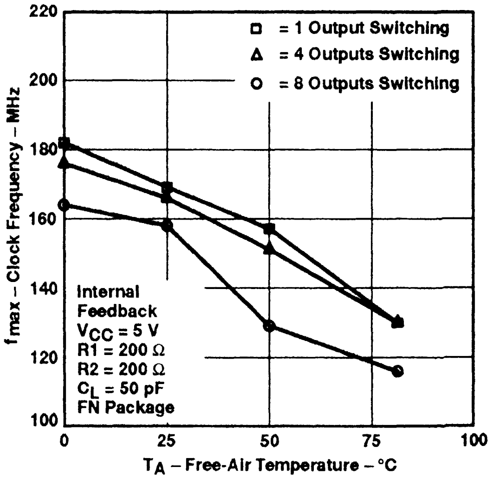
CLOCK FREQUENCY,
(Outputs Switching In Phase)
vs
FREE-AIR TEMPERATURE



CLOCK FREQUENCY,
(Binary Counter Configuration)
vs
FREE-AIR TEMPERATURE

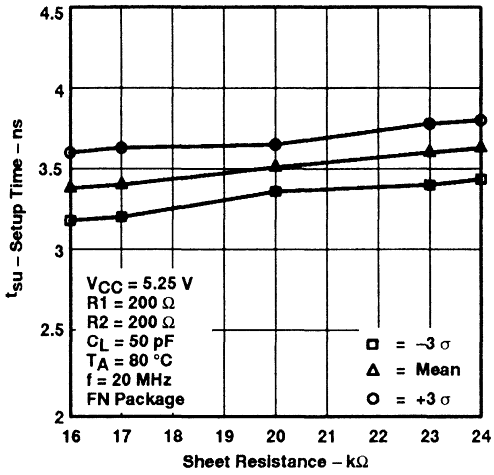


CLOCK FREQUENCY,
(Binary Counter Configuration)
vs
FREE-AIR TEMPERATURE

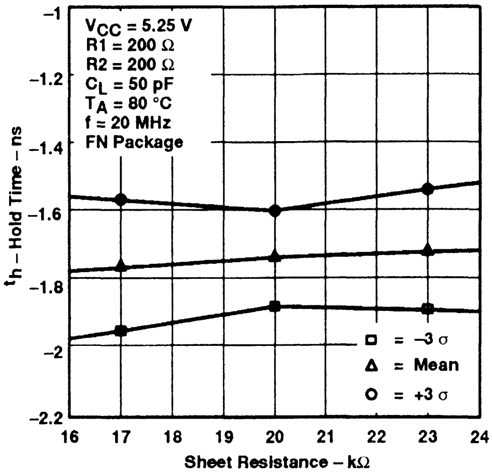


TIBPAL16R8-5C (continued)

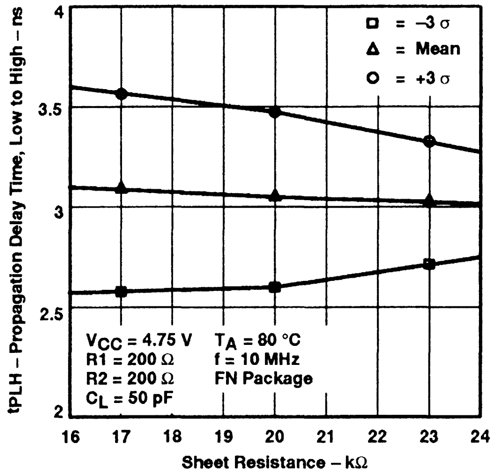
SETUP TIME (With 8 Outputs Switching in Alternate Direction) vs SHEET RESISTANCE



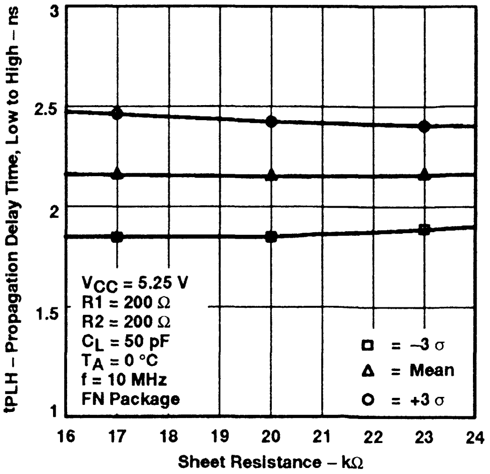
HOLD TIME (With 8 Outputs Switching in Same Direction) vs SHEET RESISTANCE



PROPAGATION DELAY TIME, CLK to Q (With 8 Outputs Switching In Same Direction) vs SHEET RESISTANCE

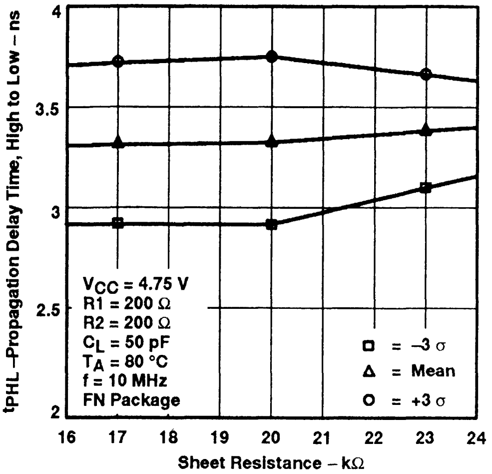


PROPAGATION DELAY TIME, CLK to Q (With 1 Output Switching) vs SHEET RESISTANCE

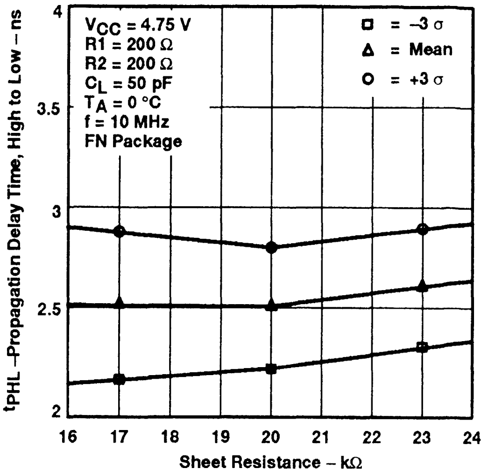


TIBPAL16R8-5C (continued)

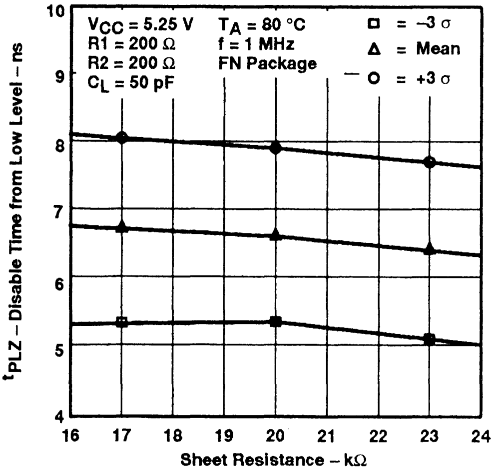
PROPAGATION DELAY TIME, CLK to Q (With 8 Outputs Switching in Same Direction) vs SHEET RESISTANCE



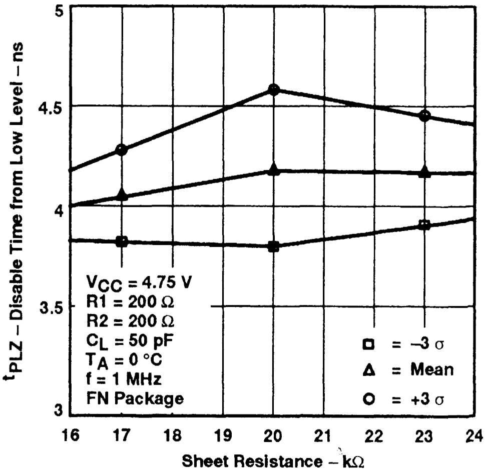
PROPAGATION DELAY TIME, CLK to Q (With 1 Output Switching) vs SHEET RESISTANCE



DISABLE TIME, $\overline{OE}$↑ to Q (With 8 Outputs Switching in Same Direction) vs SHEET RESISTANCE

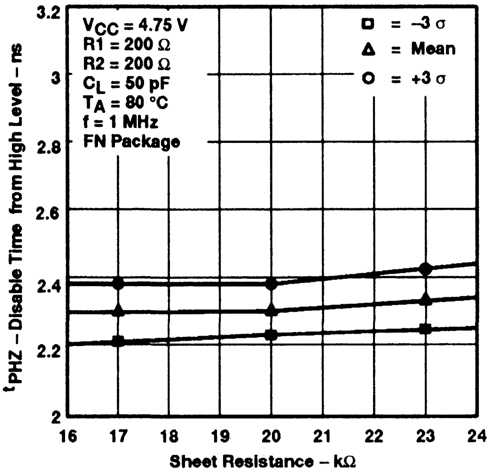


DISABLE TIME, $\overline{OE}$↑ to Q (With 1 Output Switching) vs SHEET RESISTANCE

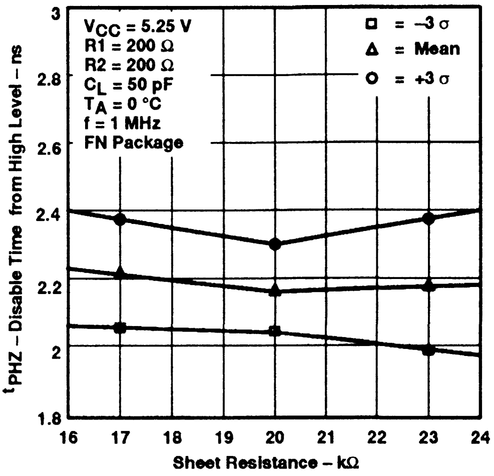


TIBPAL16R8-5C (continued)

DISABLE TIME, $\overline{OE}$↑ to Q (With 8 Outputs Switching In Same Direction) vs SHEET RESISTANCE

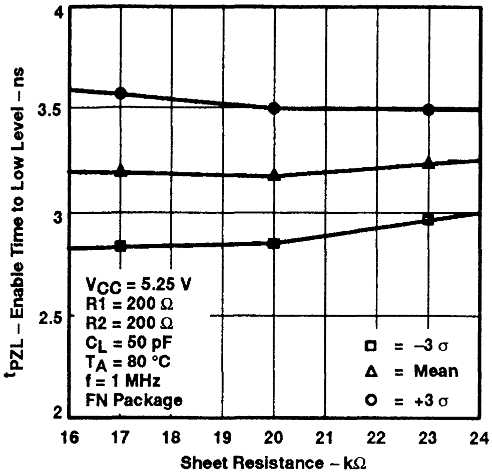


DISABLE TIME, $\overline{OE}$↑ to Q (With 1 Output Switching) vs SHEET RESISTANCE

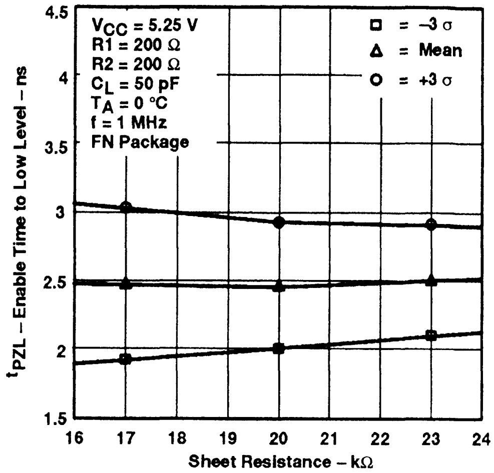


TIBPAL16R8-5C (continued)

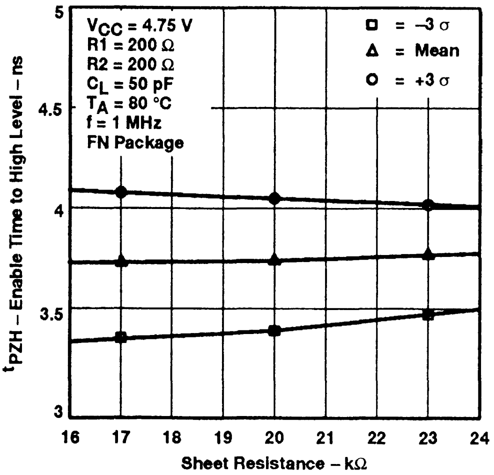
ENABLE TIME, $\overline{OE}\downarrow$ to Q
(With 8 Outputs Switching In Same Direction)
vs
SHEET RESISTANCE



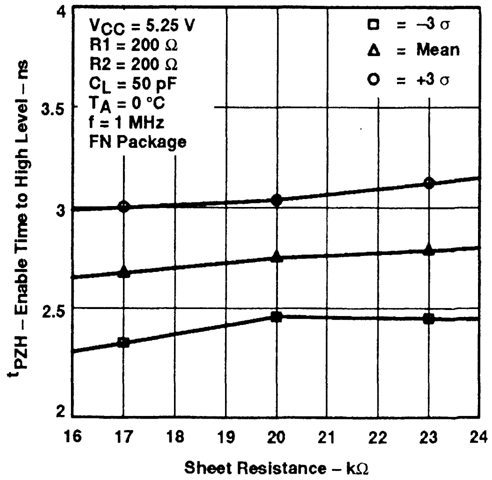
ENABLE TIME, $\overline{OE}\downarrow$ to Q
(With 1 Output Switching)
vs
SHEET RESISTANCE



ENABLE TIME, $\overline{OE}\downarrow$ to Q
(With 8 Outputs Switching In Same Direction)
vs
SHEET RESISTANCE



ENABLE TIME, $\overline{OE}\downarrow$ to Q
(With 1 Output Switching)
vs
SHEET RESISTANCE



20-pin 7-ns IMPACT-X PLDs

Devices included in this section:

TIBPAL16L8-7C
TIBPAL16R4-7C
TIBPAL16R6-7C
TIBPAL16R8-7C

DEVICE INFORMATION
20-pin 7-ns IMPACT-X PLDs

1. Technology .... IMPACT-X
2. Package Types : .... 20-pin plastic DIP,
   20-pin plastic PLCC
3. Last Die Revision .... X (None)
4. Bar Size .... 107 x 96 mils
5. Still Air Thermal Impedance :

	PDIP	PLCC
$R_{\theta JA}$	66.7	105.1
$R_{\theta JC}$	28.7	29.4

6. $R_{\theta JA}$ with Air Flow :

FPM	PDIP	PLCC
0	87.5	103.5
100	75.5	82.2
250	61.0	64.6
500	48.3	51.7
750	42.6	
1000	40.3	

This device is from the same master die as the TIBPAL20XX-7 and TIBPAL20XX-10 devices. Therefore the qualification and characterization data are the same.

QUALIFICATION INFORMATION

The TIBPAL16XX-7, TIBPAL20XX-7, and TIBPAL20XX-10 devices are qualified using the accelerated qualification program. The following summaries give the required tests and results for this device family as well as any additional test performed for additional data.

Required Tests and Results for TIBPAL16XX-7, TIBPAL20XX-7, and TIBPAL20XX-10

Device Types:	20R6-7, 20R8-7, and 20L8-7
Package Type:	24 pin PDIP
Date Codes:	935XF, 935XF, and 939XF
Die Lot Numbers:	15080, 14508, and 20604

TEST	SS/F	ENDPOINT	RESULTS	EXTENDED READPOINT	RESULTS
150°C Dynamic Op-Life	129/1	416 HRS	287/0		
125°C Dynamic Op-Life	129/1	168 HRS	257/0	1000 HRS	257/0
130°C/85% RH HAST	129/1	100 HRS	258/0		
–65°C/150°C Thermal Shock	129/1	100 CYC	129/0	1000 CYC	129/0
–65°C/150°C Temp Cycle	77/1	100 CYC	77/0	1000 CYC	77/0
ESD	3/0	2000 V	3/0		

Additional Qualification Tests and Results for TIBPAL16XX-7, TIBPAL20XX-7, and TIBPAL20XX-10

Device Type:	16R4-7
Package Type:	20 pin PDIP
Date Code:	922XF
Die Lot Numbers:	08980, 09343, and 09344

TEST	SS/F	ENDPOINT	RESULTS	EXTENDED READPOINT	RESULTS
150°C Dynamic Op-Life	129/1	384 HRS	201/0	1000 HRS	201/0
125°C Dynamic Op-Life	129/1	168 HRS	201/0	1000 HRS	201/0
130°C/85% RH HAST	129/1	100 HRS	199/0[1]		
–65°C/150°C Thermal Shock	77/1	200 CYC	201/0		
ESD	3/0	2000 V	3/0		

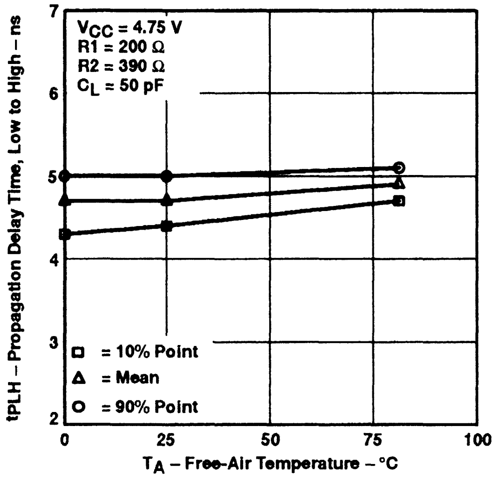
1. 2 units mechanically damaged beyond repair - unable to test - removed from sample.

CHARACTERIZATION INFORMATION

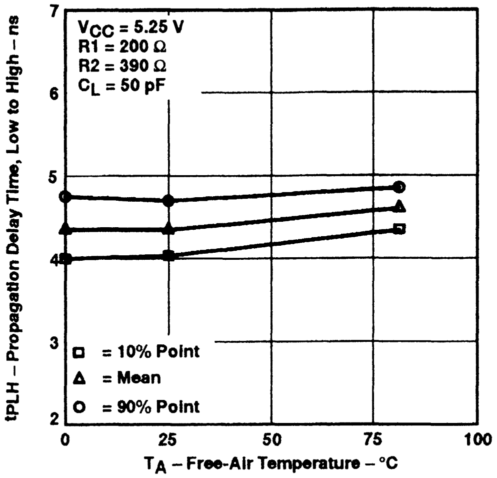
TIBPAL16L8-7C
TIBPAL16R4-7C
TIBPAL16R6-7C
TIBPAL16R8-7C

TIBPAL16L8-7C

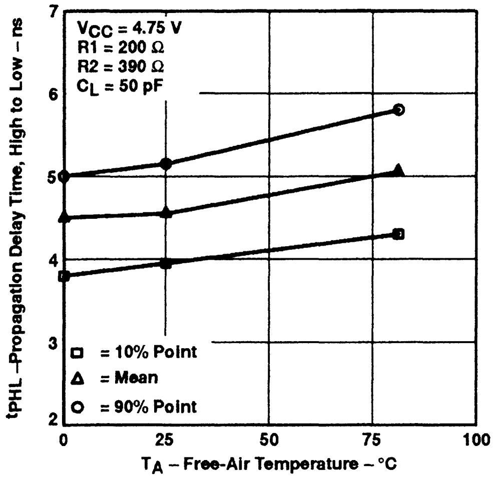
PROPAGATION DELAY TIME
(t_{PLH} from I, I/O to O, I/O)
vs
FREE-AIR TEMPERATURE



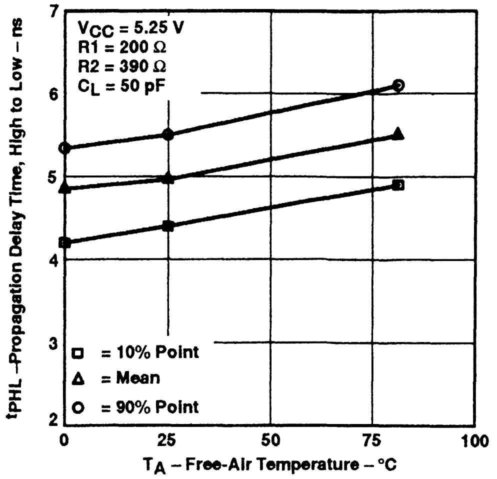
PROPAGATION DELAY TIME
(t_{PLH} from I, I/O to O, I/O)
vs
FREE-AIR TEMPERATURE



PROPAGATION DELAY TIME
(t_{PHL} from I, I/O to O, I/O)
vs
FREE-AIR TEMPERATURE

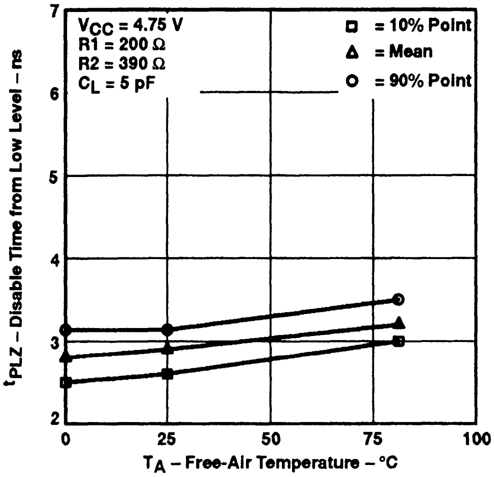


PROPAGATION DELAY TIME
(t_{PHL} from I, I/O to O, I/O)
vs
FREE-AIR TEMPERATURE

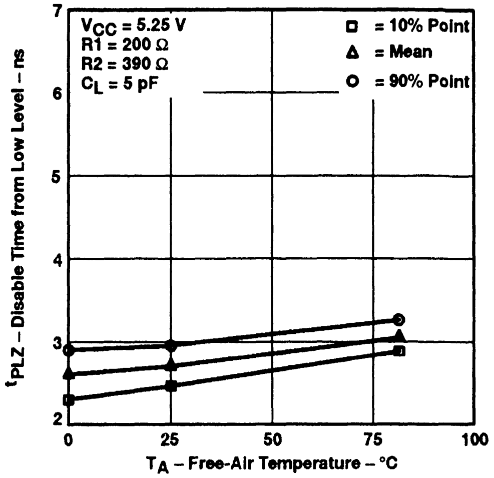


TIBPAL16L8-7C (continued)

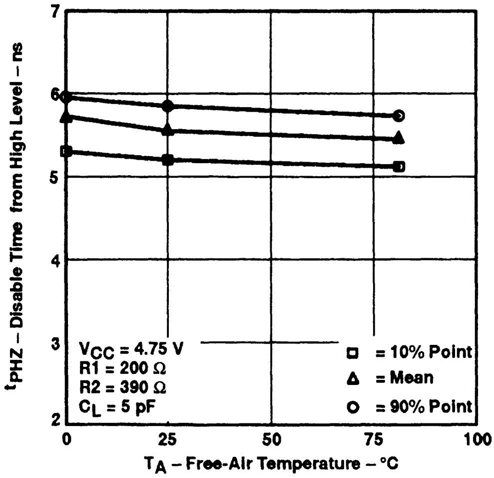
PROPAGATION DELAY TIME
(t_{PLZ} from I, I/O to O, I/O)
vs
FREE-AIR TEMPERATURE



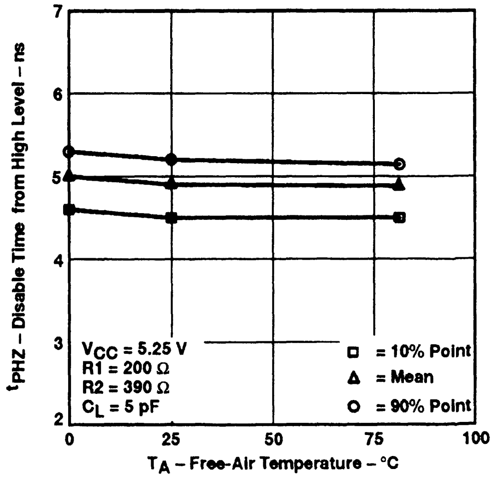
PROPAGATION DELAY TIME
(t_{PLZ} from I, I/O to O, I/O)
vs
FREE-AIR TEMPERATURE



PROPAGATION DELAY TIME
(t_{PHZ} from I, I/O to O, I/O)
vs
FREE-AIR TEMPERATURE

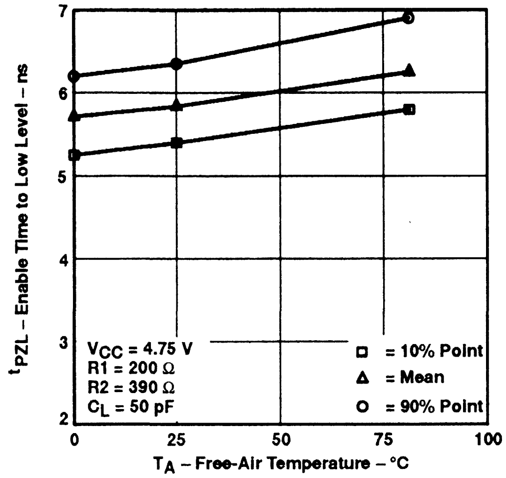


PROPAGATION DELAY TIME
(t_{PHZ} from I, I/O to O, I/O)
vs
FREE-AIR TEMPERATURE

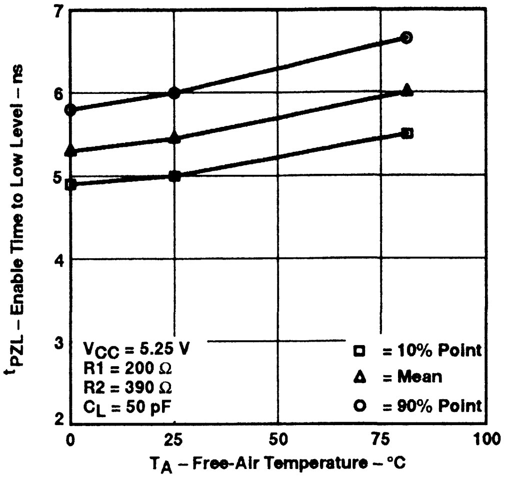


TIBPAL16L8-7C (continued)

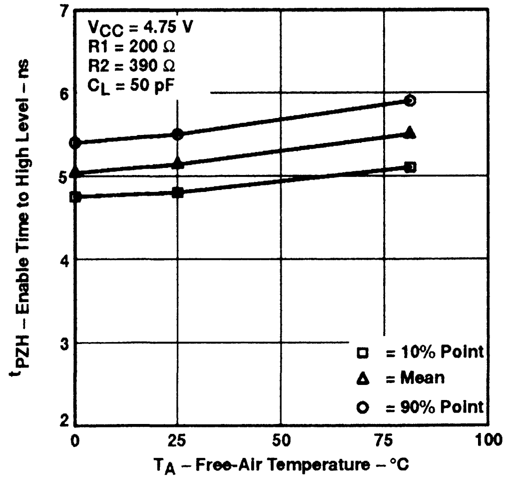
PROPAGATION DELAY TIME
(t$_{PZL}$ from I, I/O to O, I/O)
vs
FREE-AIR TEMPERATURE



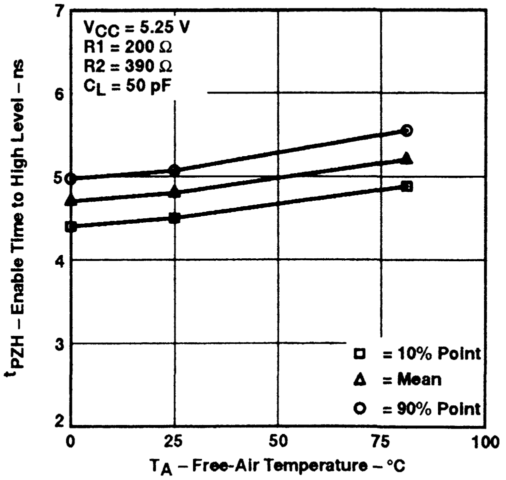
PROPAGATION DELAY TIME
(t$_{PZL}$ from I, I/O to O, I/O)
vs
FREE-AIR TEMPERATURE



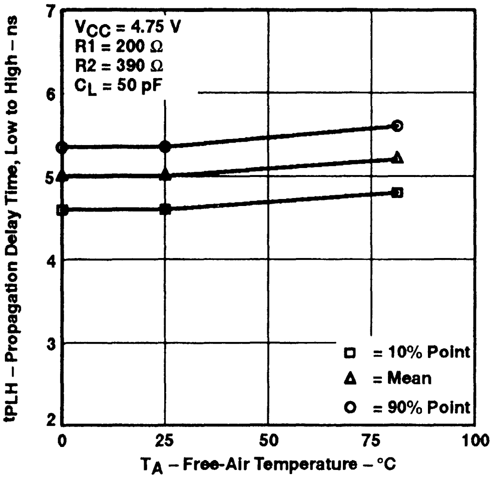
PROPAGATION DELAY TIME
(t$_{PZH}$ from I, I/O to O, I/O)
vs
FREE-AIR TEMPERATURE



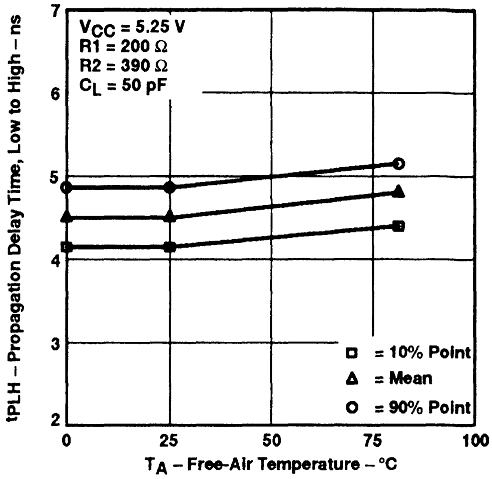
PROPAGATION DELAY TIME
(t$_{PZH}$ from I, I/O to O, I/O)
vs
FREE-AIR TEMPERATURE



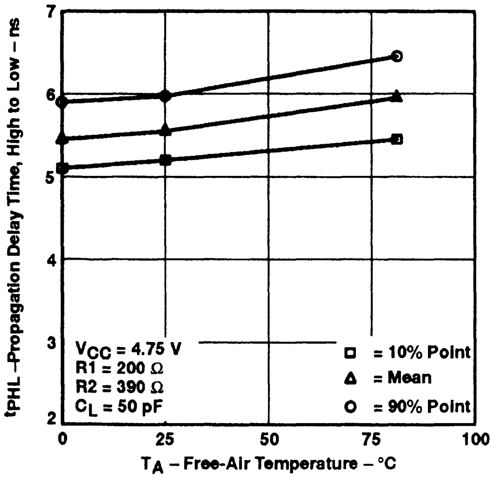
PROPAGATION DELAY TIME
(t_{PLH} from I, I/O to I/O)
vs
FREE-AIR TEMPERATURE



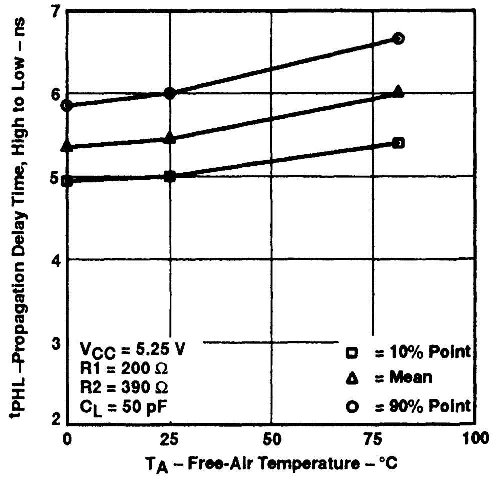
PROPAGATION DELAY TIME
(t_{PLH} from I, I/O to I/O)
vs
FREE-AIR TEMPERATURE



PROPAGATION DELAY TIME
(t_{PHL} from I, I/O to I/O)
vs
FREE-AIR TEMPERATURE

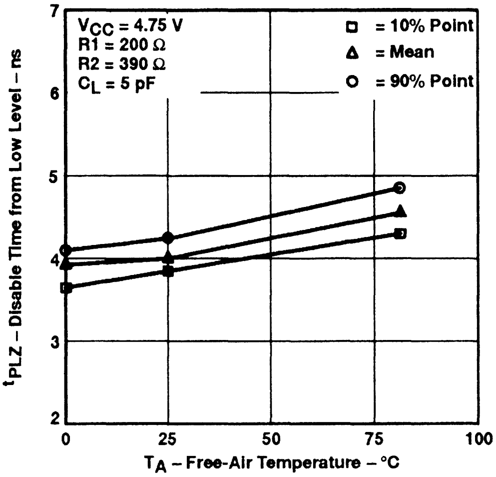


PROPAGATION DELAY TIME
(t_{PHL} from I, I/O to I/O)
vs
FREE-AIR TEMPERATURE

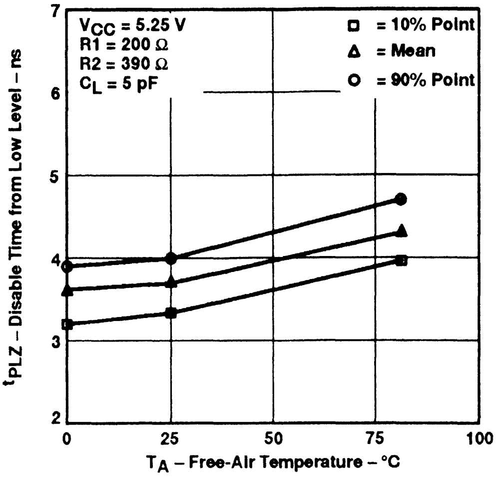


TIBPAL16R4-7C (continued)

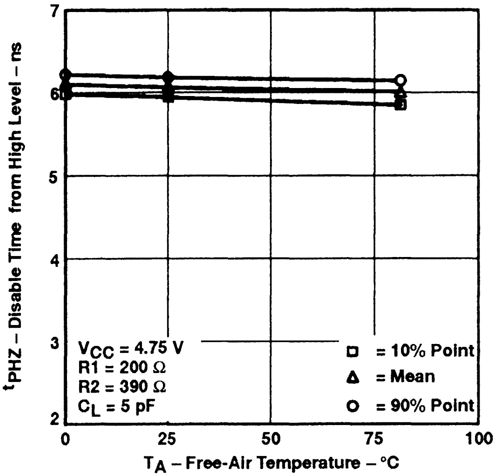
PROPAGATION DELAY TIME
(t_{PLZ} from I, I/O to I/O)
vs
FREE-AIR TEMPERATURE



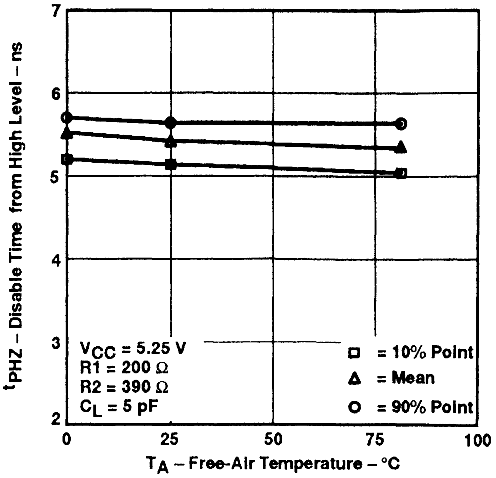
PROPAGATION DELAY TIME
(t_{PLZ} from I, I/O to I/O)
vs
FREE-AIR TEMPERATURE



PROPAGATION DELAY TIME
(t_{PHZ} from I, I/O to I/O)
vs
FREE-AIR TEMPERATURE

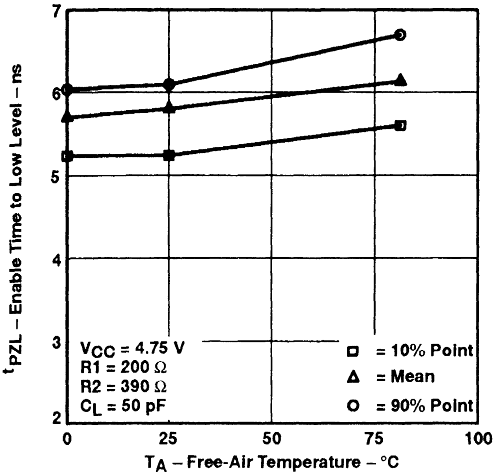


PROPAGATION DELAY TIME
(t_{PHZ} from I, I/O to I/O)
vs
FREE-AIR TEMPERATURE

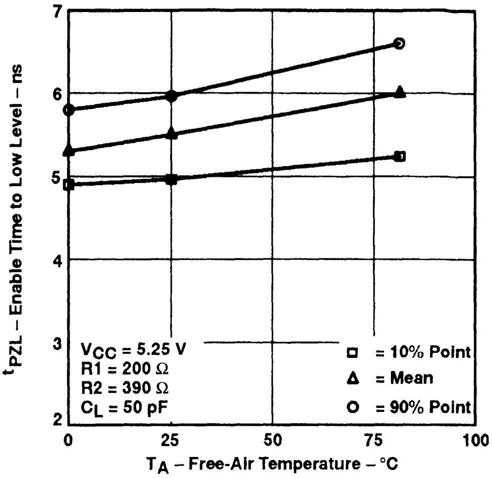


TIBPAL16R4-7C (continued)

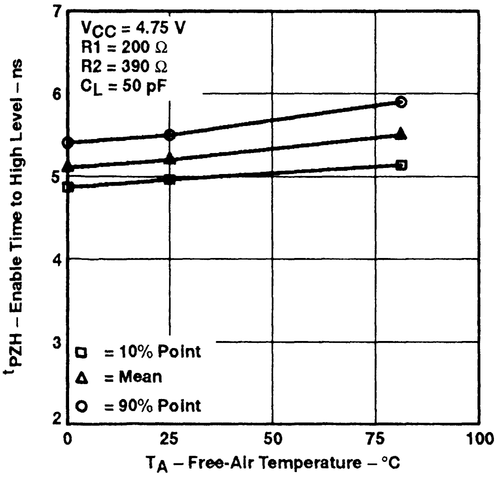
PROPAGATION DELAY TIME
(t_{PZL} from I, I/O to I/O)
vs
FREE-AIR TEMPERATURE



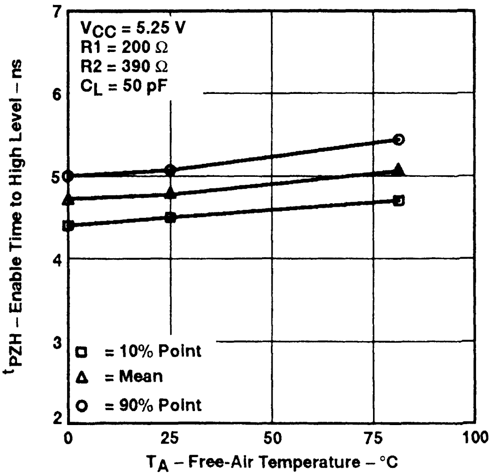
PROPAGATION DELAY TIME
(t_{PZL} from I, I/O to I/O)
vs
FREE-AIR TEMPERATURE



PROPAGATION DELAY TIME
(t_{PZH} from I, I/O to I/O)
vs
FREE-AIR TEMPERATURE

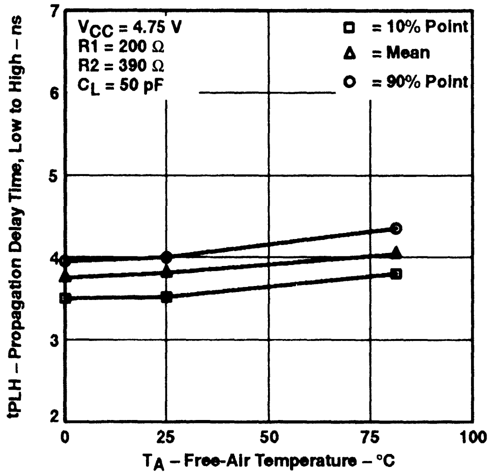


PROPAGATION DELAY TIME
(t_{PZH} from I, I/O to I/O)
vs
FREE-AIR TEMPERATURE

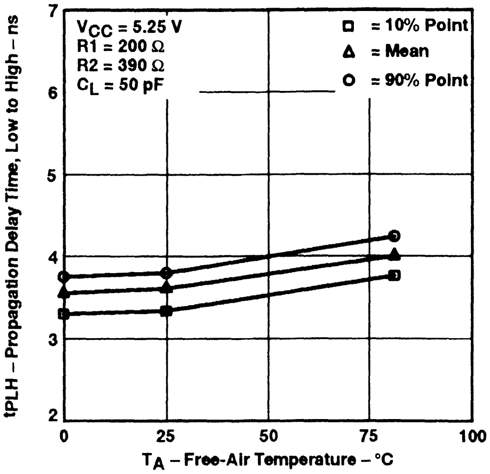


TIBPAL16R4-7C (continued)

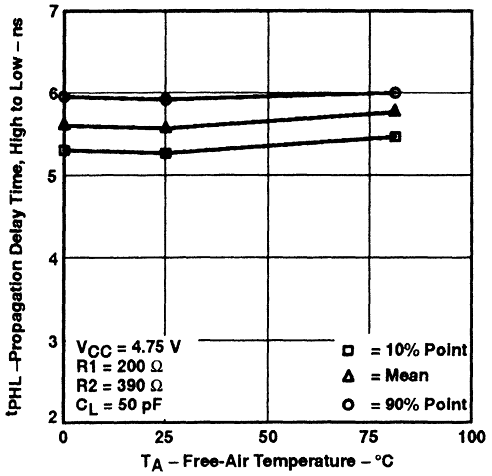
PROPAGATION DELAY TIME
(t_{PLH} from CLK to Q)
vs
FREE-AIR TEMPERATURE



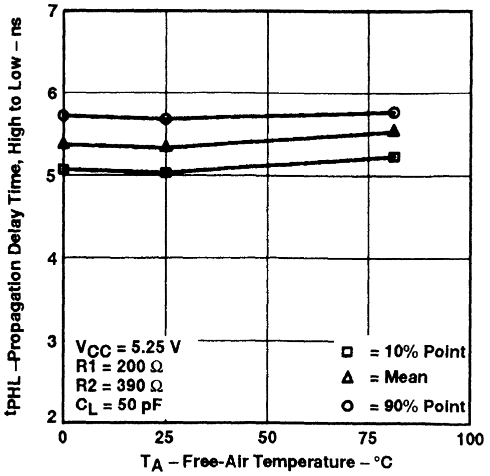
PROPAGATION DELAY TIME
(t_{PLH} from CLK to Q)
vs
FREE-AIR TEMPERATURE



PROPAGATION DELAY TIME
(t_{PHL} from CLK to Q)
vs
FREE-AIR TEMPERATURE

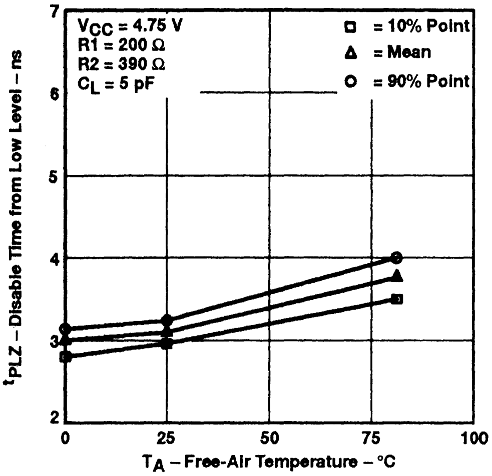


PROPAGATION DELAY TIME
(t_{PHL} from CLK to Q)
vs
FREE-AIR TEMPERATURE

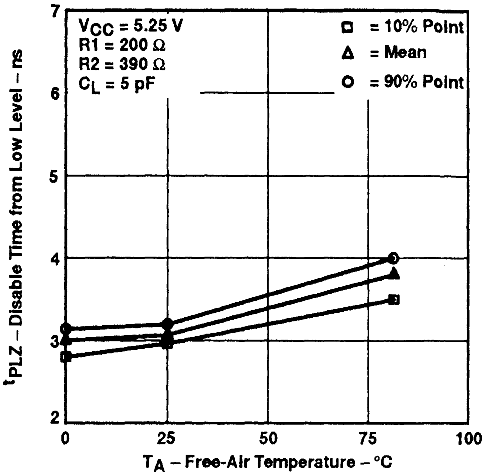


TIBPAL16R4-7C (continued)

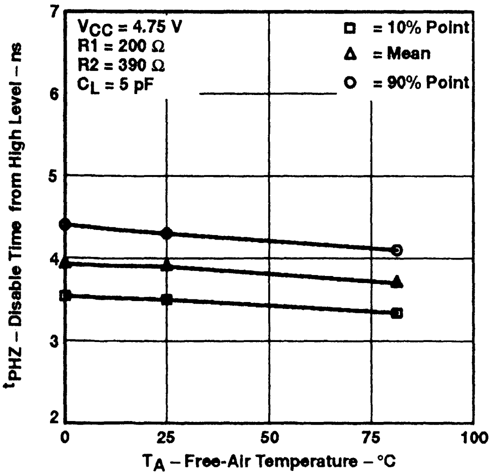
PROPAGATION DELAY TIME
(t_{PLZ} from OE↓ to Q)
vs
FREE-AIR TEMPERATURE



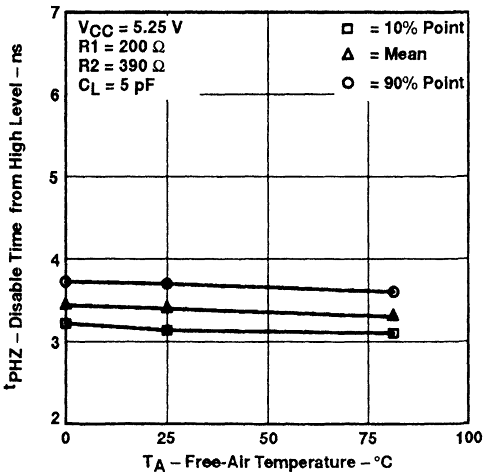
PROPAGATION DELAY TIME
(t_{PLZ} from OE↓ to Q)
vs
FREE-AIR TEMPERATURE



PROPAGATION DELAY TIME
(t_{PHZ} from OE↓ to Q)
vs
FREE-AIR TEMPERATURE

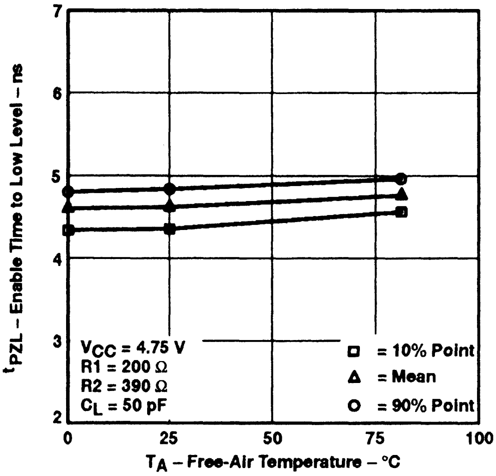


PROPAGATION DELAY TIME
(t_{PHZ} from OE↓ to Q)
vs
FREE-AIR TEMPERATURE

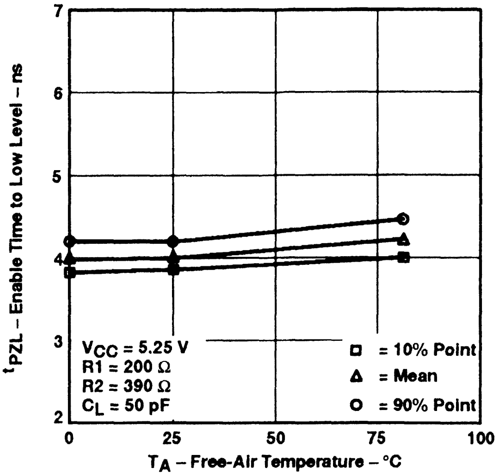


TIBPAL16R4-7C (continued)

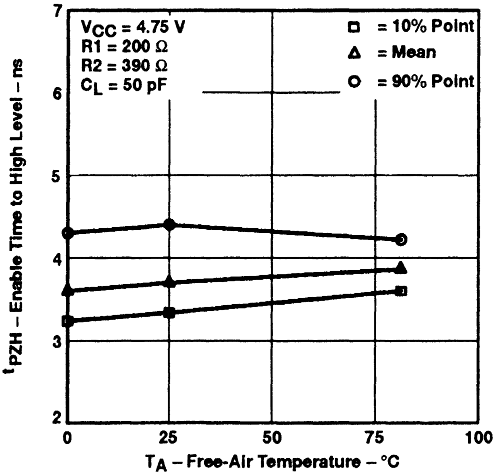
PROPAGATION DELAY TIME (t_{PZL} from OE↑ to Q) vs FREE-AIR TEMPERATURE



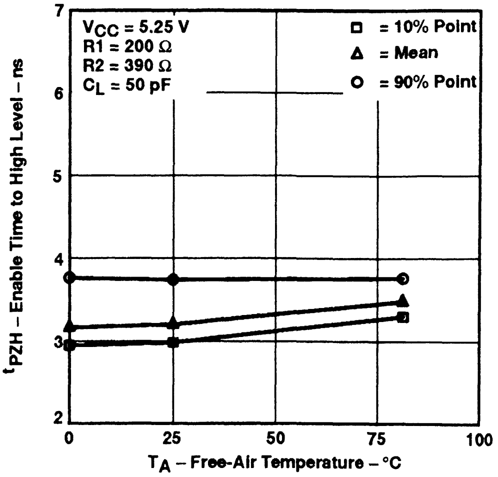
PROPAGATION DELAY TIME (t_{PZL} from OE↑ to Q) vs FREE-AIR TEMPERATURE



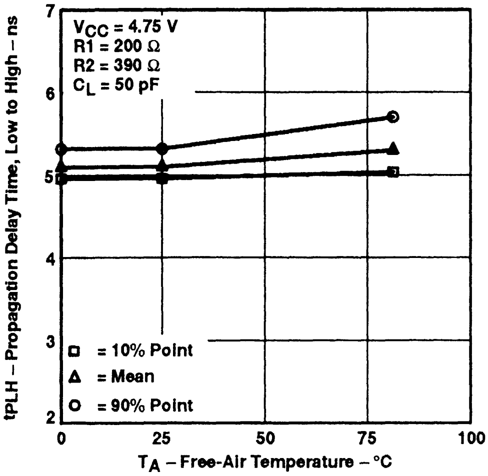
PROPAGATION DELAY TIME (t_{PZH} from OE↑ to Q) vs FREE-AIR TEMPERATURE



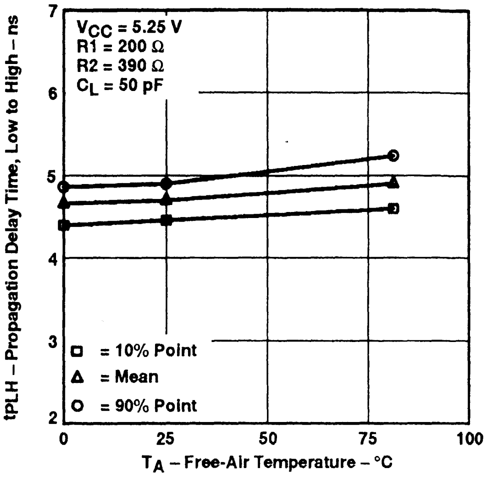
PROPAGATION DELAY TIME (t_{PZH} from OE↑ to Q) vs FREE-AIR TEMPERATURE



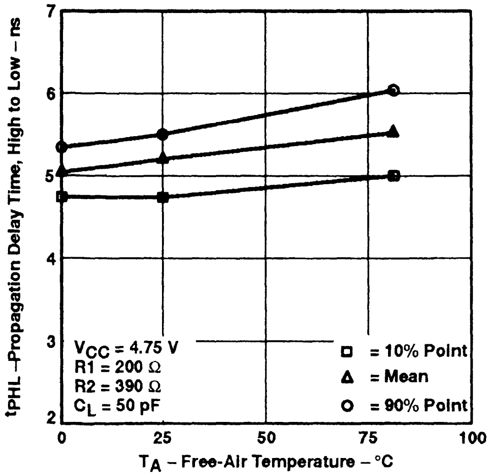
PROPAGATION DELAY TIME
(t_{PLH} from I, I/O to I/O)
vs
FREE-AIR TEMPERATURE



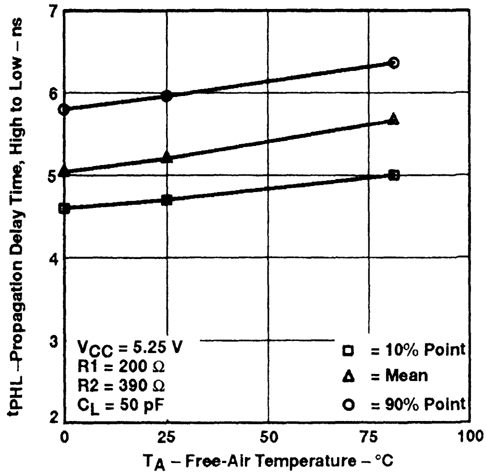
PROPAGATION DELAY TIME
(t_{PLH} from I, I/O to I/O)
vs
FREE-AIR TEMPERATURE



PROPAGATION DELAY TIME
(t_{PHL} from I, I/O to I/O)
vs
FREE-AIR TEMPERATURE

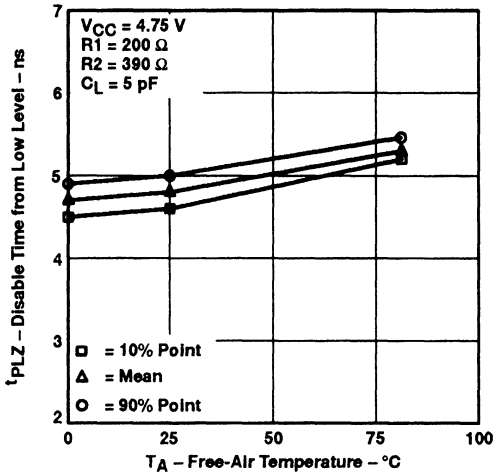


PROPAGATION DELAY TIME
(t_{PHL} from I, I/O to I/O)
vs
FREE-AIR TEMPERATURE

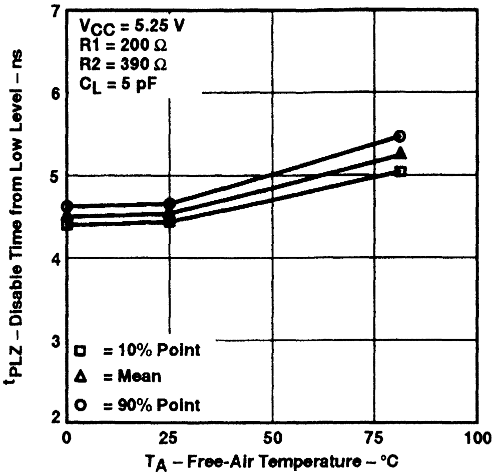


TIBPAL16R6-7C (continued)

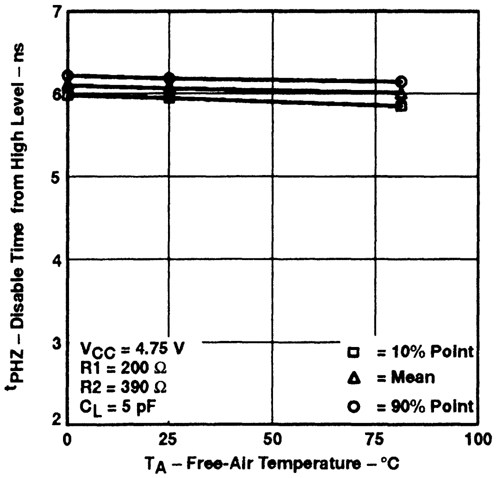
PROPAGATION DELAY TIME
(t_{PLZ} from I, I/O to I/O)
vs
FREE-AIR TEMPERATURE



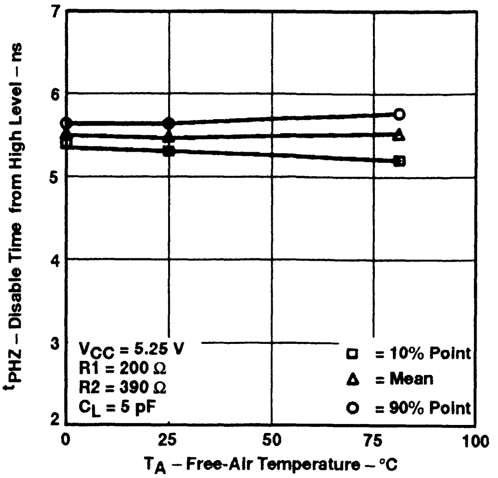
PROPAGATION DELAY TIME
(t_{PLZ} from I, I/O to I/O)
vs
FREE-AIR TEMPERATURE



PROPAGATION DELAY TIME
(t_{PHZ} from I, I/O to I/O)
vs
FREE-AIR TEMPERATURE

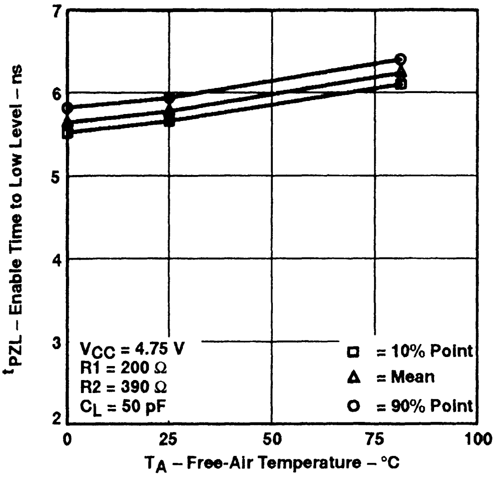


PROPAGATION DELAY TIME
(t_{PHZ} from I, I/O to I/O)
vs
FREE-AIR TEMPERATURE

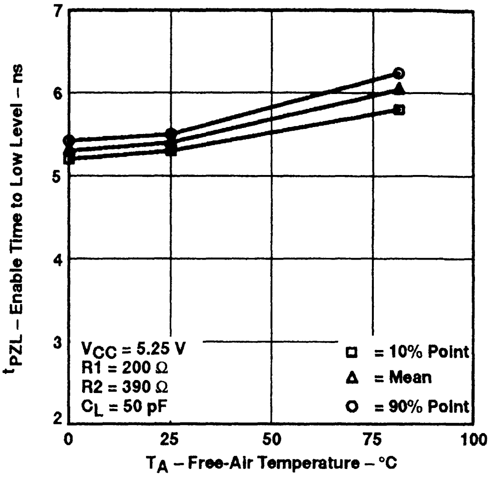


TIBPAL16R6-7C (continued)

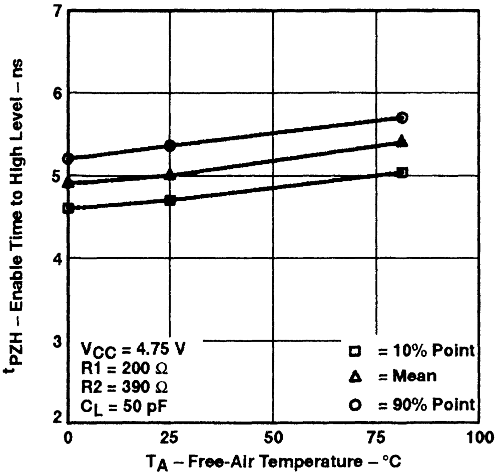
PROPAGATION DELAY TIME (t_{PZL} from I, I/O to I/O) vs FREE-AIR TEMPERATURE



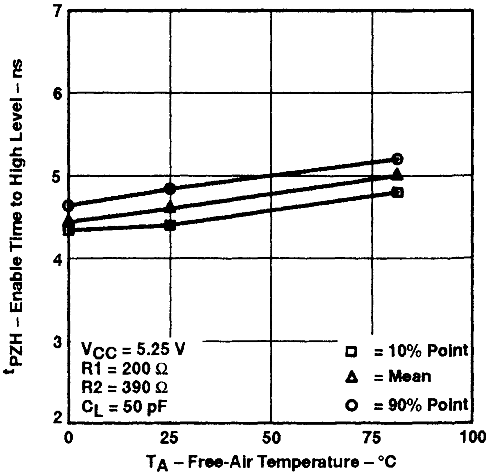
PROPAGATION DELAY TIME (t_{PZL} from I, I/O to I/O) vs FREE-AIR TEMPERATURE



PROPAGATION DELAY TIME (t_{PZH} from I, I/O to I/O) vs FREE-AIR TEMPERATURE

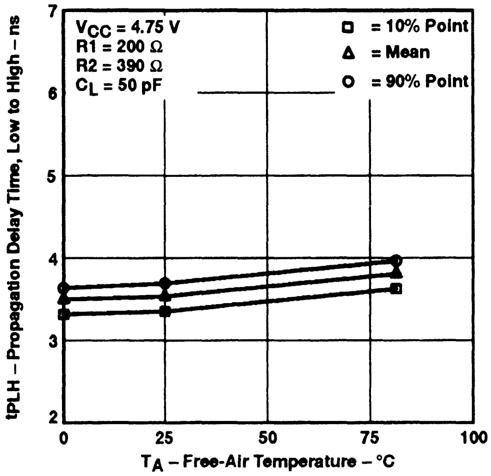


PROPAGATION DELAY TIME (t_{PZH} from I, I/O to I/O) vs FREE-AIR TEMPERATURE

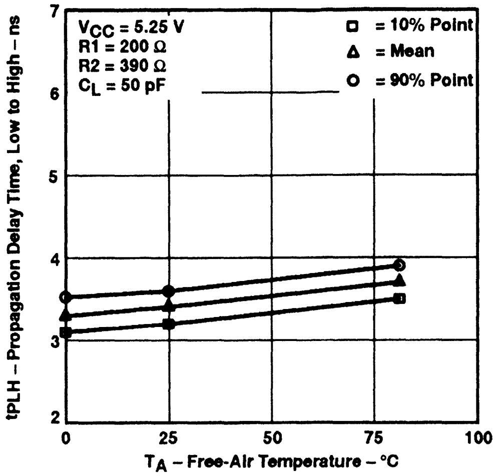


TIBPAL16R6-7C (continued)

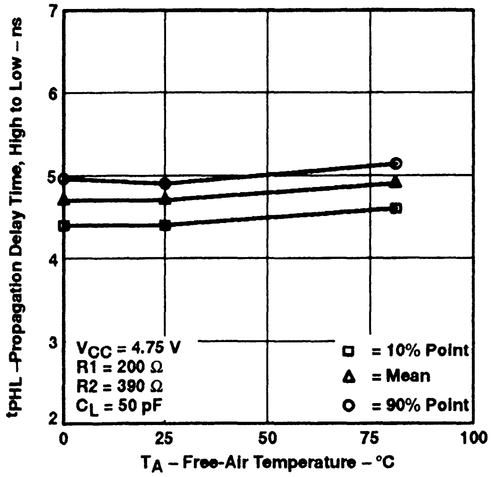
PROPAGATION DELAY TIME
(t_{PLH} from CLK to Q)
vs
FREE-AIR TEMPERATURE



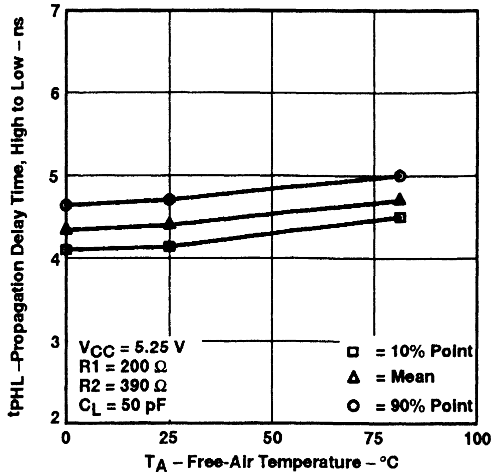
PROPAGATION DELAY TIME
(t_{PLH} from CLK to Q)
vs
FREE-AIR TEMPERATURE



PROPAGATION DELAY TIME
(t_{PHL} from CLK to Q)
vs
FREE-AIR TEMPERATURE

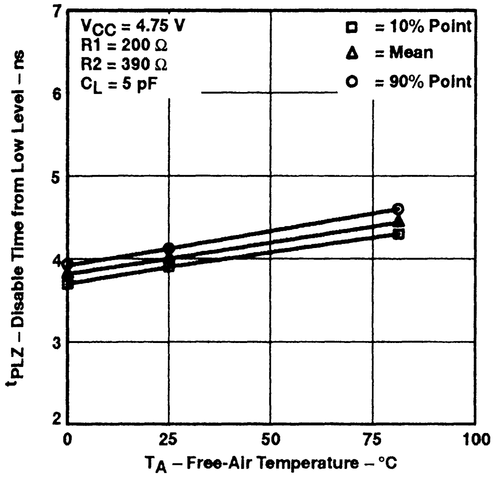


PROPAGATION DELAY TIME
(t_{PHL} from CLK to Q)
vs
FREE-AIR TEMPERATURE

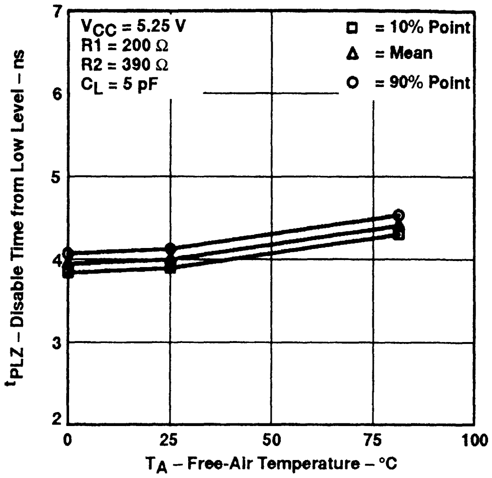


TIBPAL16R6-7C (continued)

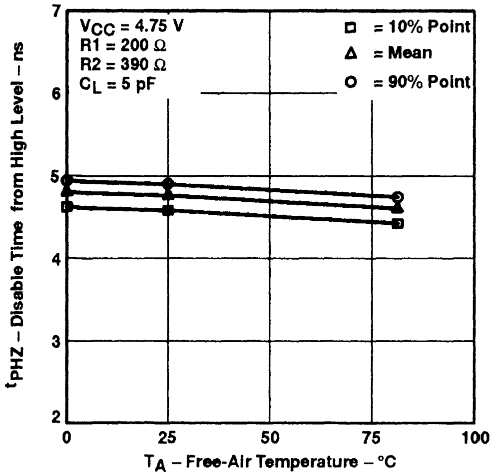
PROPAGATION DELAY TIME
(t_{PLZ} from OE↓ to Q)
vs
FREE-AIR TEMPERATURE



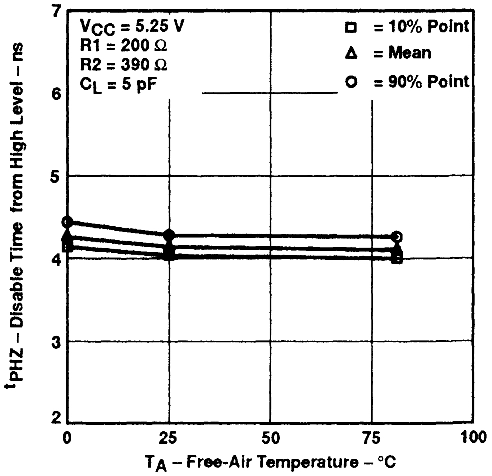
PROPAGATION DELAY TIME
(t_{PLZ} from OE↓ to Q)
vs
FREE-AIR TEMPERATURE



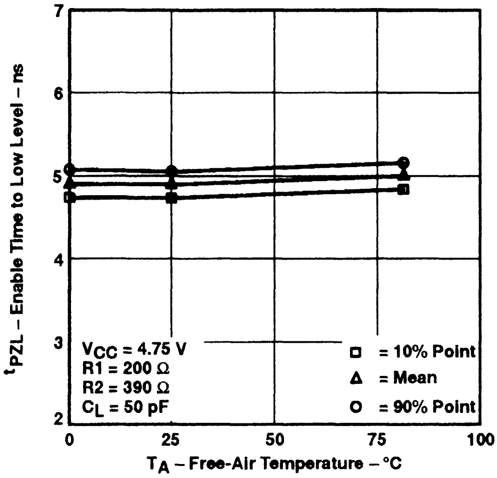
PROPAGATION DELAY TIME
(t_{PHZ} from OE↓ to Q)
vs
FREE-AIR TEMPERATURE

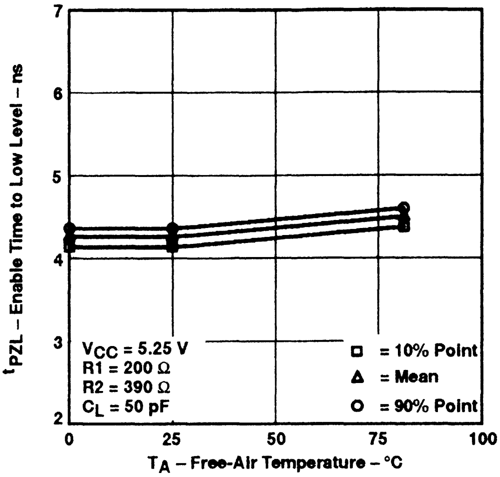


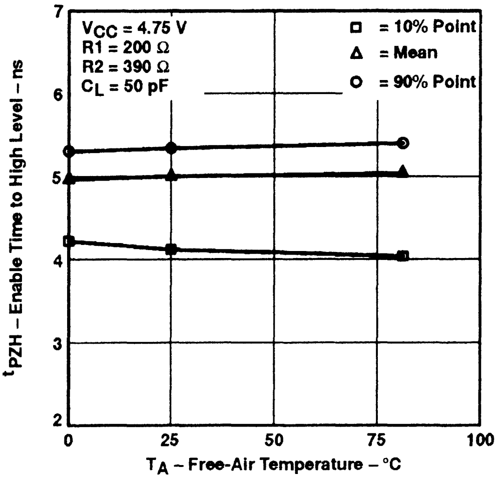
PROPAGATION DELAY TIME
(t_{PHZ} from OE↓ to Q)
vs
FREE-AIR TEMPERATURE

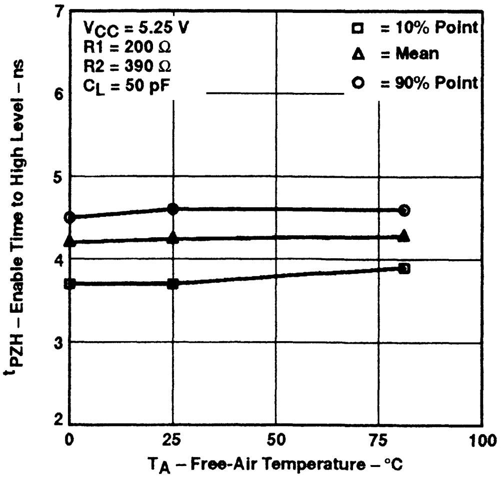


TIBPAL16R6-7C (continued)

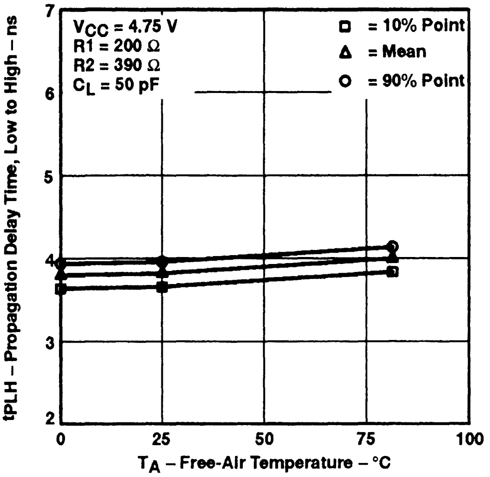

PROPAGATION DELAY TIME
(t_{PZL} from OE↑ to Q)
vs
FREE-AIR TEMPERATURE


PROPAGATION DELAY TIME
(t_{PZL} from OE↑ to Q)
vs
FREE-AIR TEMPERATURE

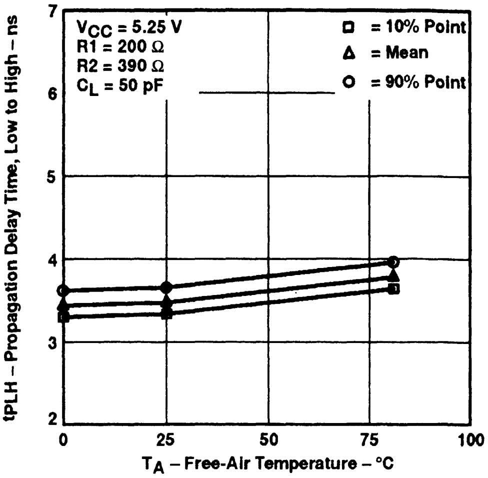

PROPAGATION DELAY TIME
(t_{PZH} from OE↑ to Q)
vs
FREE-AIR TEMPERATURE


PROPAGATION DELAY TIME
(t_{PZH} from OE↑ to Q)
vs
FREE-AIR TEMPERATURE

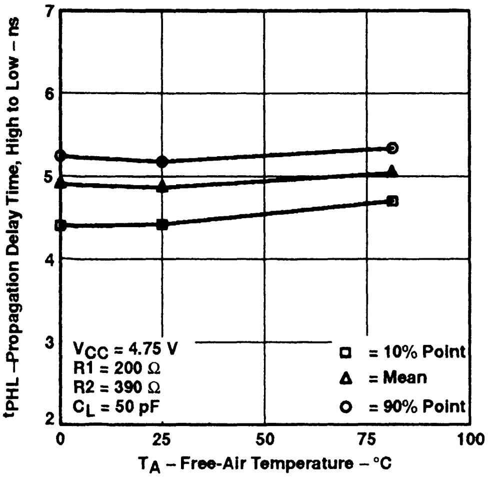
PROPAGATION DELAY TIME
(t_{PLH} from CLK to Q)
vs
FREE-AIR TEMPERATURE



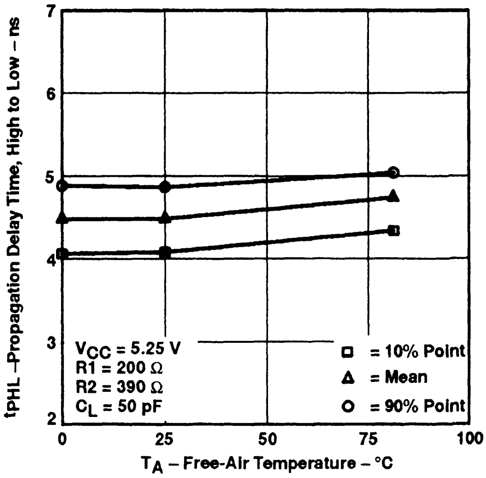
PROPAGATION DELAY TIME
(t_{PLH} from CLK to Q)
vs
FREE-AIR TEMPERATURE



PROPAGATION DELAY TIME
(t_{PHL} from CLK to Q)
vs
FREE-AIR TEMPERATURE

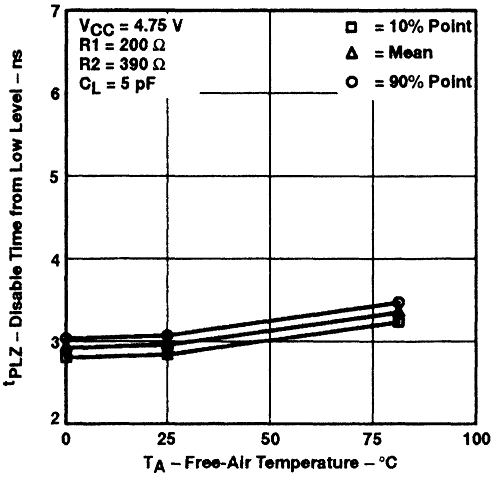


PROPAGATION DELAY TIME
(t_{PHL} from CLK to Q)
vs
FREE-AIR TEMPERATURE

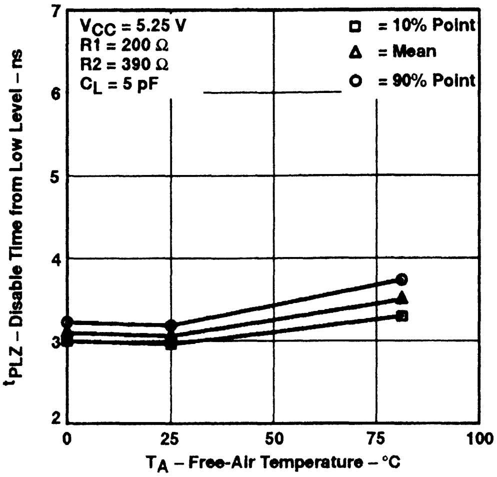


TIBPAL16R8-7C (continued)

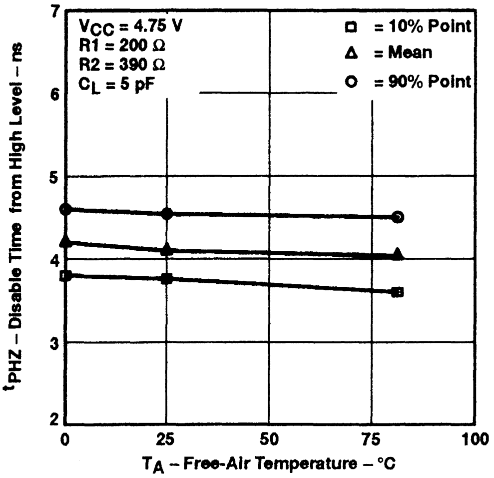
PROPAGATION DELAY TIME
(t_{PLZ} from OE↓ to Q)
vs
FREE-AIR TEMPERATURE



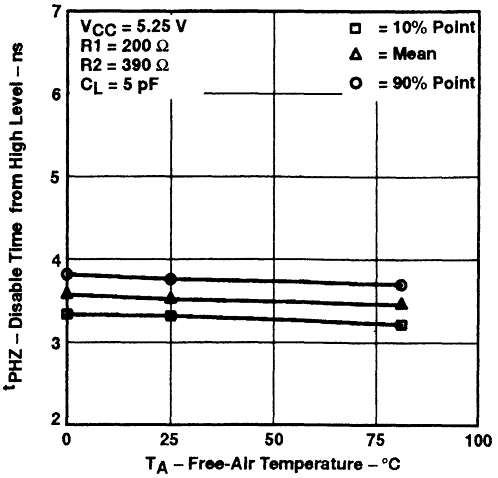
PROPAGATION DELAY TIME
(t_{PLZ} from OE↓ to Q)
vs
FREE-AIR TEMPERATURE



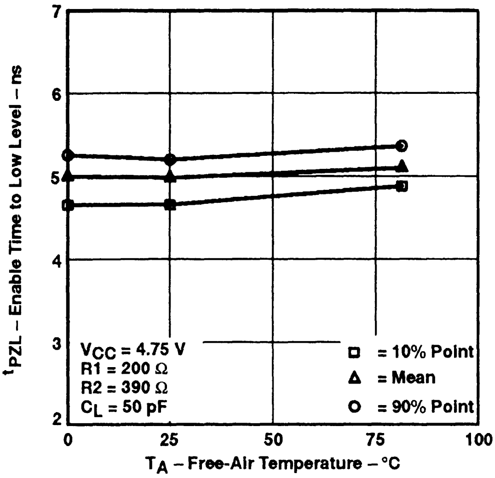
PROPAGATION DELAY TIME
(t_{PHZ} from OE↓ to Q)
vs
FREE-AIR TEMPERATURE

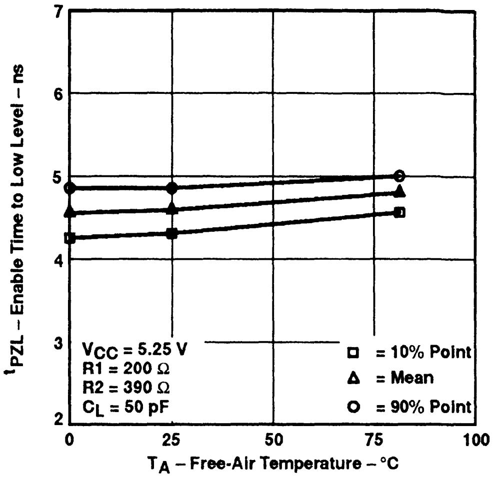


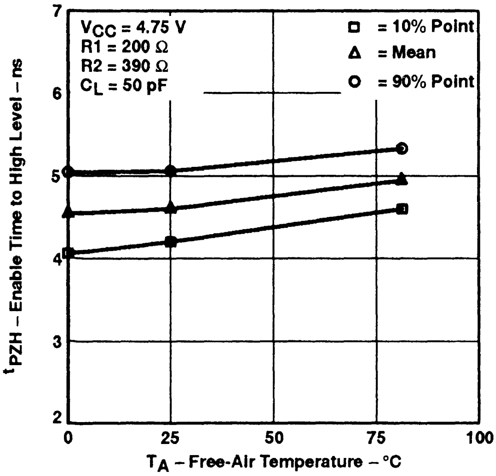
PROPAGATION DELAY TIME
(t_{PHZ} from OE↓ to Q)
vs
FREE-AIR TEMPERATURE

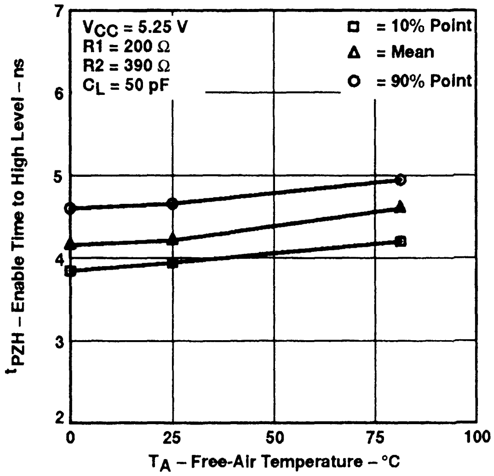


TIBPAL16R8-7C (continued)

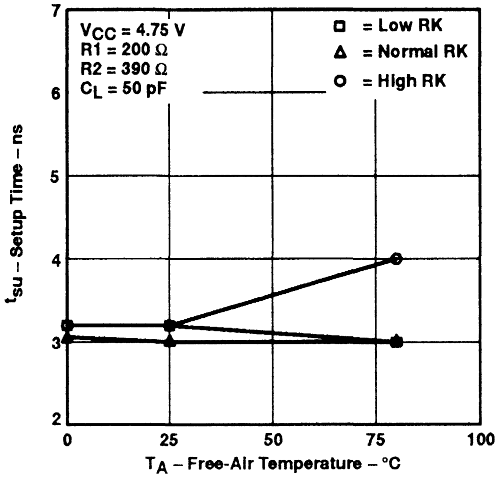

PROPAGATION DELAY TIME
(t_{PZL} from OE↑ to Q)
vs
FREE-AIR TEMPERATURE


PROPAGATION DELAY TIME
(t_{PZL} from OE↑ to Q)
vs
FREE-AIR TEMPERATURE

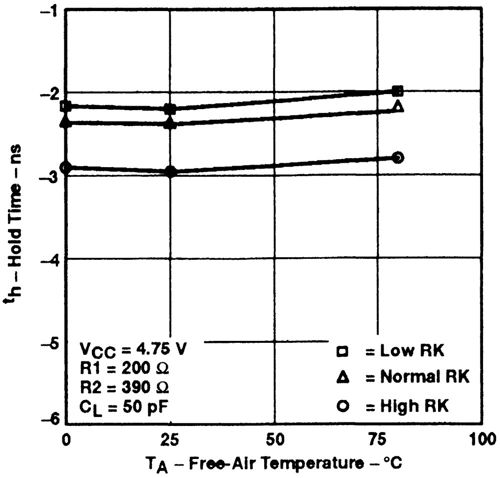

PROPAGATION DELAY TIME
(t_{PZH} from OE↑ to Q)
vs
FREE-AIR TEMPERATURE


PROPAGATION DELAY TIME
(t_{PZH} from OE↑ to Q)
vs
FREE-AIR TEMPERATURE

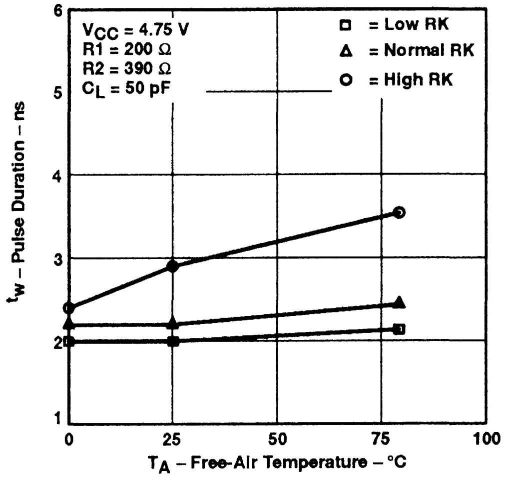
SETUP TIME
(Input or feedback before CLK ↑)
vs
FREE-AIR TEMPERATURE



HOLD TIME
(Input or feedback after CLK ↑)
vs
FREE-AIR TEMPERATURE



PULSE DURATION
(High or Low)
vs
FREE-AIR TEMPERATURE



20-pin 10-ns IMPACT-X PLDs

Devices included in this section:

TIBPAL16L8-10C
TIBPAL16R4-10C
TIBPAL16R6-10C
TIBPAL16R8-10C

DEVICE INFORMATION

20-pin 10-ns IMPACT-X PLDs

1. Technology .... IMPACT-X
2. Package Types : .... 20-pin plastic DIP,
   20-pin plastic PLCC
3. Last Die Revision .... X (None)
4. Bar Size .... 93 x 90 mils
5. Still Air Thermal Impedance :

	PDIP	**PLCC**
$R_{\theta JA}$	66.7	105.1
$R_{\theta JC}$	28.7	29.4

6. $R_{\theta JA}$ with Air Flow :

FPM	**PDIP**	**PLCC**
0	87.5	103.5
100	75.5	82.2
250	61.0	64.6
500	48.3	51.7
750	42.6	
1000	40.3	

QUALIFICATION INFORMATION

The TIBPAL16XX-10 devices were qualified in 1986 before the previously mentioned standards were incorporated. These devices are however included in the reliability monitors which requires the same level of quality and reliability as the newer products. The following summaries give the required tests and results for each device and any additional test performed for additional data.

Required Tests and Results for TIBPAL16XX-10

Device Type:	16R4-10
Package Type:	20 pin PDIP
Die Lot Number:	6340945

TEST	SS/F	ENDPOINT	RESULTS
125°C Static Op-Life	128/1	1000 HRS	128/0
125°C Dynamic Op-Life	127/1	1000 HRS	127/0
85°C/85% RH	129/1	1000 HRS	129/0
–65°C/150°C Temp Cycle	128/1	1000 CYC	128/0
Autoclave	77/1	240 HRS	77/1[1]
ESD	21/0	2000 V	21/0

Additional Qualification Tests and Results for TIBPAL16XX-10

Device Types:	16R4-10 and16R8-10
Package Type:	20 pin PDIP
Die Lot Numbers:	7014316 and 7043816

TEST	SS/F	ENDPOINT	RESULTS
125°C Static Op-Life	129/1	1000 HRS	129/1[1]
125°C Dynamic Op-Life	129/1	1000 HRS	129/0
85°C/85% RH	129/1	1000 HRS	129/0
–65°C/150°C Temp Cycle	129/1	1000 CYC	129/0
Autoclave	77/1	240 HRS	77/0
ESD	21/0	2000 V	21/0

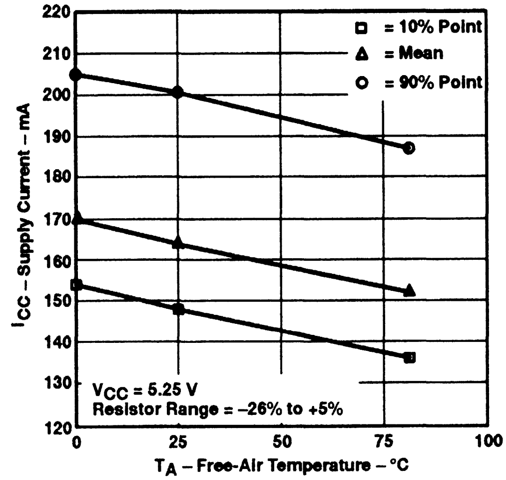
1. Input leakage, failure mode unresolved.

CHARACTERIZATION INFORMATION

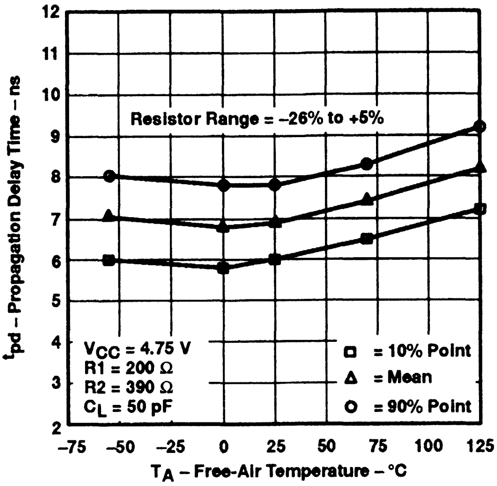
TIBPAL16L8-10
TIBPAL16R4-10
TIBPAL16R6-10
TIBPAL16R8-10

TIBPAL16L8-10

SUPPLY CURRENT
(Virgin Device)
vs
FREE-AIR TEMPERATURE

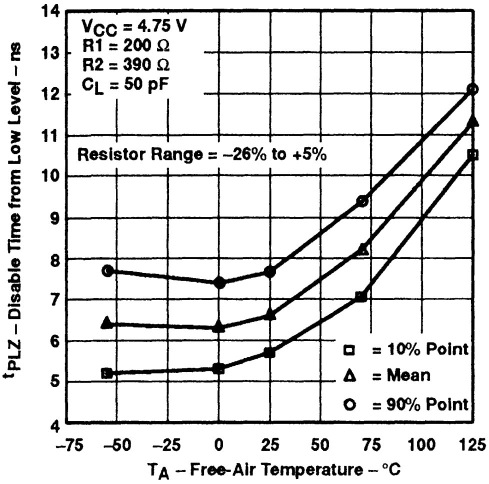


PROPAGATION DELAY TIME
(I, I/O to O, I/O)
vs
FREE-AIR TEMPERATURE

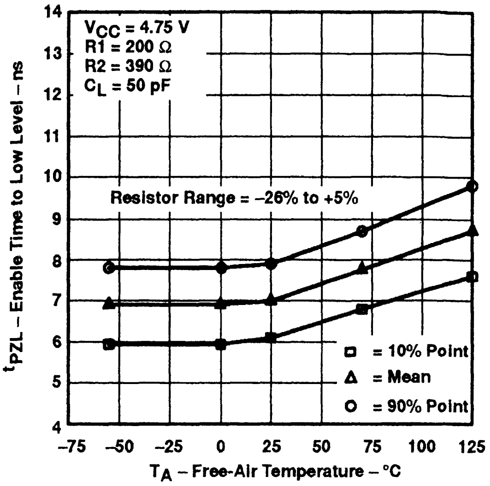


TIBPAL16L8-10 (continued)

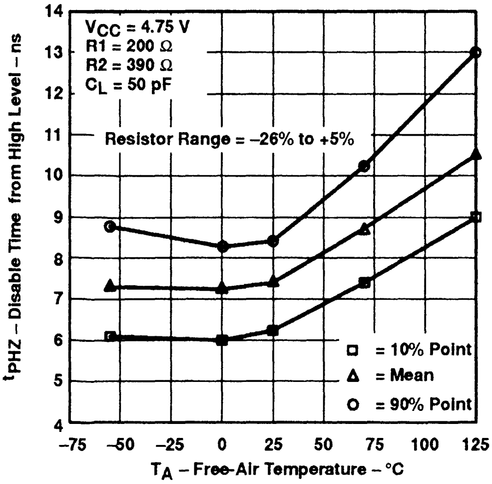
DISABLE TIME
(t_{PLZ} from I, I/O to O, I/O)
vs
FREE-AIR TEMPERATURE



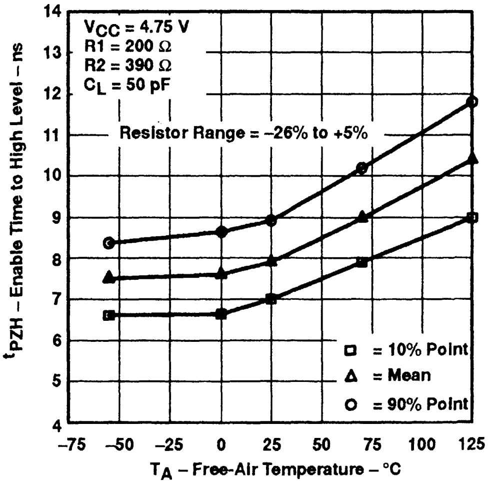
ENABLE TIME
(t_{PZL} from I, I/O to O, I/O)
vs
FREE-AIR TEMPERATURE



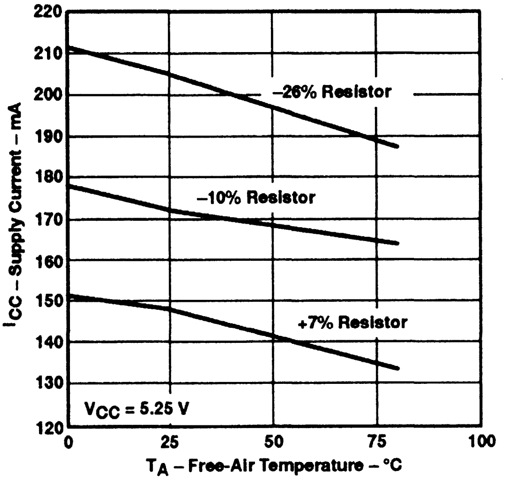
DISABLE TIME
(t_{PHZ} from I, I/O to O, I/O)
vs
FREE-AIR TEMPERATURE



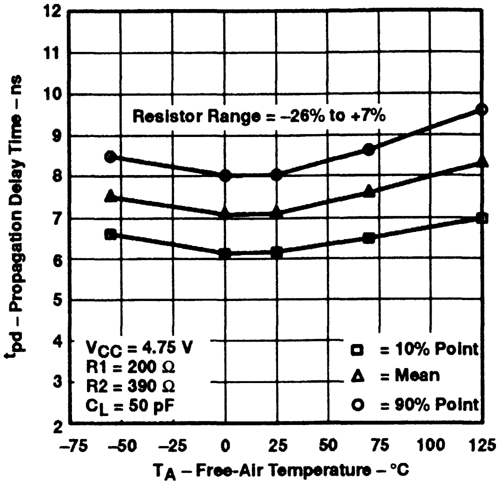
ENABLE TIME
(t_{PZH} from I, I/O to O, I/O)
vs
FREE-AIR TEMPERATURE



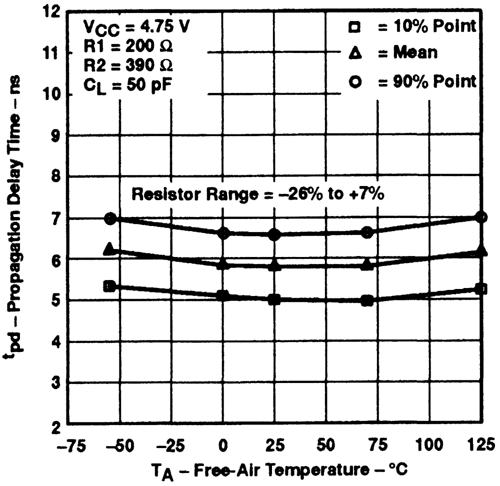
SUPPLY CURRENT
(Virgin Device)
vs
FREE-AIR TEMPERATURE



PROPAGATION DELAY TIME
(I, I/O to O, I/O)
vs
FREE-AIR TEMPERATURE

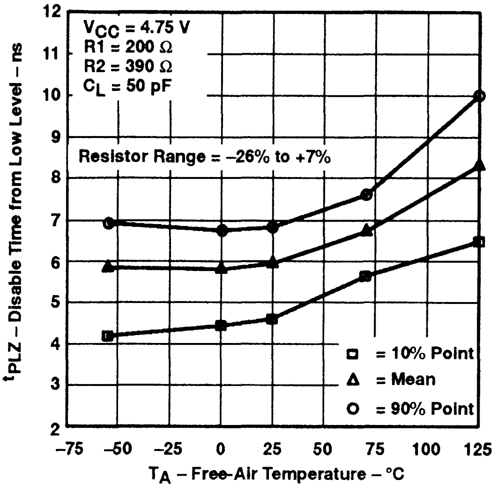


PROPAGATION DELAY TIME
(CLK to Q)
vs
FREE-AIR TEMPERATURE

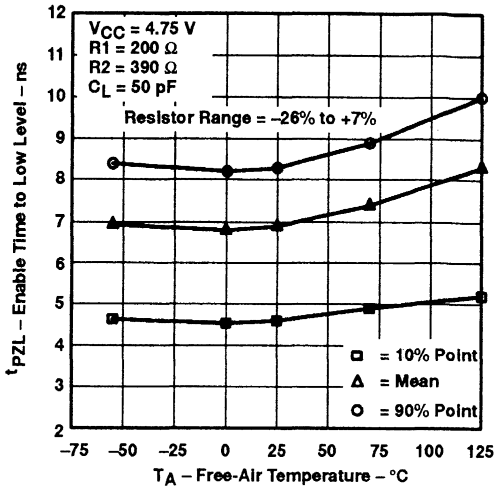


TIBPAL16R4-10 (continued)

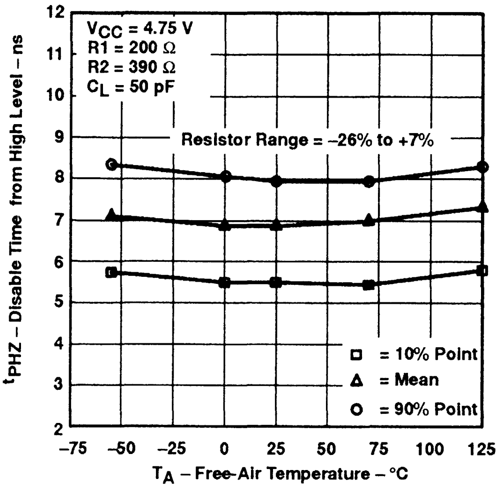
DISABLE TIME
(t_{PLZ} from I, I/O to O, I/O)
vs
FREE-AIR TEMPERATURE



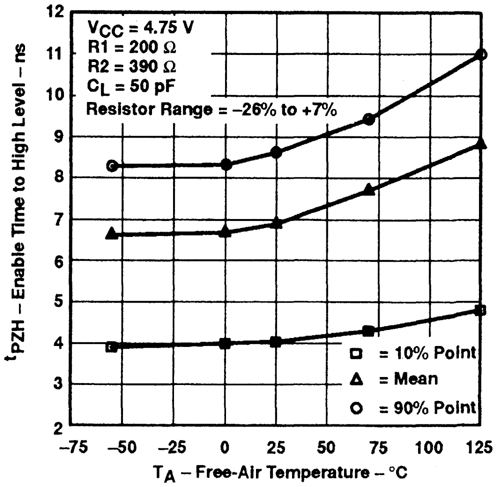
ENABLE TIME
(t_{PZL} from I, I/O to O, I/O)
vs
FREE-AIR TEMPERATURE



DISABLE TIME
(t_{PHZ} from I, I/O to O, I/O)
vs
FREE-AIR TEMPERATURE

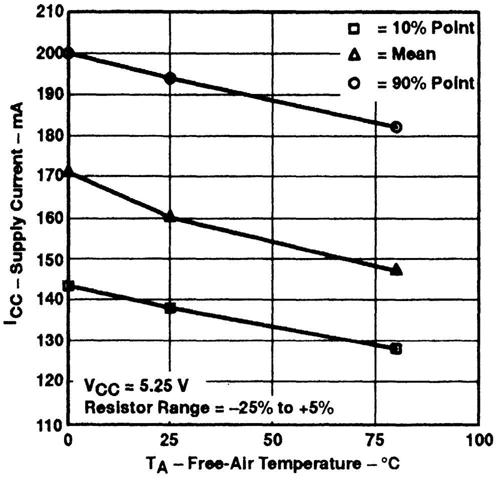


ENABLE TIME
(t_{PZH} from I, I/O to O, I/O)
vs
FREE-AIR TEMPERATURE

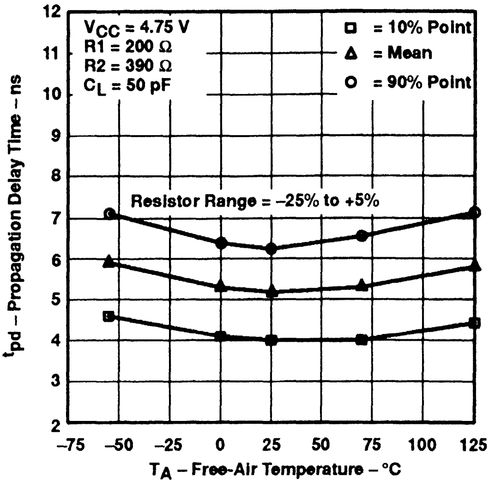


TIBPAL16R8-10

SUPPLY CURRENT (Virgin Device) vs FREE-AIR TEMPERATURE

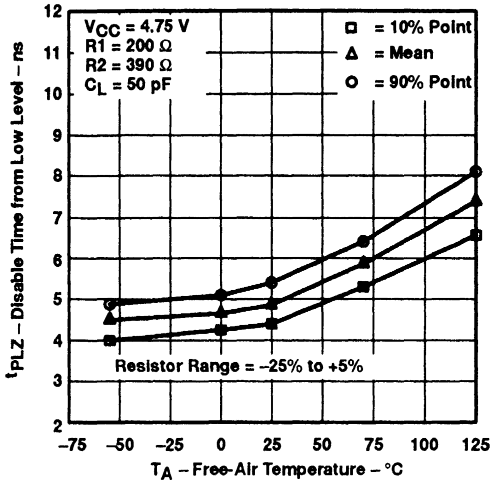


PROPAGATION DELAY TIME (CLK to Q) vs FREE-AIR TEMPERATURE

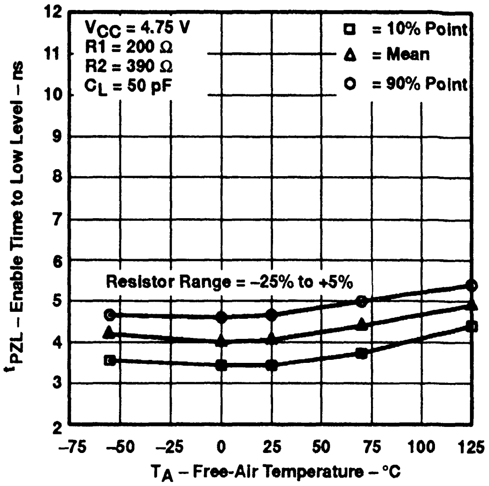


TIBPAL16R8-10 (continued)

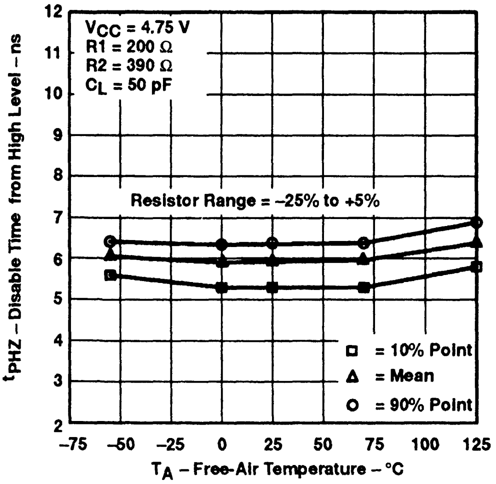
DISABLE TIME
(t_{PLZ} from $\overline{OE}$↑ to Q)
vs
FREE-AIR TEMPERATURE



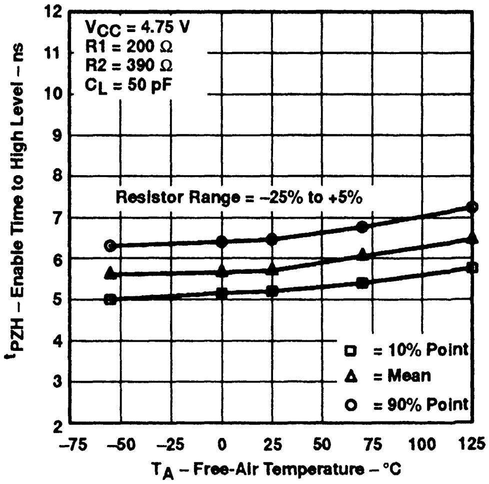
ENABLE TIME
(t_{PZL} from $\overline{OE}$↓ to Q)
vs
FREE-AIR TEMPERATURE



DISABLE TIME
(t_{PHZ} from $\overline{OE}$↑ to Q)
vs
FREE-AIR TEMPERATURE



ENABLE TIME
(t_{PZH} from $\overline{OE}$↓ to Q)
vs
FREE-AIR TEMPERATURE



24-pin 5-ns IMPACT-X PLDs

Devices included in this section:

TIBPAL20L8-5C
TIBPAL20R4-5C
TIBPAL20R6-5C
TIBPAL20R8-5C

DEVICE INFORMATION
24-pin 5-ns IMPACT-X PLDs

1. Technology .... IMPACT-X
2. Package Types : .... 20-pin plastic DIP,
   20-pin plastic PLCC
3. Last Die Revision .... X (none)
4. Bar Size : .... 20L8 : 85 x 107 mils
   20R4 : 93 x 107 mils
   20R6 : 93 x 107 mils
   20R8 : 93 x 107 mils
5. Still Air Thermal Impedance :

	PDIP	PLCC
$R_{\theta JA}$	71.5	84.8
$R_{\theta JC}$	31.2	26.7

6. $R_{\theta JA}$ with Air Flow :

FPM	PDIP	PLCC
0	82.6	92.9
100	62.8	69.6
250	46.3	61.0
500	37.6	50.1
750		44.2
1000		41.0

QUALIFICATION INFORMATION

The TIBPAL20XX-5 devices are qualified using the accelerated qualification program.The following summaries give the required tests and results for each device and any additional test performed for additional data. With this particular device family, the TIBPAL16XX and the TIBPAL20XX parts are essentially the same die so the data for these two families are the same.

16L8-5 and 20L8-5

Required Tests and Results for TIBPAL16L8-5 and TIBPAL20L8-5

Device Type:	20L8-5
Package Type:	24 pin PDIP
Date Code:	944XF
Die Lot Number:	361

TEST	SS/F	ENDPOINT	RESULTS	EXTENDED READPOINT	RESULTS
150°C Dynamic Op-Life	129/1	416 HRS	129/0		
125°C Dynamic Op-Life	129/1	168 HRS	128/0[1]	1000 HRS	128/0
130°C/85% RH HAST	76/0	500 HRS	76/0		
–65°C/150°C Thermal Shock	129/1	500 CYC	129/0		
ESD	3/0	2000 V	3/0		

Additional Qualification Tests and Results for TIBPAL16L8-5 and TIBPAL20L8-5

Device Type:	20L8-5
Package Type:	24 pin PDIP
Date Code:	009XF
Die Lot Numbers:	02332, 29314, and 35505

TEST	ENDPOINT	RESULTS
150°C Dynamic Op-Life	416 HRS	201/2[2]
125°C Dynamic Op-Life	1000 HRS	201/0
130°C/85% RH HAST	200 HRS	201/0
–65°C/150°C Thermal Shock	1000 CYC	201/0
ESD	2000 V	3/0

16R4-5 and 20R4-5

Required Tests and Results for TIBPAL16R4-5 and TIBPAL20R4-5

Device Type:	20R4-5
Package Type:	24 pin PDIP
Date Code:	048XF
Die Lot Number:	28933

Required Tests and Results for TIBPAL16R4-5 and TIBPAL20R4-5 (continued)

TEST	SS/F	ENDPOINT	RESULTS	EXTENDED READPOINT	RESULTS
125°C Dynamic Op-Life	129/1	1000 HRS	128/1[3]	2000 HRS	128/0
130°C/85% RH HAST	129/1	100 HRS	129/0		
–65°C/150°C Thermal Shock	129/1	1000 CYC	129/0		
ESD	3/0	2000 V	6/0		

16R6-5 and 20R6-5

Required Tests and Results for TIBPAL16R6-5 and TIBPAL20R6-5

Device Type:	20R6-5
Package Type:	24 pin PDIP
Date Code:	9122
Die Lot Number:	1127109

TEST	SS/F	ENDPOINT	RESULTS	EXTENDED READPOINT	RESULTS
125°C Dynamic Op-Life	129/1	1000 HRS	129/0		
130°C/85% RH HAST	129/1	100 HRS	127/0[4]		
–65°C/150°C Thermal Shock	129/1	1000 CYC	129/0		
–65°C/150°C Temp Cycle	129/1	1000 CYC	129/0		
ESD	3/0	2000 V	3/0		

16R8-5 and 20R8-5

Required Tests and Results for TIBPAL16R8-5 and TIBPAL20R8-5

Device Type:	20R8-5
Package Type:	24 pin PDIP
Date Code:	048XF
Die Lot Number:	0289233

TEST	SS/F	ENDPOINT	RESULTS	EXTENDED READPOINT	RESULTS
150°C Dynamic Op-Life	129/1	416 HRS	129/0	1000 HRS	129/0
125°C Dynamic Op-Life	129/1	168 HRS	129/0	1000 HRS	129/0
130°C/85% RH HAST	129/1	200 HRS	129/0		
–65°C/150°C Thermal Shock	129/1	200 CYC	129/0		
–65°C/150°C Temp Cycle	129/1	1000 CYC	129/0		
ESD	3/0	2000 V	3/0		
Autoclave	76/0	240 HRS	76/0		

Additional Qualification Tests and Results for TIBPAL16R8-5 and TIBPAL20R8-5

Device Type:	20R8-5
Package Type:	24 pin PDIP
Date Code:	106XF
Die Lot Numbers:	0289233, 0310676, and 1 011759

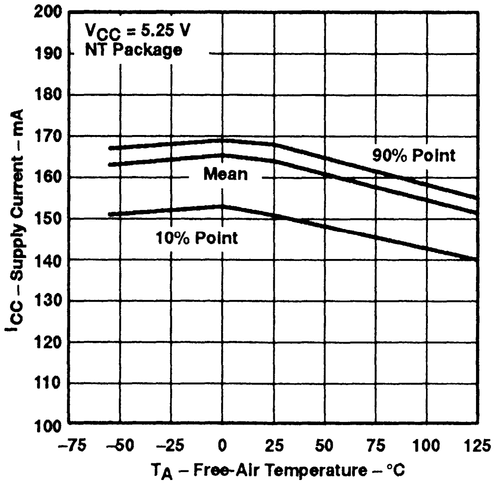
TEST	**ENDPOINT**	**RESULTS**
150°C Dynamic Op-Life	416 HRS	400/1[3]
125°C Dynamic Op-Life	1000 HRS	400/0
85°C/85% RH Biased Humidity	1000 HRS	201/0
–65°C/150°C Temp Cycle	1000 CYC	201/1[4]
ESD	2000 V	3/0

1. 1 unit received EOS damage due to reverse socket insertion - removed from population.
2. Failure determined to be caused by ESD/EOS, source unknown. TI FA Report # D12-00531
3. Failure determined to be caused by reverse socketing. TI FA Report # D12-00662
4. 2 units mechanically damaged beyond repair – unable to test – removed from sample.
5. Failure caused by mechanical damage of 1st level metal. TI FA Report # D13-00004
6. Failure analysis results conclude interlevel oxide crack caused metal-1 to metal-2 short. TI FA Report # D13-00010

CHARACTERIZATION INFORMATION

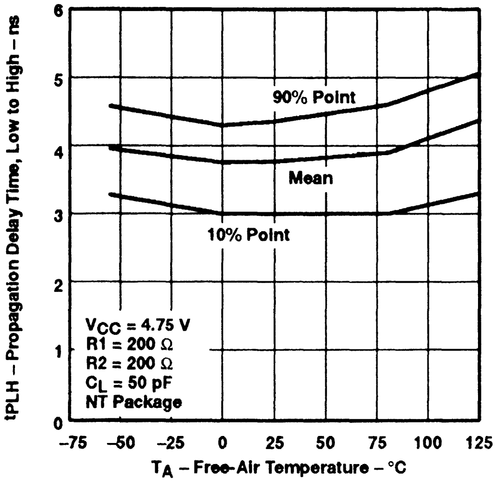
TIBPAL20L8-5C
TIBPAL20R8-5C

SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

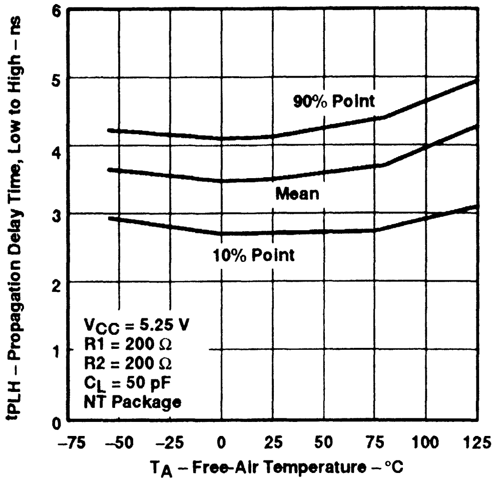


TIBPAL20L8-5C (continued)

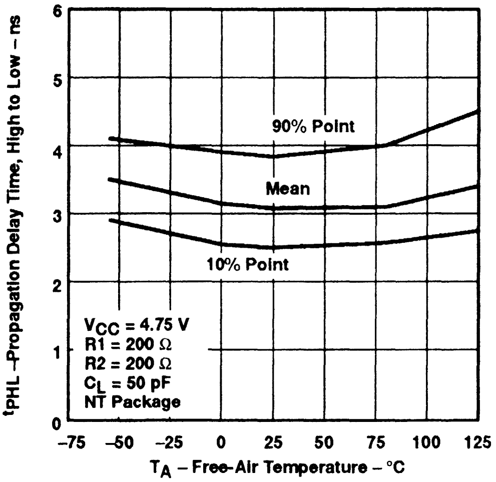
PROPAGATION DELAY TIME
(t_{PLH} from I, I/O to O, I/O)
vs
FREE-AIR TEMPERATURE



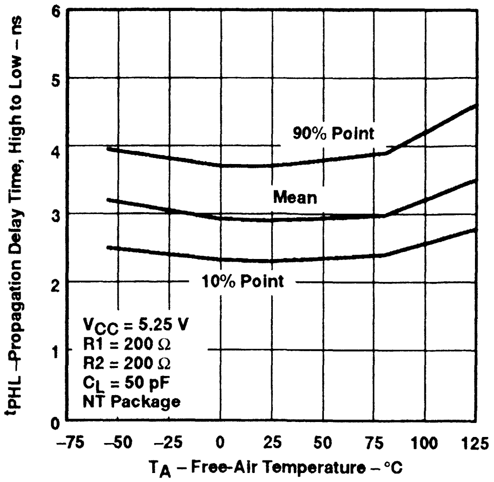
PROPAGATION DELAY TIME
(t_{PLH} from I, I/O to O, I/O)
vs
FREE-AIR TEMPERATURE



PROPAGATION DELAY TIME
(t_{PHL} from I, I/O to O, I/O)
vs
FREE-AIR TEMPERATURE

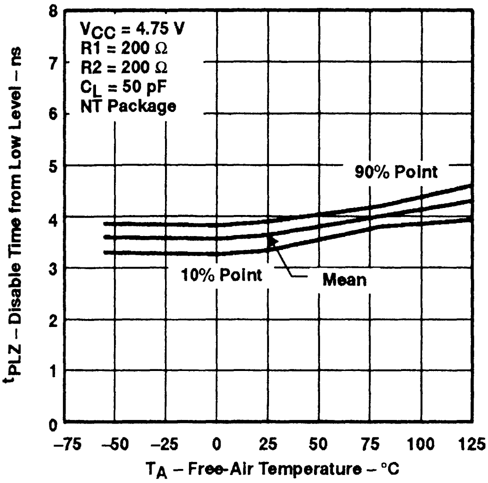


PROPAGATION DELAY TIME
(t_{PHL} from I, I/O to O, I/O)
vs
FREE-AIR TEMPERATURE

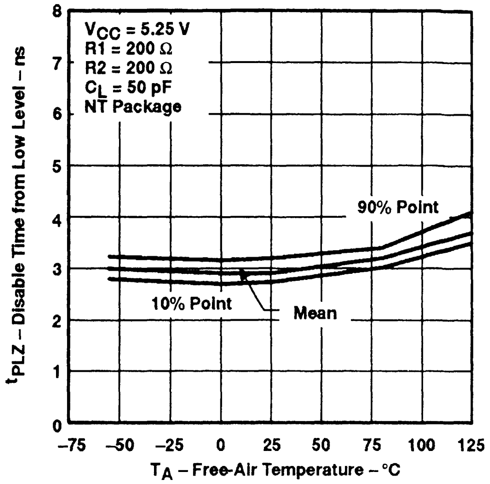


TIBPAL20L8-5C (continued)

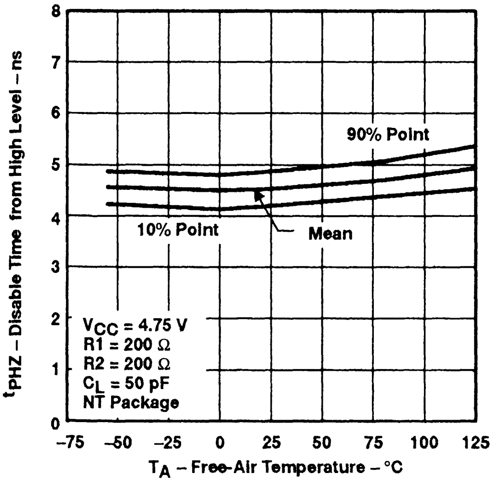
DISABLE TIME (t_{PLZ} from I, I/O to O, I/O) vs FREE-AIR TEMPERATURE



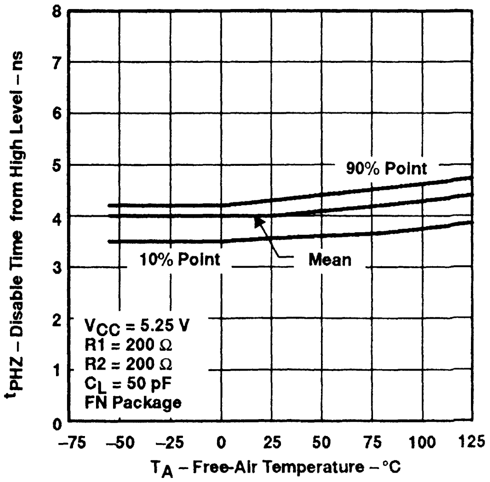
DISABLE TIME (t_{PLZ} from I, I/O to O, I/O) vs FREE-AIR TEMPERATURE



DISABLE TIME (t_{PHZ} from I, I/O to O, I/O) vs FREE-AIR TEMPERATURE

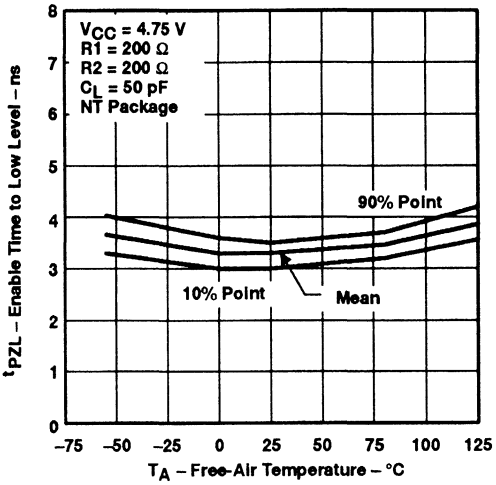


DISABLE TIME (t_{PHZ} from I, I/O to O, I/O) vs FREE-AIR TEMPERATURE

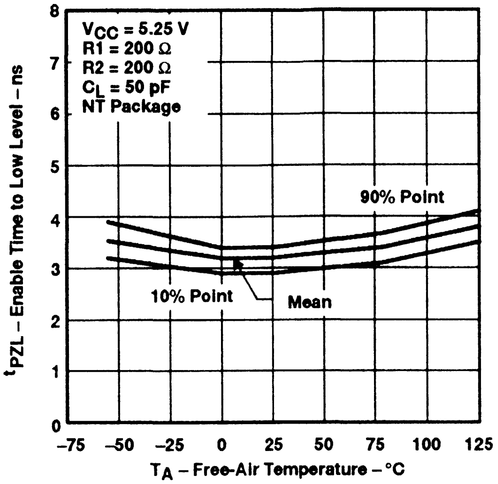


TIBPAL20L8-5C (continued)

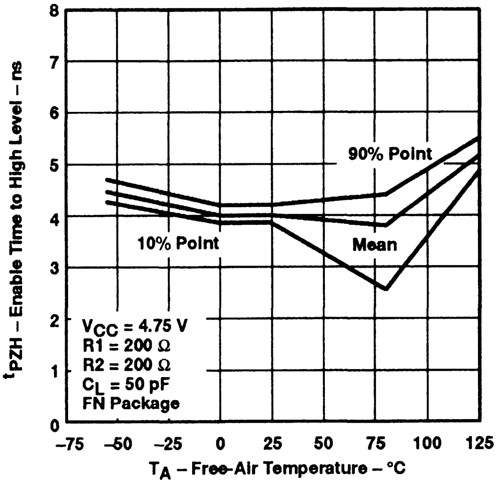
ENABLE TIME (t_{PZL} from I, I/O to O, I/O) vs FREE-AIR TEMPERATURE



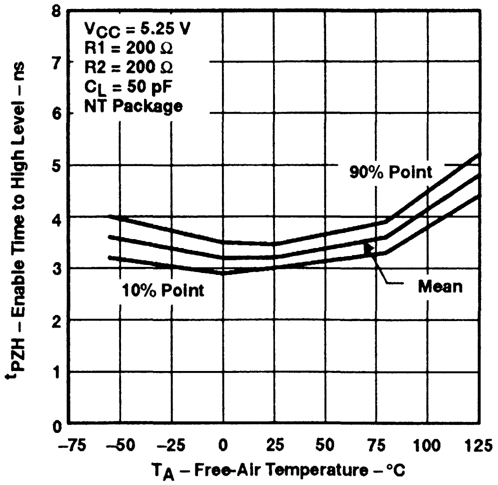
ENABLE TIME (t_{PZL} from I, I/O to O, I/O) vs FREE-AIR TEMPERATURE



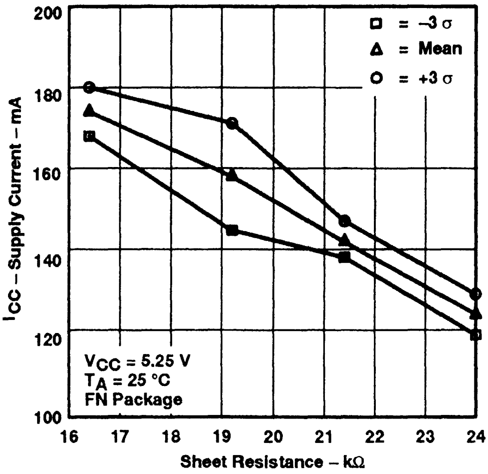
ENABLE TIME (t_{PZH} from I, I/O to O, I/O) vs FREE-AIR TEMPERATURE



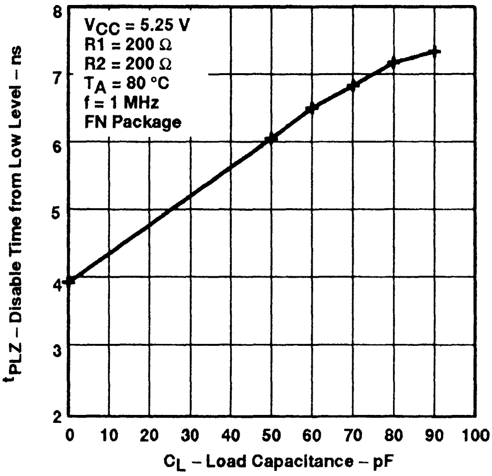
ENABLE TIME (t_{PZH} from I, I/O to O, I/O) vs FREE-AIR TEMPERATURE



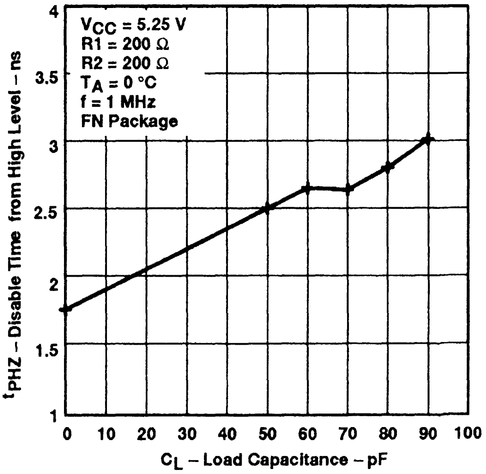
SUPPLY CURRENT
vs
SHEET RESISTANCE



DISABLE TIME (t_{PLZ})
$\overline{OE}$↑ to Q with 8 Outputs Switching in Phase
vs
LOAD CAPACITANCE

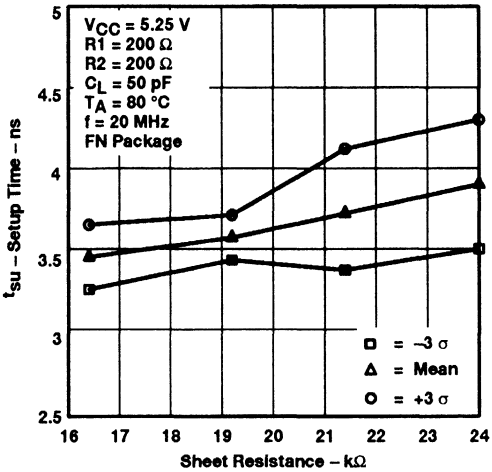


DISABLE TIME (t_{PHZ})
$\overline{OE}$↑ to Q with 1 Output Switching
vs
LOAD CAPACITANCE

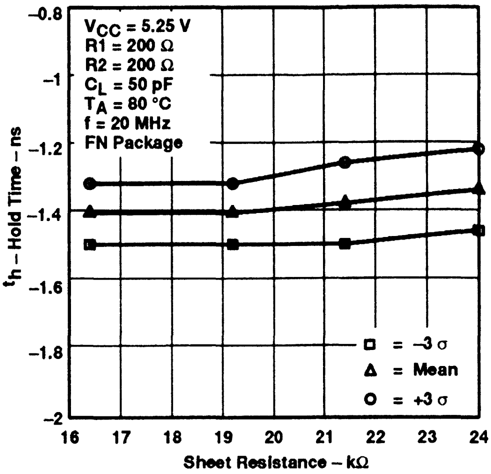


TIBPAL20R8-5C (continued)

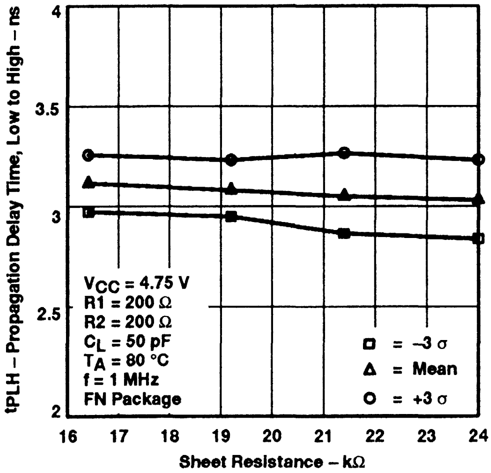
SETUP TIME (With 8 Outputs Switching In Alternate Direction) vs SHEET RESISTANCE



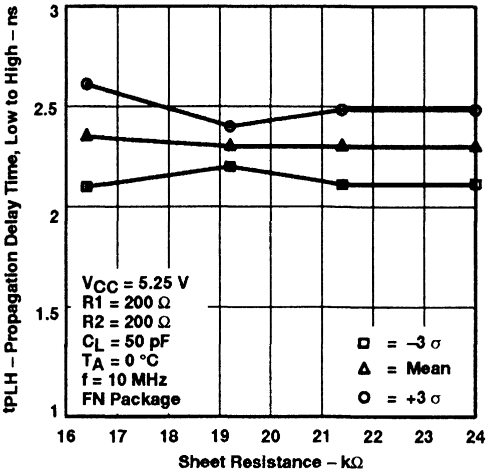
HOLD TIME (With 8 Outputs Switching In Same Direction) vs SHEET RESISTANCE



PROPAGATION DELAY TIME, CLK to Q (With 8 Outputs Switching In Same Direction) vs SHEET RESISTANCE

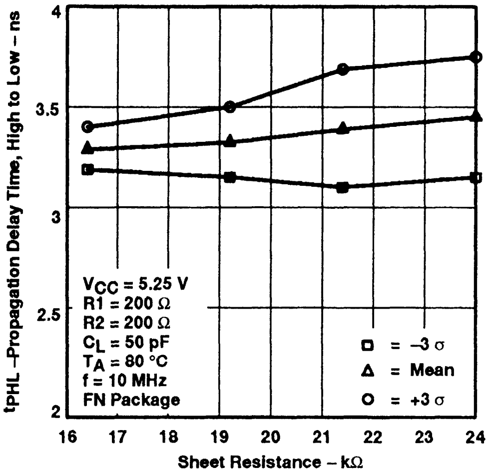


PROPAGATION DELAY TIME, CLK to Q (With 1 Output Switching) vs SHEET RESISTANCE

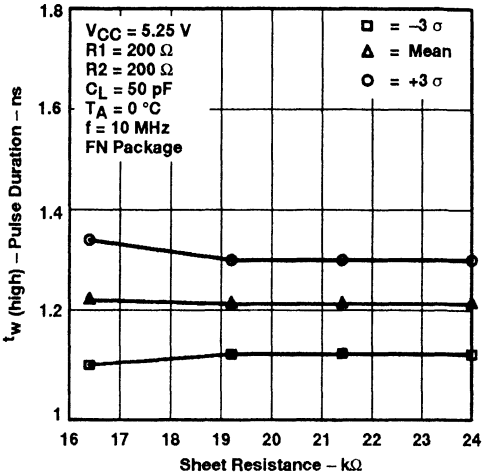


TIBPAL20R8-5C (continued)

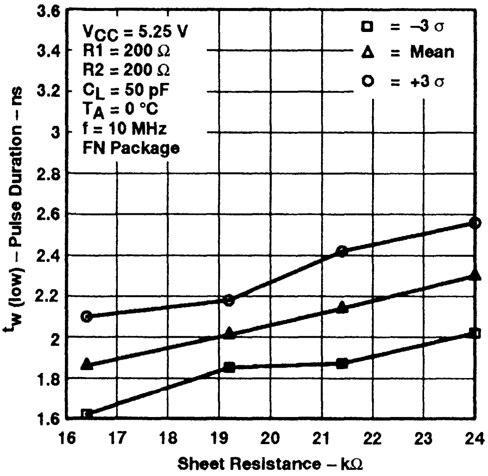
PROPAGATION DELAY TIME, CLK to Q
(With 8 Outputs Switching in Same Direction)
vs
SHEET RESISTANCE



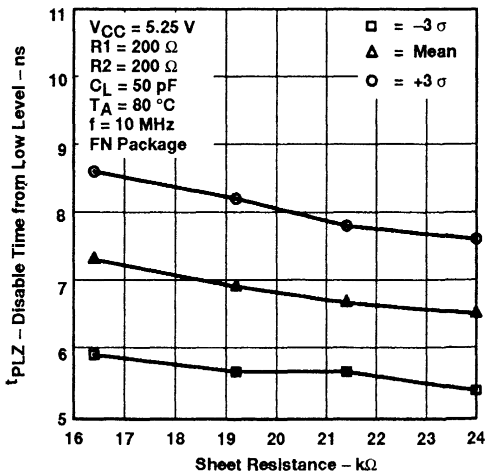
PULSE DURATION
(With 1 Output Switching)
vs
SHEET RESISTANCE



PULSE DURATION
(With 1 Output Switching)
vs
SHEET RESISTANCE

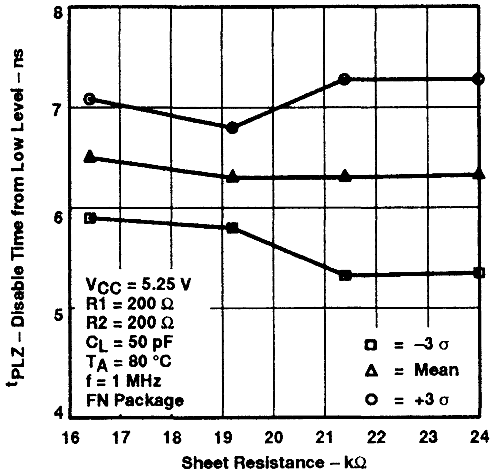


DISABLE TIME, $\overline{OE}$↑ to Q
(With 8 Outputs Switching in Same Direction)
vs
SHEET RESISTANCE

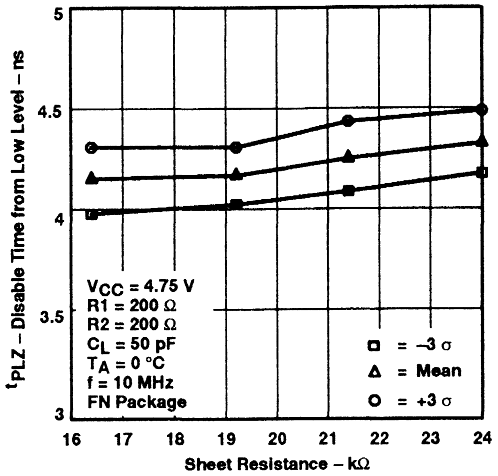


TIBPAL20R8-5C (continued)

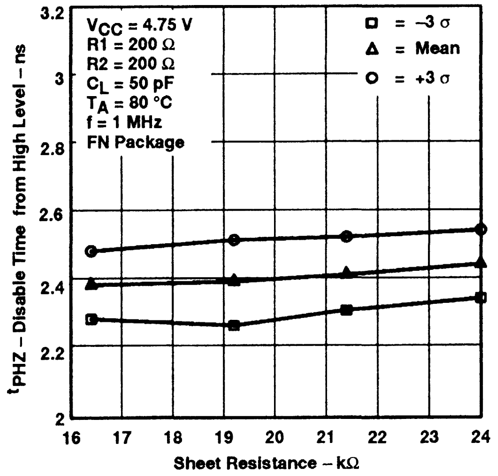
DISABLE TIME, $\overline{\text{OE}}$↑ to Q
(With 8 Outputs Switching in Same Direction)
vs
SHEET RESISTANCE



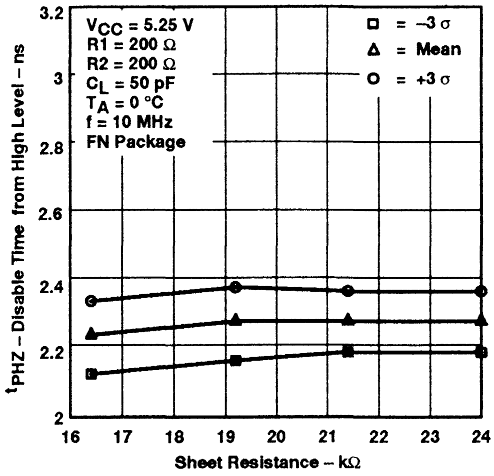
DISABLE TIME, $\overline{\text{OE}}$↑ to Q
(With 1 Output Switching)
vs
SHEET RESISTANCE



DISABLE TIME, $\overline{\text{OE}}$↑ to Q
(With 8 Outputs Switching in Same Direction)
vs
SHEET RESISTANCE

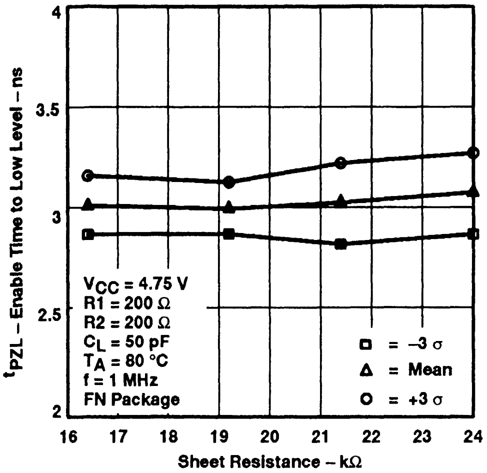


DISABLE TIME, $\overline{\text{OE}}$↑ to Q
(With 1 Output Switching)
vs
SHEET RESISTANCE

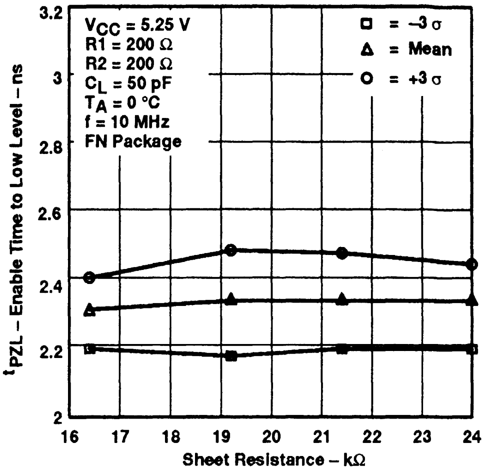


TIBPAL20R8-5C (continued)

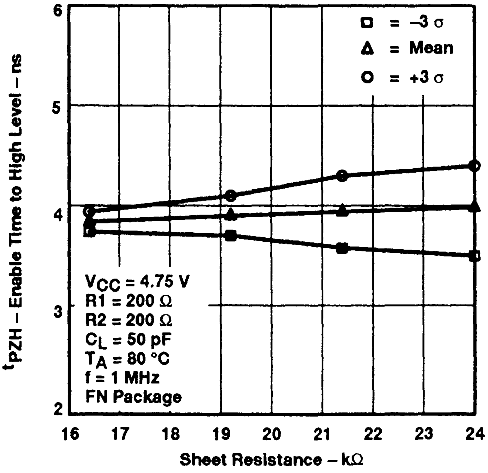
ENABLE TIME, $\overline{OE}$↓ to Q
(With 8 Outputs Switching In Same Direction)
vs
SHEET RESISTANCE



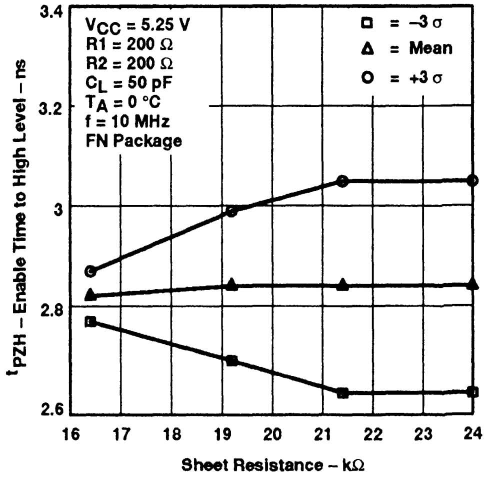
ENABLE TIME, $\overline{OE}$↓ to Q
(With 1 Output Switching)
vs
SHEET RESISTANCE



ENABLE TIME, $\overline{OE}$↓ to Q
(With 8 Outputs Switching In Same Direction)
vs
SHEET RESISTANCE



ENABLE TIME, $\overline{OE}$↓ to Q
(With 1 Output Switching)
vs
SHEET RESISTANCE



24-pin 7-ns and 24-pin 10-ns IMPACT-X PLDs

Devices included in this section:

TIBPAL20L8-7C
TIBPAL20R4-7C
TIBPAL20R6-7C
TIBPAL20R8-7C
TIBPAL20L8-10C
TIBPAL20R4-10C
TIBPAL20R6-10C
TIBPAL20R8-10C

DEVICE INFORMATION

24-pin 7-ns and 24-pin 10-ns IMPACT-X PLDs

1. Technology .... IMPACT-X
2. Package Types: .... 24-pin plastic DIP,
   28-pin plastic PLCC
3. Last Die Revision .... X (None)
4. Bar Size .... 107 x 96 mils
5. Still Air Thermal Impedance :

	PDIP	PLCC
$R_{\theta JA}$	71.5	84.8
$R_{\theta JC}$	31.2	26.7

6. $R_{\theta JA}$ with Air Flow :

FPM	PDIP	PLCC
0	82.6	92.9
100	62.8	69.6
250	46.3	61.0
500	37.6	50.1
750		44.2
1000		41.0

The TIBPAL20XX-10 is down binned (selected from) TIBPAL20XX-7. The TIBPAL20XX-10 devices are not tested to the 7-ns specifications.

This device is from the same master bar as the TIBPAL16XX-7C. Therefore the qualification and characterization data are the same.

QUALIFICATION INFORMATION

The TIBPAL16XX-7, TIBPAL20XX-7, and TIBPAL20XX-10 devices are qualified using the accelerated qualification program. The following summaries give the required tests and results for this device family as well as any additional test performed for additional data.

Required Tests and Results for TIBPAL16XX-7, TIBPAL20XX-7, and TIBPAL20XX-10

Device Types:	20R6-7, 20R8-7, and 20L8-7
Package Type:	24 pin PDIP
Date Codes:	935XF, 935XF, and 939XF
Die Lot Numbers:	15080, 14508, and 20604

TEST	SS/F	ENDPOINT	RESULTS	EXTENDED READPOINT	RESULTS
150°C Dynamic Op-Life	129/1	420 HRS	287/0		
125°C Dynamic Op-Life	129/1	208 HRS	257/0	1000 HRS	257/0
130°C/85% RH HAST	129/1	100 HRS	258/0		
–65°C/150°C Thermal Shock	129/1	100 CYC	129/0	1000 CYC	129/0
–65°C/150°C Temp Cycle	77/1	100 CYC	77/0	1000 CYC	77/0
ESD	3/0	2000 V	3/0		

Additional Qualification Tests and Results for TIBPAL16XX-7, TIBPAL20XX-7, and TIBPAL20XX-10

Device Type:	20R4-7
Package Type:	20 pin PDIP
Date Code:	922XF
Die Lot Numbers:	08980, 09343, and 09344

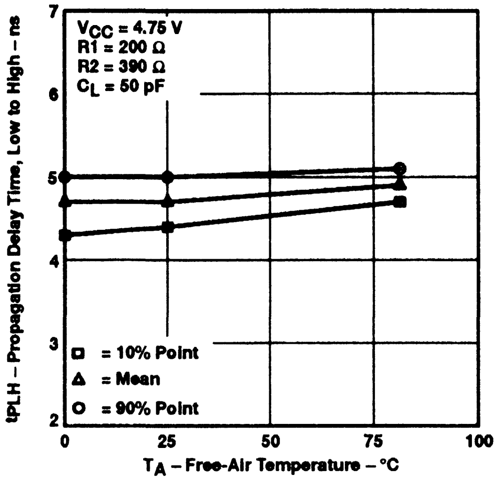
TEST	SS/F	ENDPOINT	RESULTS	EXTENDED READPOINT	RESULTS
150°C Dynamic Op-Life	129/1	384 HRS	201/0	1000 HRS	201/0
125°C Dynamic Op-Life	129/1	208 HRS	201/0	1000 HRS	201/0
130°C/85% RH HAST	129/1	100 HRS	199/0[1]		
–65°C/150°C Thermal Shock	77/1	200 CYC	201/0		
ESD	3/0	2000 V	3/0		

1. 2 units mechanically damaged beyond repair - unable to test - removed from sample.

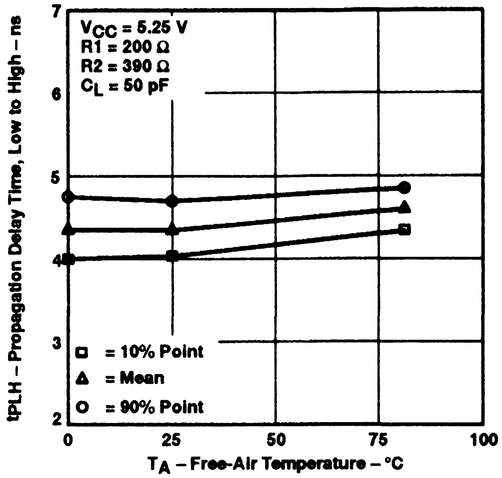
CHARACTERIZATION INFORMATION

TIBPAL20L8-7C/10C
TIBPAL20R4-7C/10C
TIBPAL20R6-7C/10C
TIBPAL20R8-7C/10C

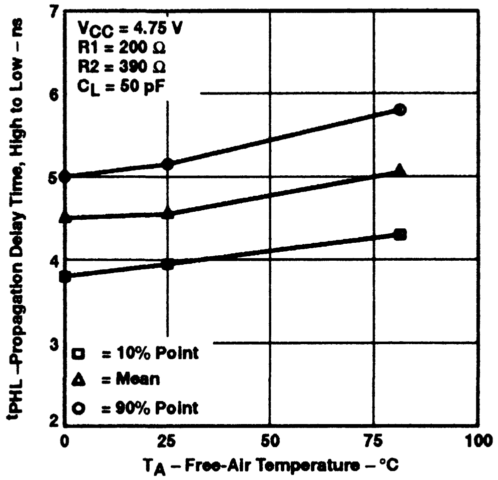
PROPAGATION DELAY TIME
(t_{PLH} from I, I/O to O, I/O)
vs
FREE-AIR TEMPERATURE



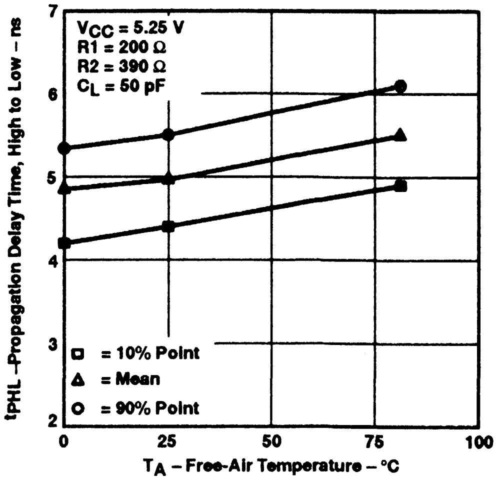
PROPAGATION DELAY TIME
(t_{PLH} from I, I/O to O, I/O)
vs
FREE-AIR TEMPERATURE



PROPAGATION DELAY TIME
(t_{PHL} from I, I/O to O, I/O)
vs
FREE-AIR TEMPERATURE

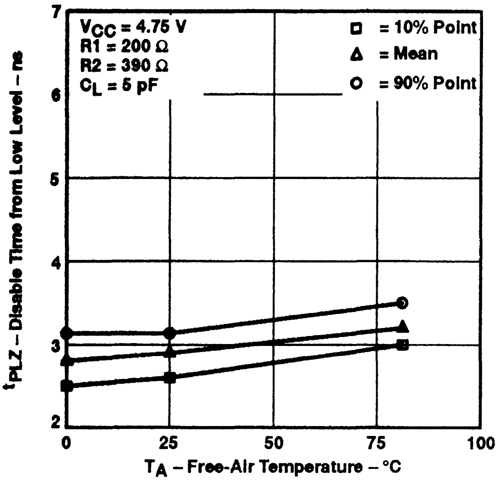


PROPAGATION DELAY TIME
(t_{PHL} from I, I/O to O, I/O)
vs
FREE-AIR TEMPERATURE

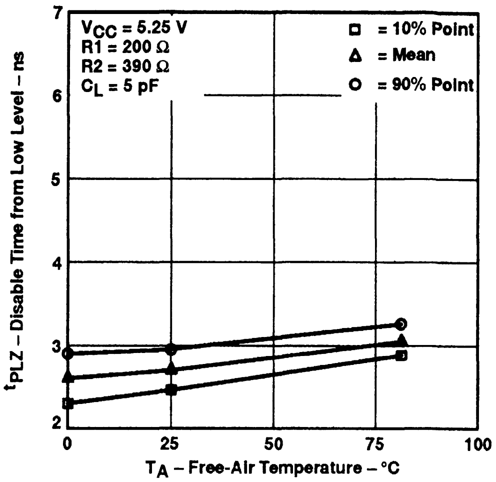


TIBPAL20L8-7C (continued)

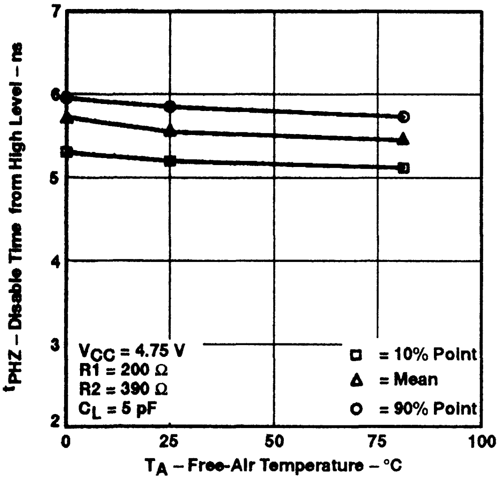
PROPAGATION DELAY TIME
(t_{PLZ} from I, I/O to O, I/O)
vs
FREE-AIR TEMPERATURE



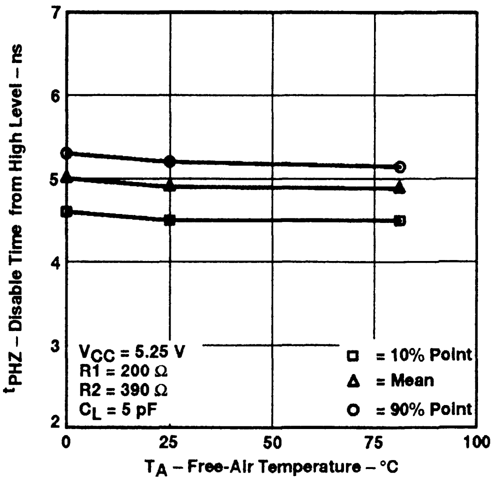
PROPAGATION DELAY TIME
(t_{PLZ} from I, I/O to O, I/O)
vs
FREE-AIR TEMPERATURE



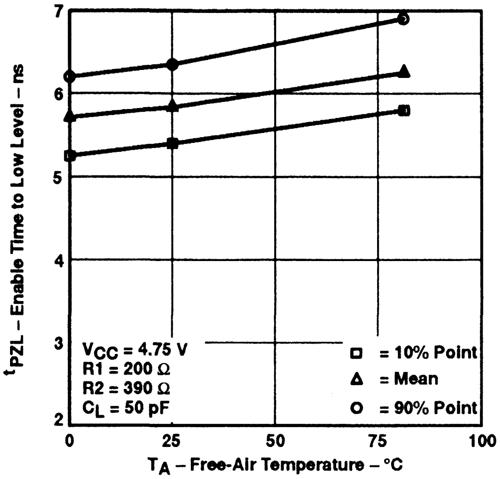
PROPAGATION DELAY TIME
(t_{PHZ} from I, I/O to O, I/O)
vs
FREE-AIR TEMPERATURE

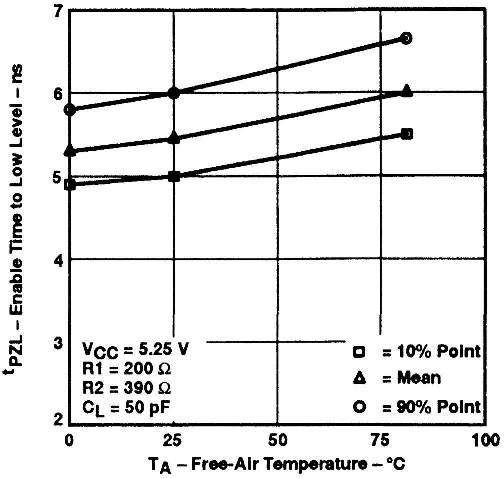


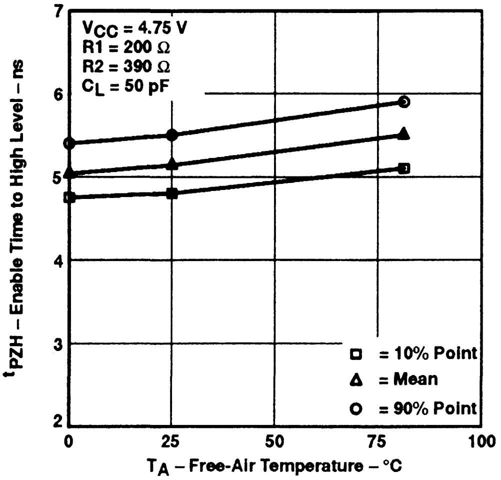
PROPAGATION DELAY TIME
(t_{PHZ} from I, I/O to O, I/O)
vs
FREE-AIR TEMPERATURE

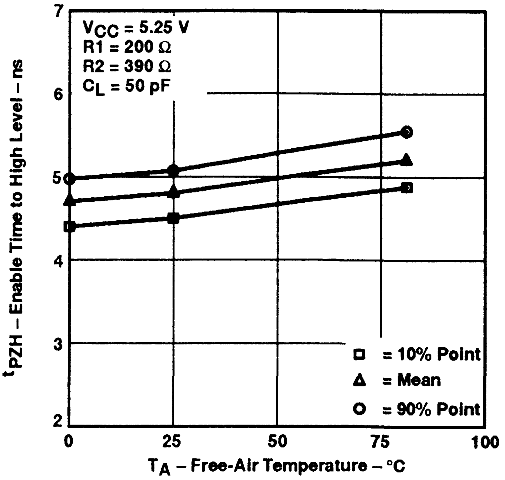


TIBPAL20L8-7C (continued)

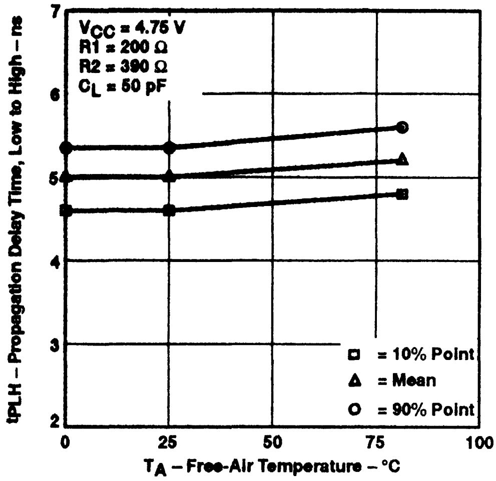

PROPAGATION DELAY TIME
(t_{PZL} from I, I/O to O, I/O)
vs
FREE-AIR TEMPERATURE


PROPAGATION DELAY TIME
(t_{PZL} from I, I/O to O, I/O)
vs
FREE-AIR TEMPERATURE

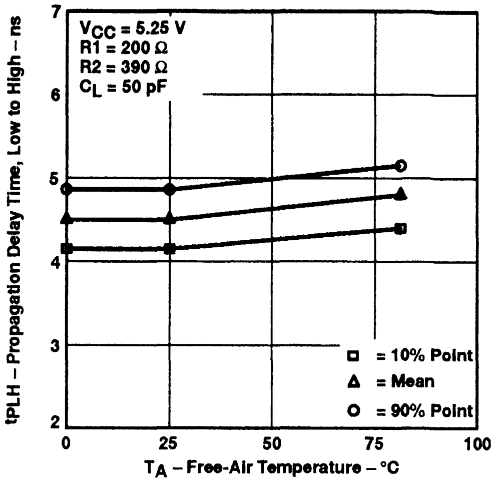

PROPAGATION DELAY TIME
(t_{PZH} from I, I/O to O, I/O)
vs
FREE-AIR TEMPERATURE


PROPAGATION DELAY TIME
(t_{PZH} from I, I/O to O, I/O)
vs
FREE-AIR TEMPERATURE

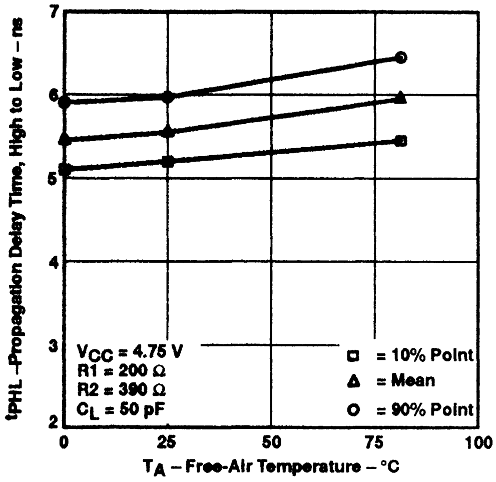
PROPAGATION DELAY TIME (t_{PLH} from I, I/O to I/O) vs FREE-AIR TEMPERATURE



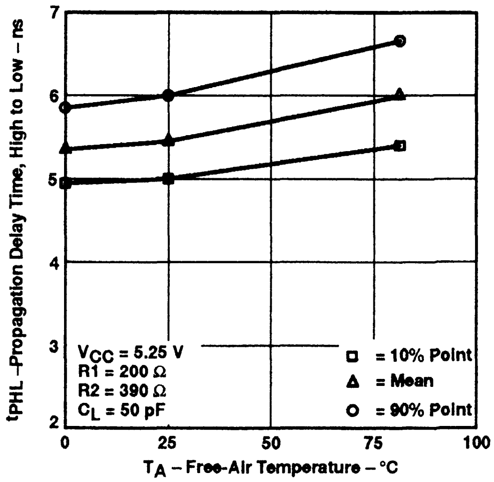
PROPAGATION DELAY TIME (t_{PLH} from I, I/O to I/O) vs FREE-AIR TEMPERATURE



PROPAGATION DELAY TIME (t_{PHL} from I, I/O to I/O) vs FREE-AIR TEMPERATURE

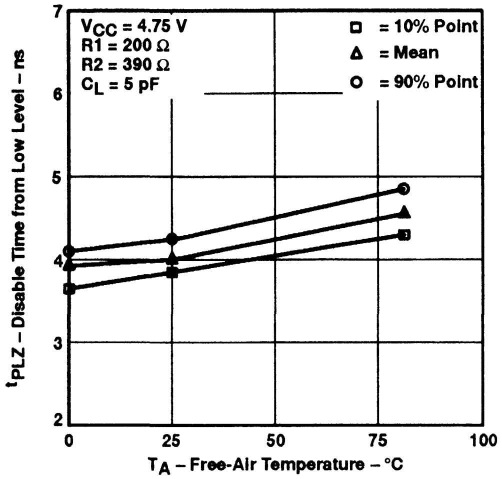


PROPAGATION DELAY TIME (t_{PHL} from I, I/O to I/O) vs FREE-AIR TEMPERATURE

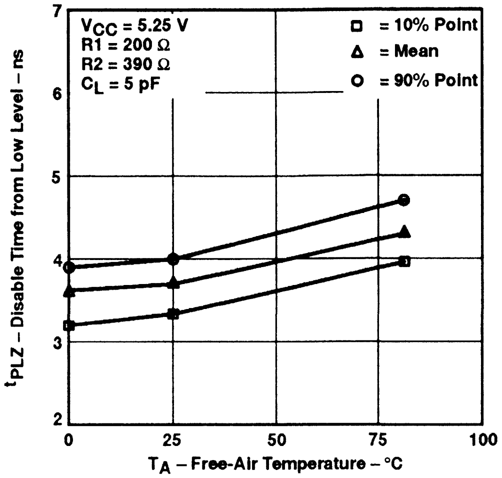


TIBPAL20R4-7C (continued)

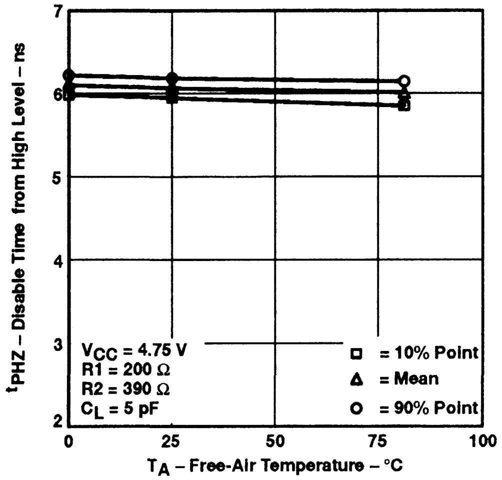
PROPAGATION DELAY TIME
(t_{PLZ} from I, I/O to I/O)
vs
FREE-AIR TEMPERATURE



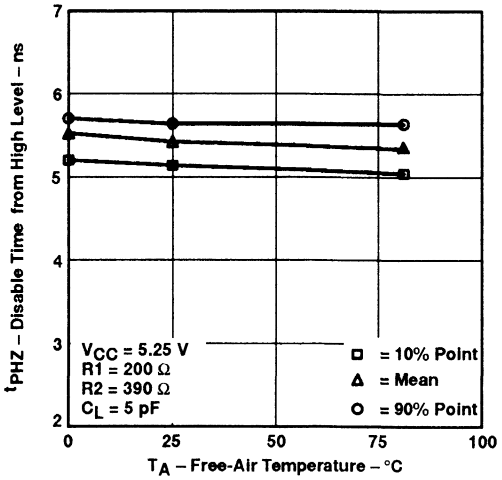
PROPAGATION DELAY TIME
(t_{PLZ} from I, I/O to I/O)
vs
FREE-AIR TEMPERATURE



PROPAGATION DELAY TIME
(t_{PHZ} from I, I/O to I/O)
vs
FREE-AIR TEMPERATURE

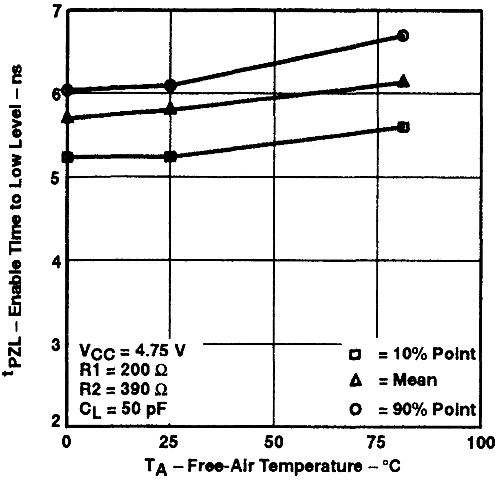


PROPAGATION DELAY TIME
(t_{PHZ} from I, I/O to I/O)
vs
FREE-AIR TEMPERATURE

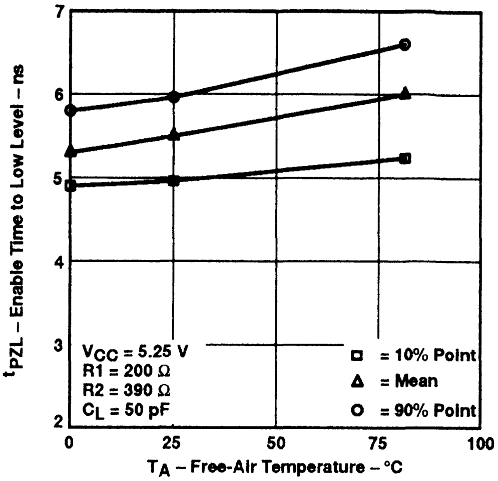


TIBPAL20R4-7C (continued)

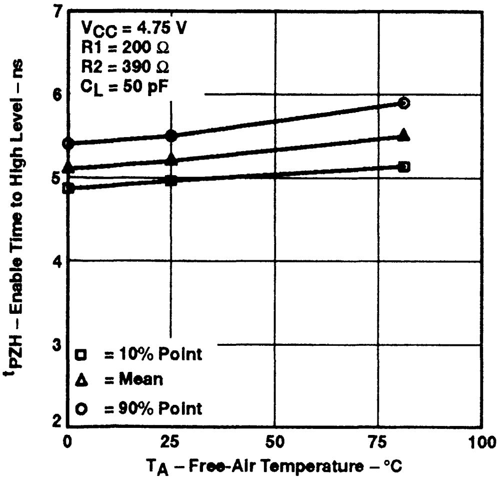
PROPAGATION DELAY TIME
(t_{PZL} from I, I/O to I/O)
vs
FREE-AIR TEMPERATURE



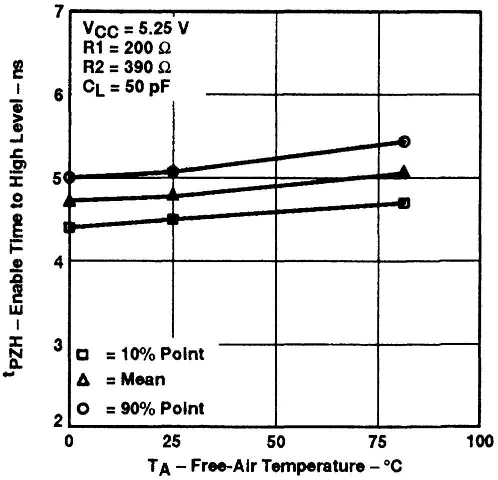
PROPAGATION DELAY TIME
(t_{PZL} from I, I/O to I/O)
vs
FREE-AIR TEMPERATURE



PROPAGATION DELAY TIME
(t_{PZH} from I, I/O to I/O)
vs
FREE-AIR TEMPERATURE

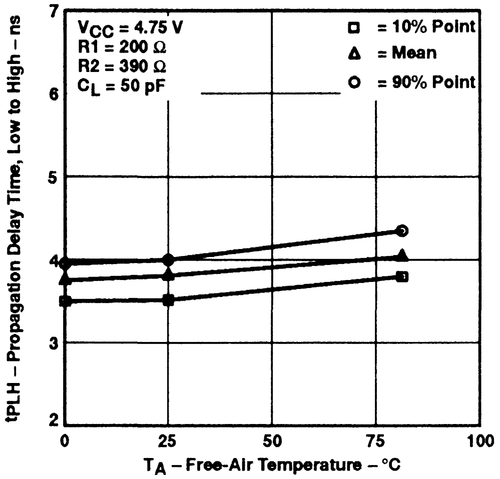


PROPAGATION DELAY TIME
(t_{PZH} from I, I/O to I/O)
vs
FREE-AIR TEMPERATURE

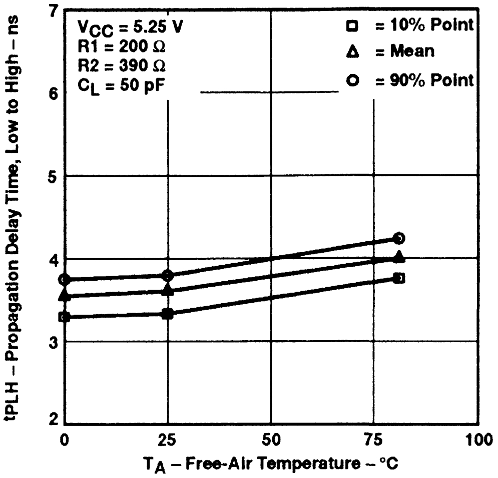


TIBPAL20R4-7C (continued)

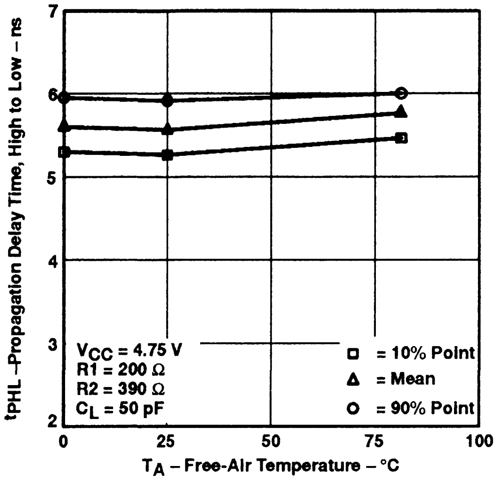
PROPAGATION DELAY TIME (t_{PLH} from CLK to Q) vs FREE-AIR TEMPERATURE



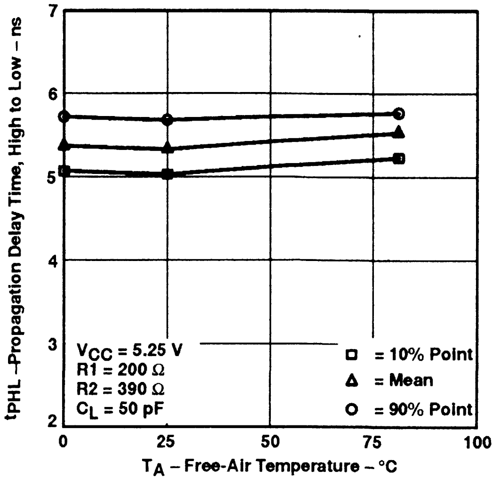
PROPAGATION DELAY TIME (t_{PLH} from CLK to Q) vs FREE-AIR TEMPERATURE



PROPAGATION DELAY TIME (t_{PHL} from CLK to Q) vs FREE-AIR TEMPERATURE

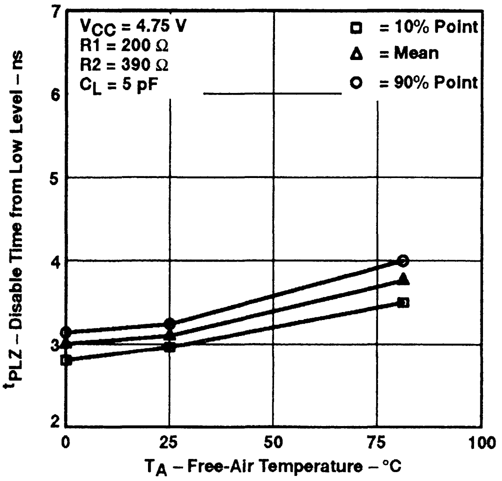


PROPAGATION DELAY TIME (t_{PHL} from CLK to Q) vs FREE-AIR TEMPERATURE

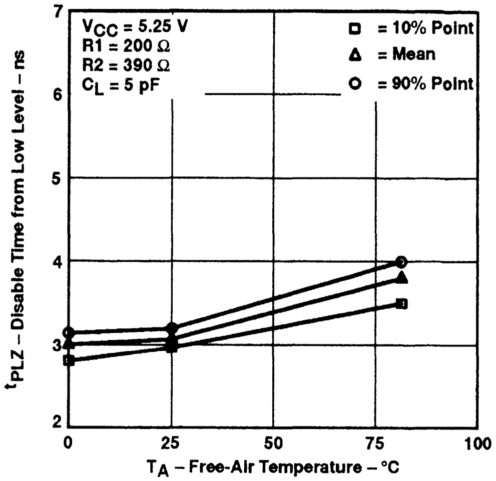


TIBPAL20R4-7C (continued)

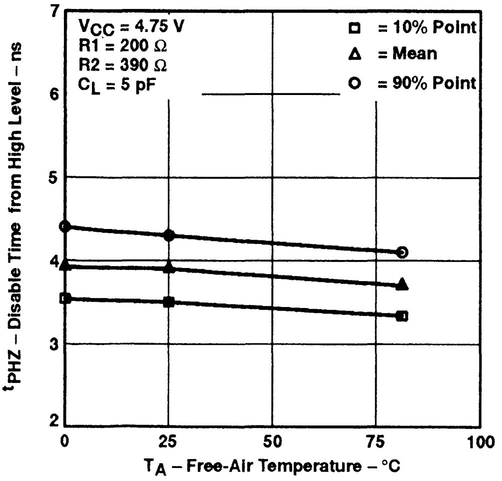
PROPAGATION DELAY TIME
(t_{PLZ} from OE↓ to Q)
vs
FREE-AIR TEMPERATURE



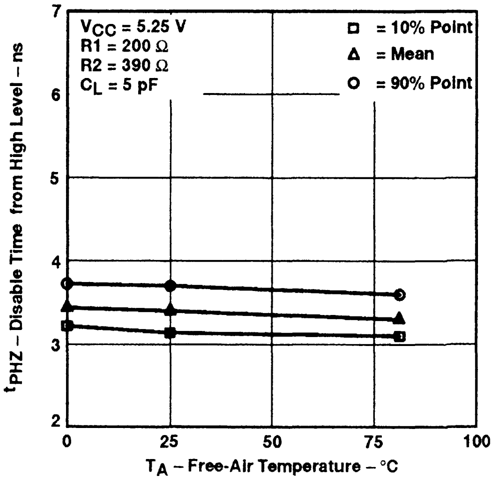
PROPAGATION DELAY TIME
(t_{PLZ} from OE↓ to Q)
vs
FREE-AIR TEMPERATURE



PROPAGATION DELAY TIME
(t_{PHZ} from OE↓ to Q)
vs
FREE-AIR TEMPERATURE

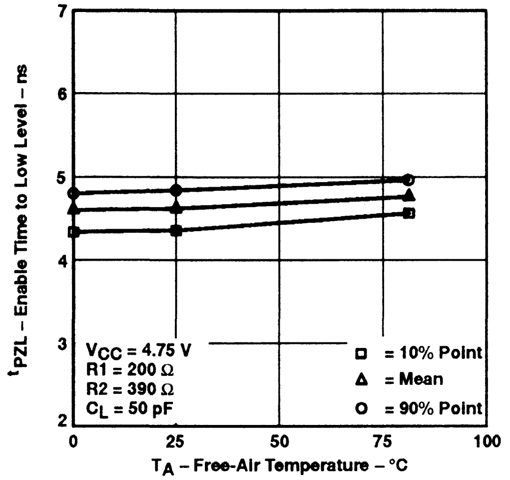


PROPAGATION DELAY TIME
(t_{PHZ} from OE↓ to Q)
vs
FREE-AIR TEMPERATURE

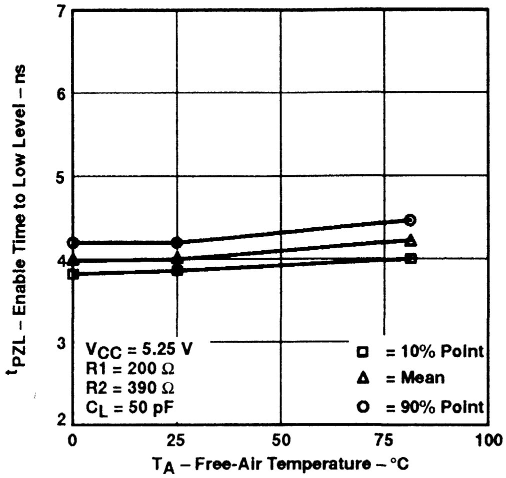


TIBPAL20R4-7C (continued)

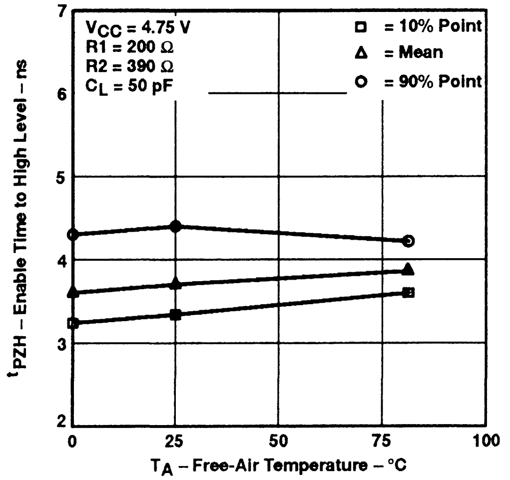
PROPAGATION DELAY TIME
(t_{PZL} from OE↑ to Q)
vs
FREE-AIR TEMPERATURE



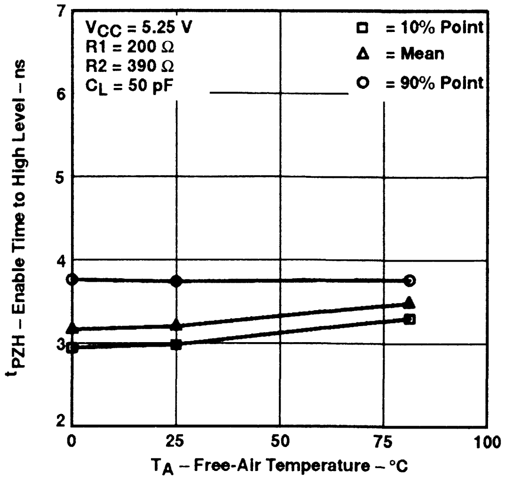
PROPAGATION DELAY TIME
(t_{PZL} from OE↑ to Q)
vs
FREE-AIR TEMPERATURE



PROPAGATION DELAY TIME
(t_{PZH} from OE↑ to Q)
vs
FREE-AIR TEMPERATURE

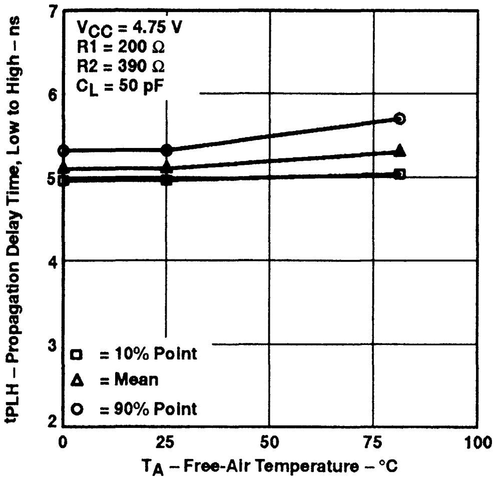


PROPAGATION DELAY TIME
(t_{PZH} from OE↑ to Q)
vs
FREE-AIR TEMPERATURE

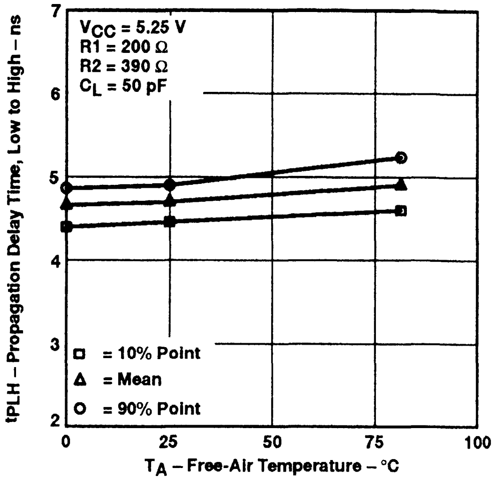


TIBPAL20R6-7C

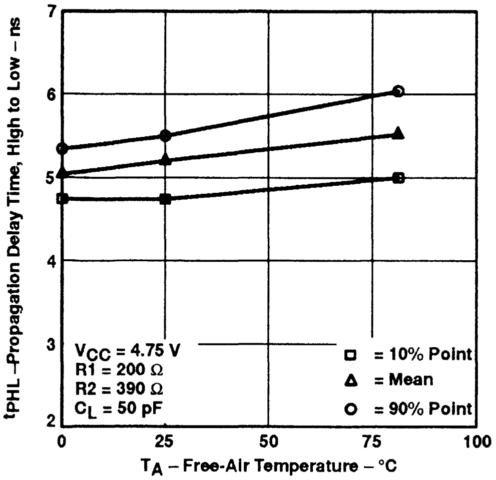
PROPAGATION DELAY TIME
(t_{PLH} from I, I/O to I/O)
vs
FREE-AIR TEMPERATURE



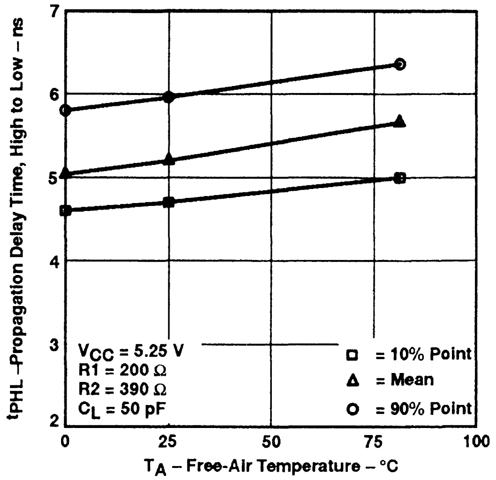
PROPAGATION DELAY TIME
(t_{PLH} from I, I/O to I/O)
vs
FREE-AIR TEMPERATURE



PROPAGATION DELAY TIME
(t_{PHL} from I, I/O to I/O)
vs
FREE-AIR TEMPERATURE

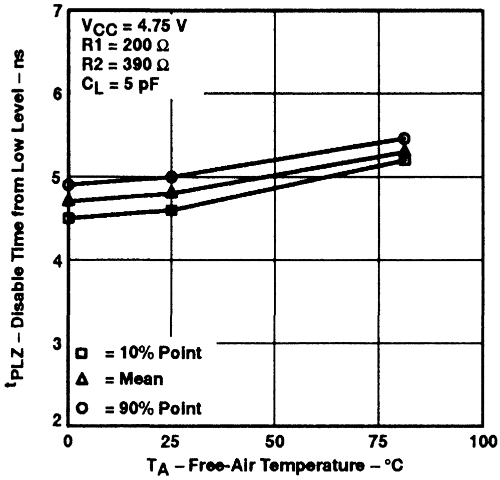


PROPAGATION DELAY TIME
(t_{PHL} from I, I/O to I/O)
vs
FREE-AIR TEMPERATURE

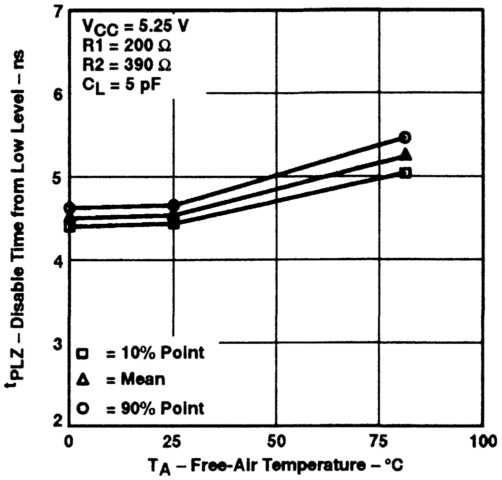


TIBPAL20R6-7C (continued)

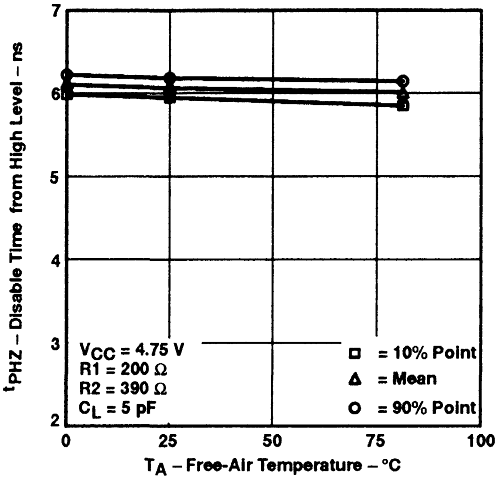
PROPAGATION DELAY TIME
(t_{PLZ} from I, I/O to I/O)
vs
FREE-AIR TEMPERATURE



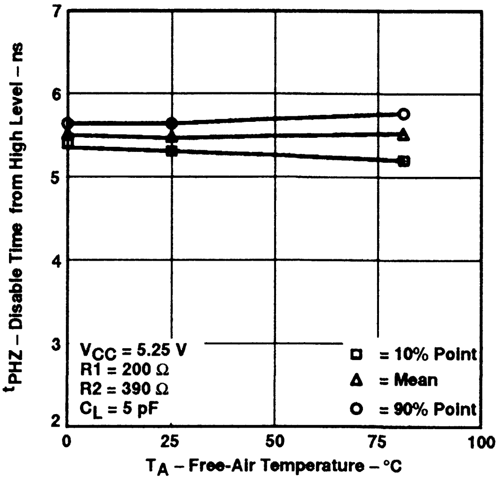
PROPAGATION DELAY TIME
(t_{PLZ} from I, I/O to I/O)
vs
FREE-AIR TEMPERATURE



PROPAGATION DELAY TIME
(t_{PHZ} from I, I/O to I/O)
vs
FREE-AIR TEMPERATURE

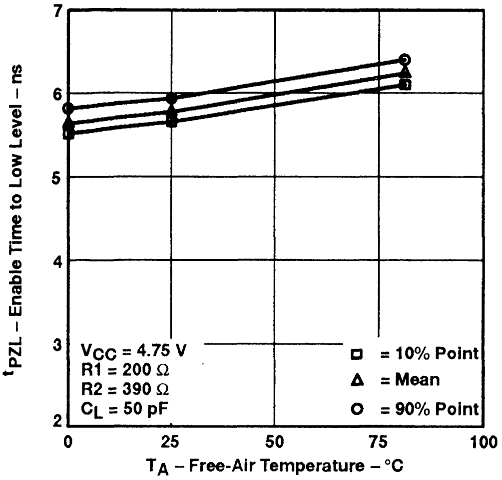


PROPAGATION DELAY TIME
(t_{PHZ} from I, I/O to I/O)
vs
FREE-AIR TEMPERATURE

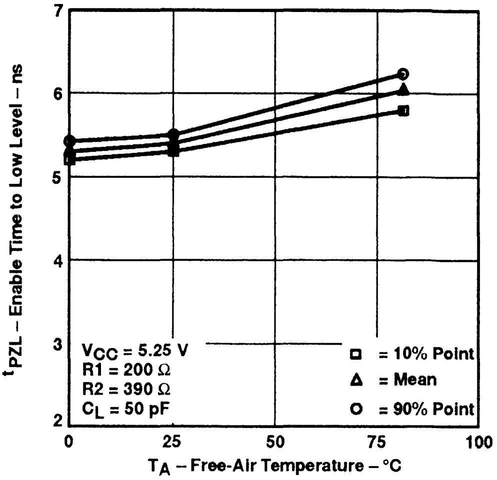


TIBPAL20R6-7C (continued)

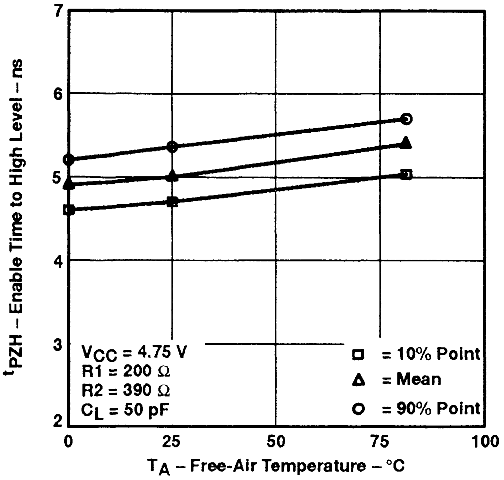
PROPAGATION DELAY TIME (t_{PZL} from I, I/O to I/O) vs FREE-AIR TEMPERATURE



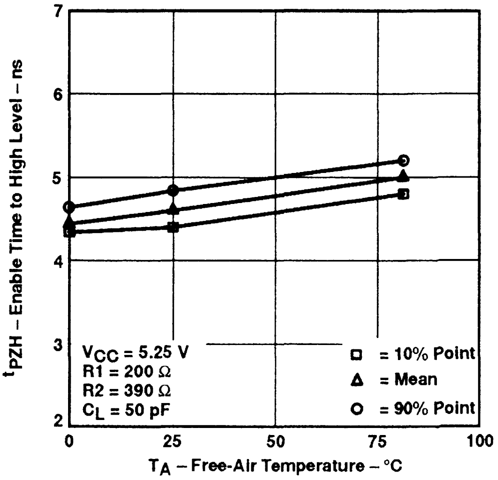
PROPAGATION DELAY TIME (t_{PZL} from I, I/O to I/O) vs FREE-AIR TEMPERATURE



PROPAGATION DELAY TIME (t_{PZH} from I, I/O to I/O) vs FREE-AIR TEMPERATURE

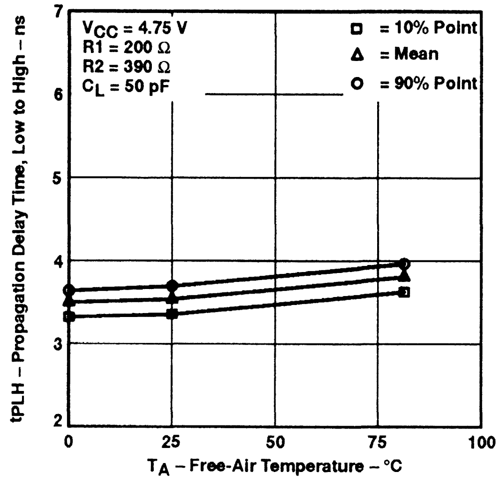


PROPAGATION DELAY TIME (t_{PZH} from I, I/O to I/O) vs FREE-AIR TEMPERATURE

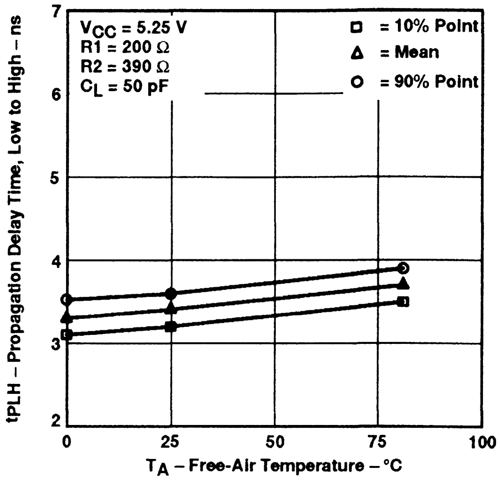


TIBPAL20R6-7C (continued)

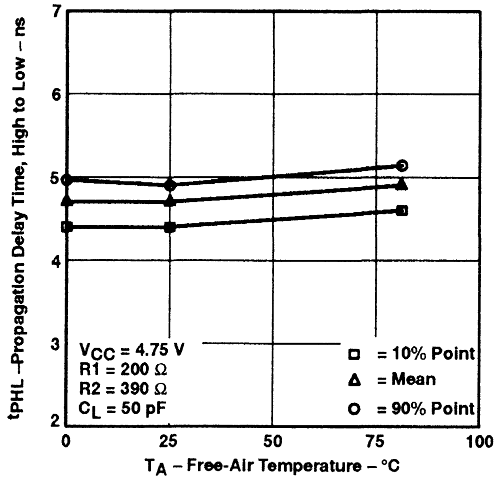
PROPAGATION DELAY TIME
(t_{PLH} from CLK to Q)
vs
FREE-AIR TEMPERATURE



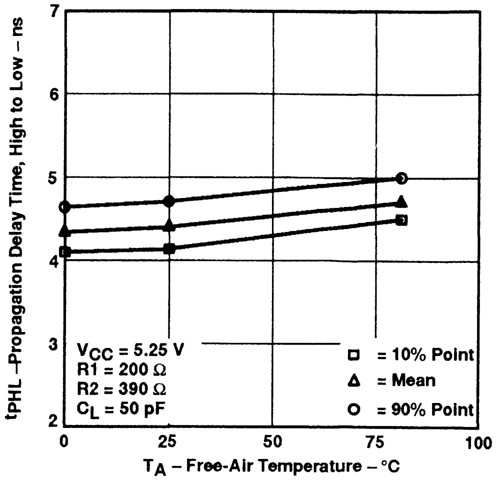
PROPAGATION DELAY TIME
(t_{PLH} from CLK to Q)
vs
FREE-AIR TEMPERATURE



PROPAGATION DELAY TIME
(t_{PHL} from CLK to Q)
vs
FREE-AIR TEMPERATURE

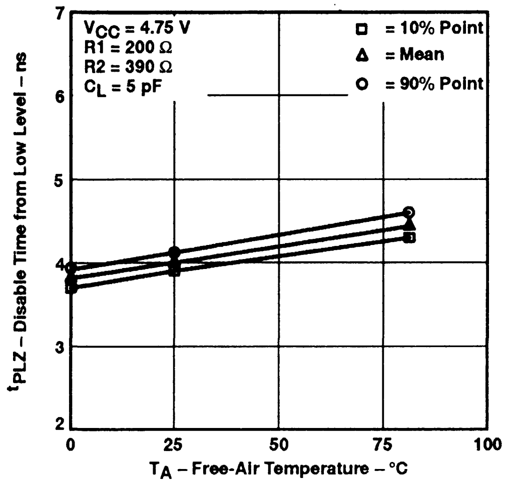


PROPAGATION DELAY TIME
(t_{PHL} from CLK to Q)
vs
FREE-AIR TEMPERATURE

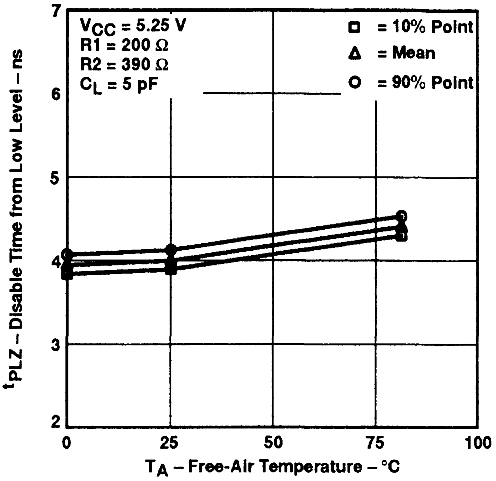


TIBPAL20R6-7C (continued)

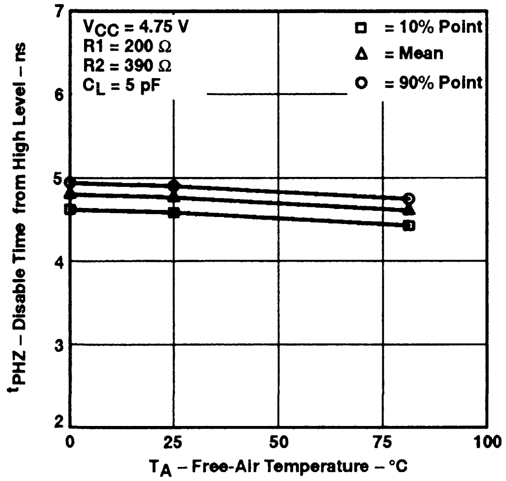
PROPAGATION DELAY TIME
(t_{PLZ} from OE↓ to Q)
vs
FREE-AIR TEMPERATURE



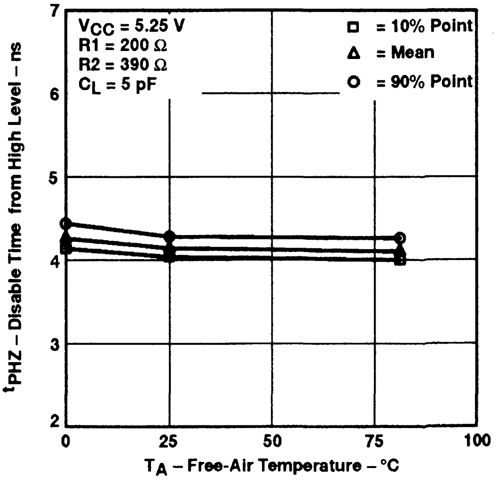
PROPAGATION DELAY TIME
(t_{PLZ} from OE↓ to Q)
vs
FREE-AIR TEMPERATURE



PROPAGATION DELAY TIME
(t_{PHZ} from OE↓ to Q)
vs
FREE-AIR TEMPERATURE

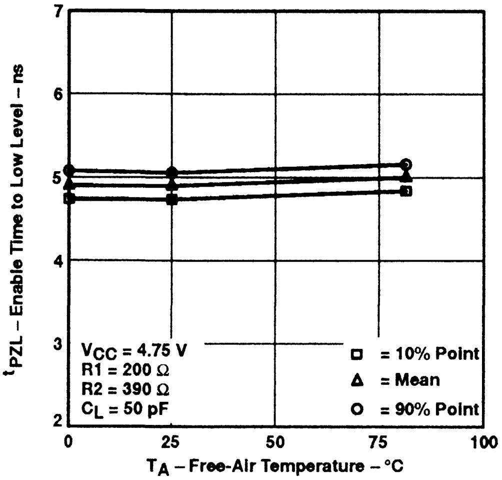


PROPAGATION DELAY TIME
(t_{PHZ} from OE↓ to Q)
vs
FREE-AIR TEMPERATURE

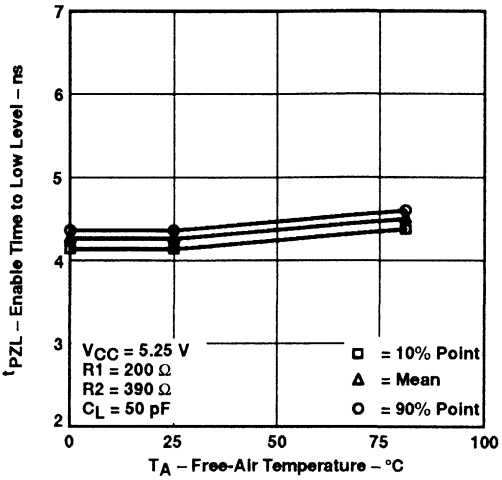


TIBPAL20R6-7C (continued)

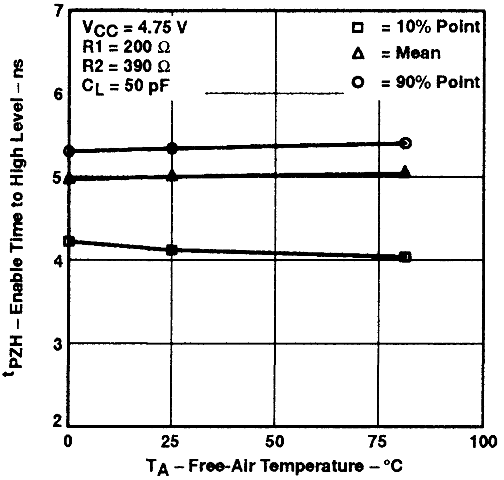
PROPAGATION DELAY TIME
(t_{PZL} from OE↑ to Q)
vs
FREE-AIR TEMPERATURE



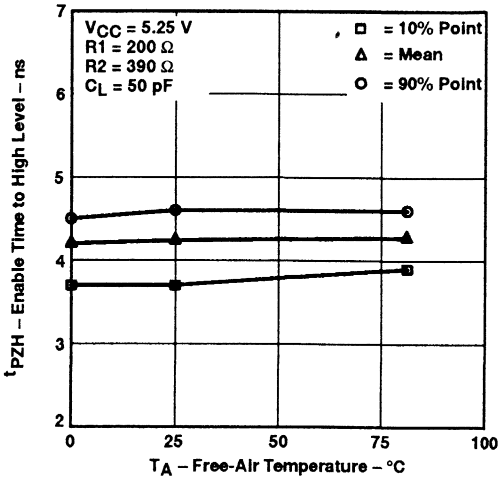
PROPAGATION DELAY TIME
(t_{PZL} from OE↑ to Q)
vs
FREE-AIR TEMPERATURE



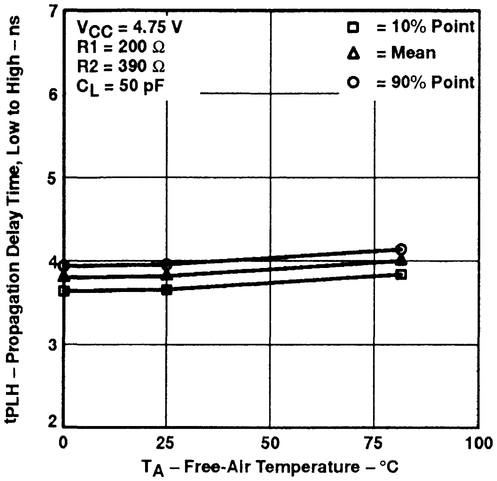
PROPAGATION DELAY TIME
(t_{PZH} from OE↑ to Q)
vs
FREE-AIR TEMPERATURE



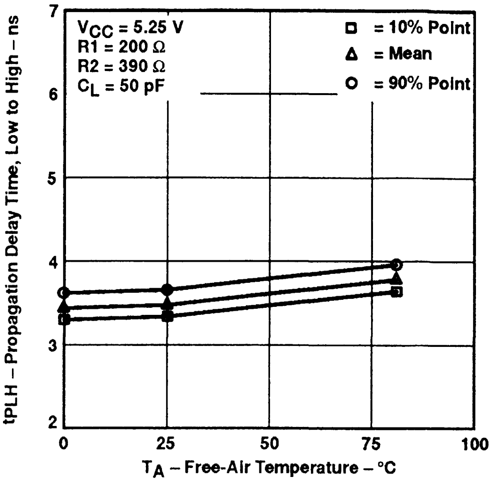
PROPAGATION DELAY TIME
(t_{PZH} from OE↑ to Q)
vs
FREE-AIR TEMPERATURE



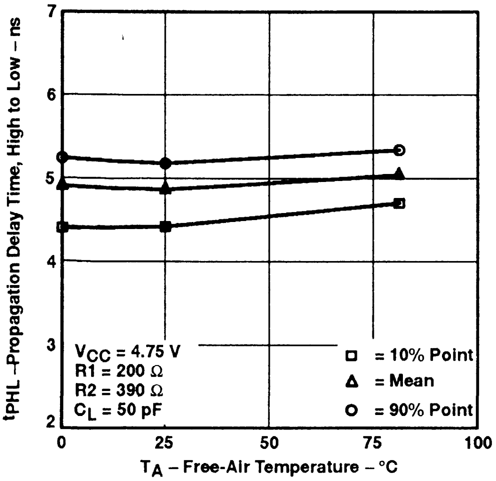
PROPAGATION DELAY TIME (t_{PLH} from CLK to Q) vs FREE-AIR TEMPERATURE



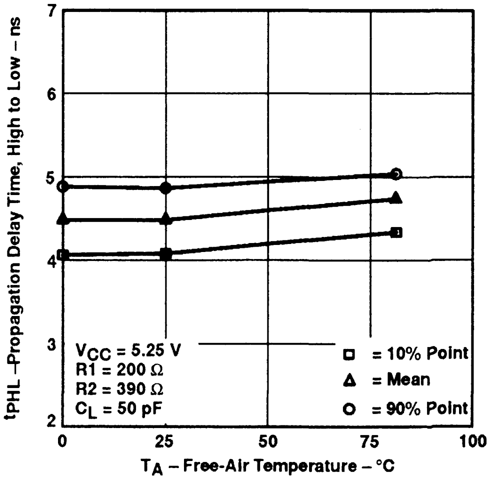
PROPAGATION DELAY TIME (t_{PLH} from CLK to Q) vs FREE-AIR TEMPERATURE



PROPAGATION DELAY TIME (t_{PHL} from CLK to Q) vs FREE-AIR TEMPERATURE

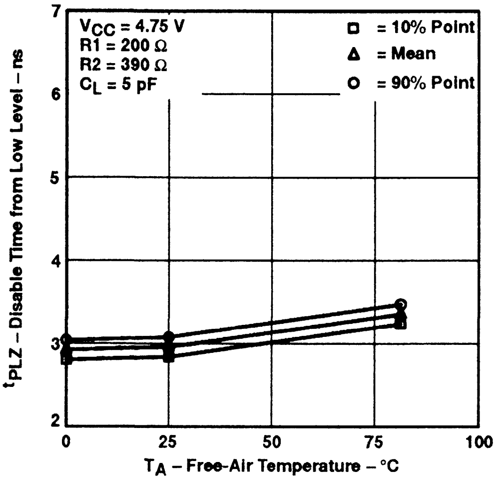


PROPAGATION DELAY TIME (t_{PHL} from CLK to Q) vs FREE-AIR TEMPERATURE

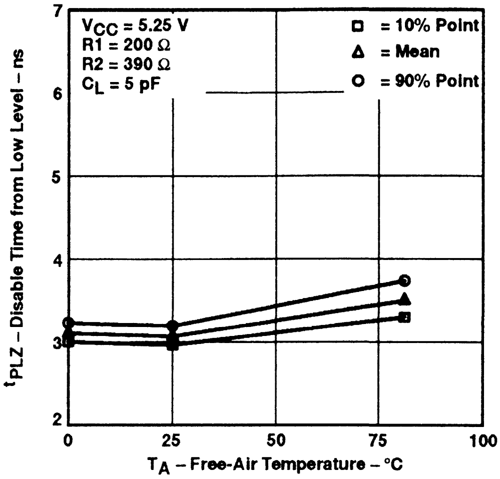


TIBPAL20R8-7C (continued)

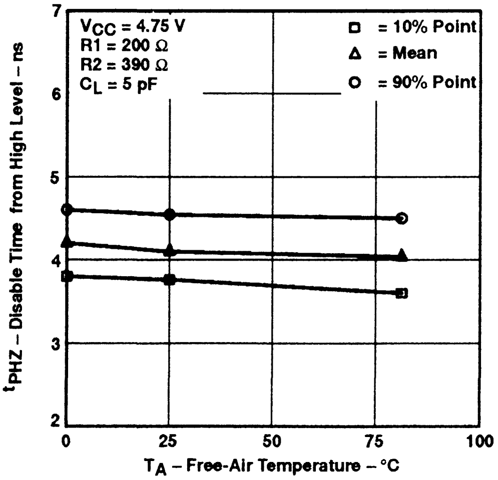
PROPAGATION DELAY TIME
(t_{PLZ} from OE↓ to Q)
vs
FREE-AIR TEMPERATURE



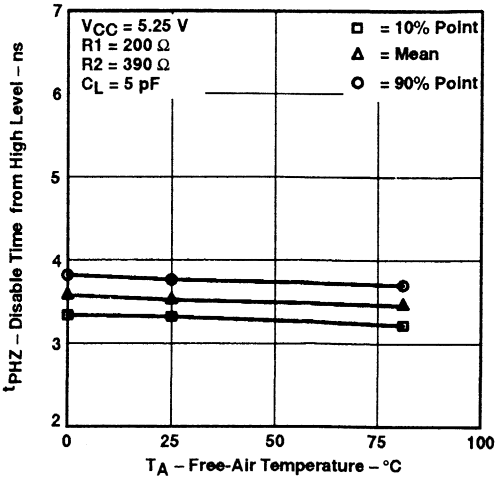
PROPAGATION DELAY TIME
(t_{PLZ} from OE↓ to Q)
vs
FREE-AIR TEMPERATURE



PROPAGATION DELAY TIME
(t_{PHZ} from OE↓ to Q)
vs
FREE-AIR TEMPERATURE

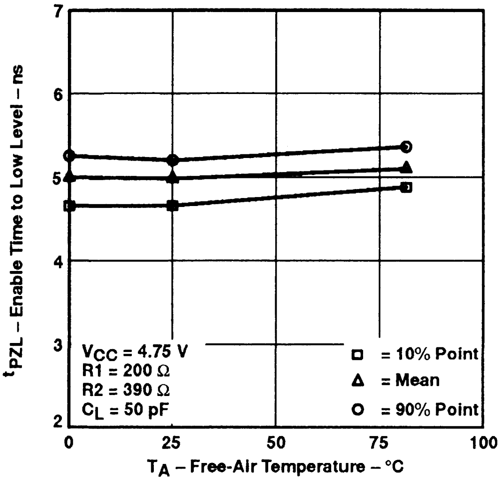


PROPAGATION DELAY TIME
(t_{PHZ} from OE↓ to Q)
vs
FREE-AIR TEMPERATURE

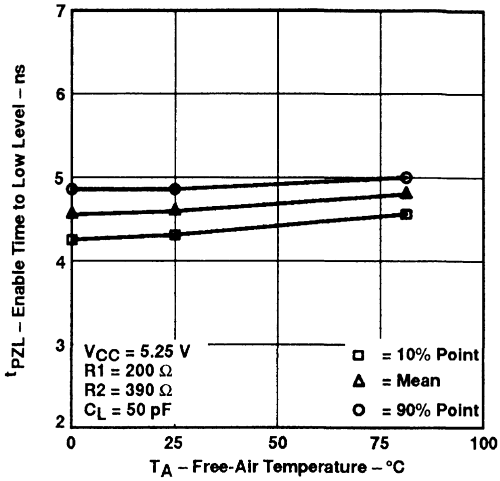


TIBPAL20R8-7C (continued)

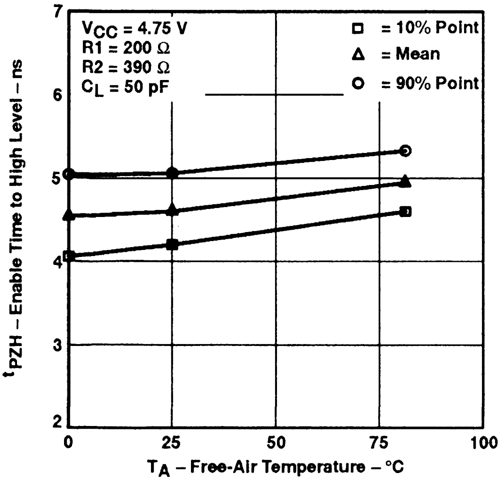
PROPAGATION DELAY TIME
(t_{PZL} from OE↑ to Q)
vs
FREE-AIR TEMPERATURE



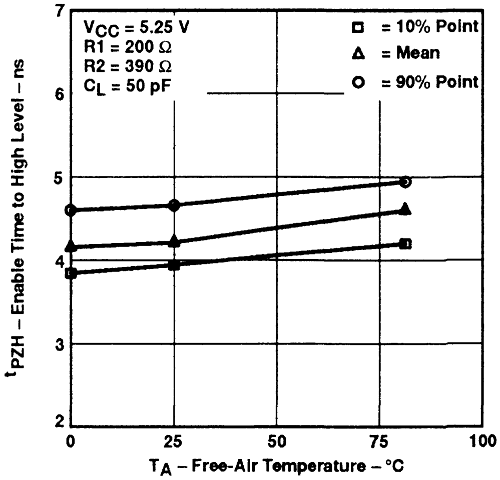
PROPAGATION DELAY TIME
(t_{PZL} from OE↑ to Q)
vs
FREE-AIR TEMPERATURE



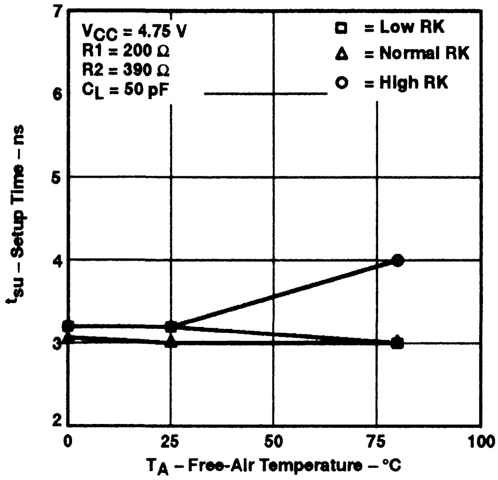
PROPAGATION DELAY TIME
(t_{PZH} from OE↑ to Q)
vs
FREE-AIR TEMPERATURE



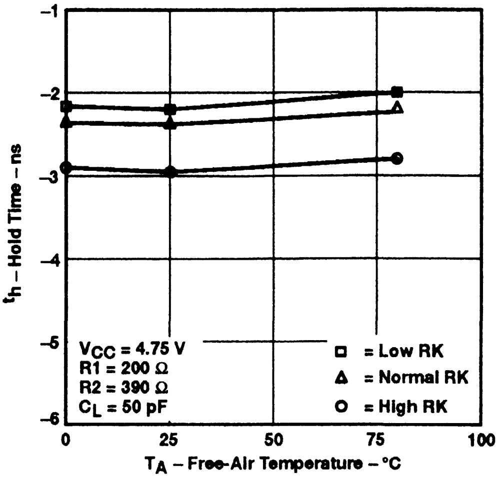
PROPAGATION DELAY TIME
(t_{PZH} from OE↑ to Q)
vs
FREE-AIR TEMPERATURE



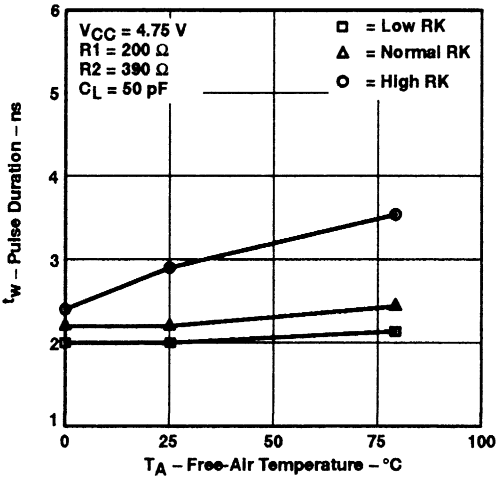
SETUP TIME
(Input or feedback before CLK ↑)
vs
FREE-AIR TEMPERATURE



HOLD TIME
(Input or feedback after CLK ↑)
vs
FREE-AIR TEMPERATURE



PULSE DURATION
(High or Low)
vs
FREE-AIR TEMPERATURE



TIBPAL22V10-15BC

DEVICE INFORMATION
TIBPAL22V10-15BC

1. Technology .... IMPACT-X
2. Package Types : .... 24-pin plastic DIP, 28-pin plastic PLCC
3. Last Die Revision .... X (None)
4. Bar Size .... 130 x 130 mils
5. Still Air Thermal Impedance :

	PDIP	**PLCC**
$R_{\theta JA}$	70.4	94.1
$R_{\theta JC}$	25.7	20.6

6. $R_{\theta JA}$ with Air Flow :

FPM	**PDIP**	**PLCC**
0	83.0	83.3
100	63.0	57.9
250	46.0	46.4
500	38.0	35.3
750		28.8
1000		25.4

QUALIFICATION INFORMATION

The TIBPAL22V10-15BC is qualified using the accelerated qualification program. The following summaries give the required tests and results for this device and any additional test performed for additional data.

Required Tests and Results for TIBPAL22V10-15BC

Package Type: 24 pin PDIP
Die Lot Numbers: 9190916, 9244530, and 9107132

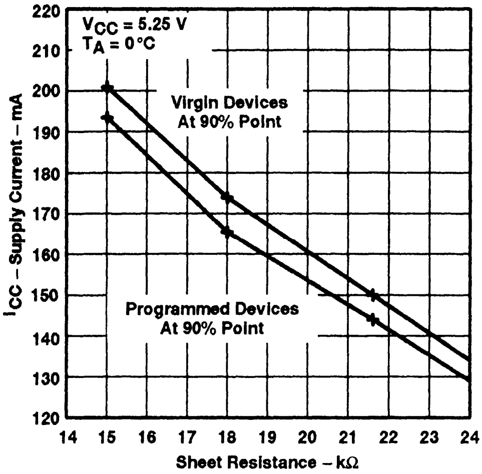
TEST	SS/F	ENDPOINT	RESULTS	EXTENDED READPOINT	RESULTS
125°C Dynamic Op-Life	129/1	1000 HRS	200/0		
130°C/85% RH HAST	129/1	100 HRS	200/1[1]	500 HRS	199/0
–65°C/150°C Temp Cycle	129/1	1000 CYC	199/0[2]		
–65°C/150°C Thermal Shock	77/1	200 CYC	200/0	1000 HRS	200/0
Autoclave	77/1	240 HRS	77/0		
ESD	3/0	2000 V	3/0		

1. Continuity failure caused by ESD. TI FA Report # D12-00443
2. 1 unit mechanically damaged, broken lead, unable to test - removed from population.

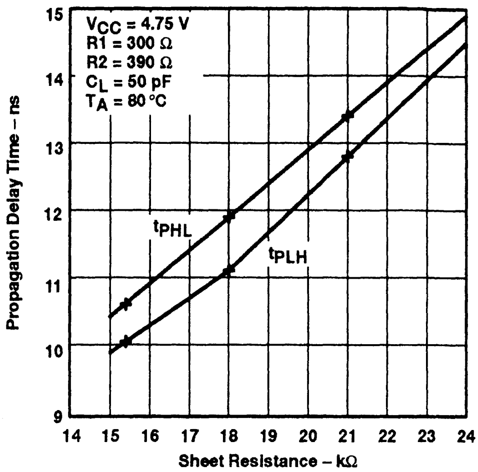
CHARACTERIZATION INFORMATION

TIBPAL22V10-15B

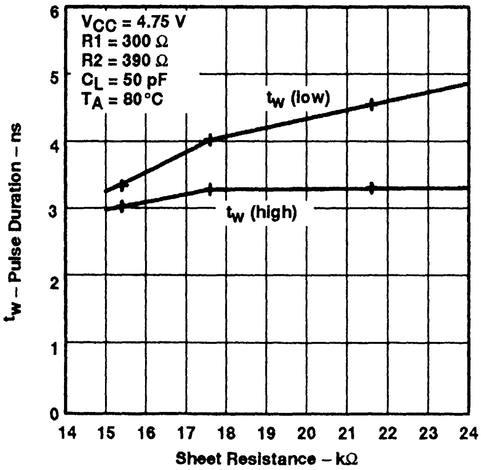
SUPPLY CURRENT vs SHEET RESISTANCE



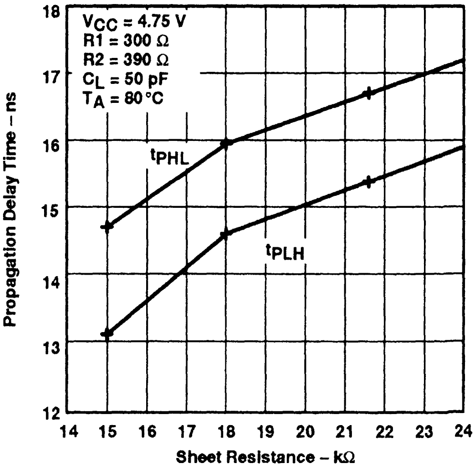
PROPAGATION DELAY TIME (I, I/O to I/O) vs SHEET RESISTANCE



PULSE DURATION vs SHEET RESISTANCE

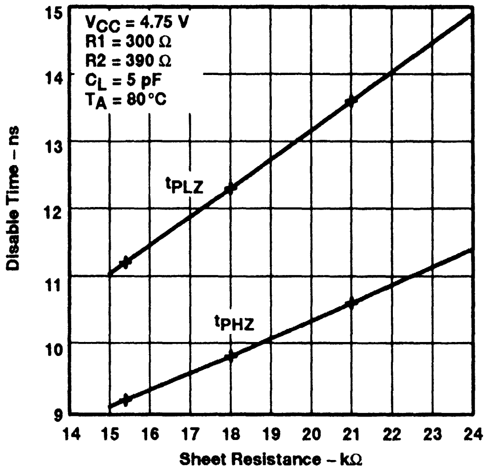


PROPAGATION DELAY TIME (CLK to I/O) vs SHEET RESISTANCE

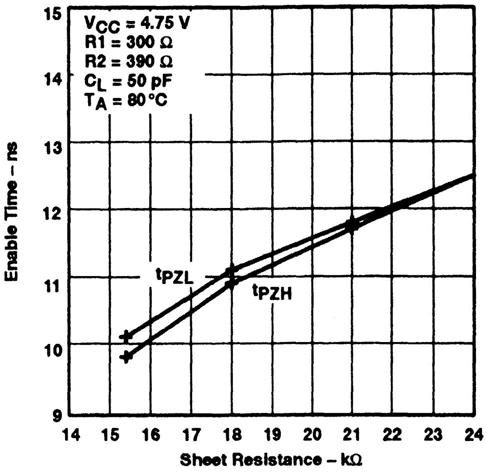


TIBPAL22V10-15B (continued)

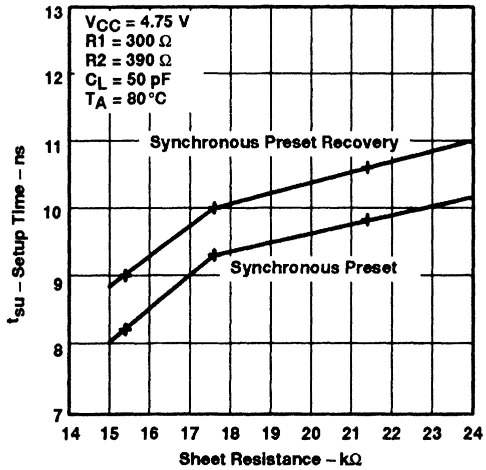
DISABLE TIME
vs
SHEET RESISTANCE



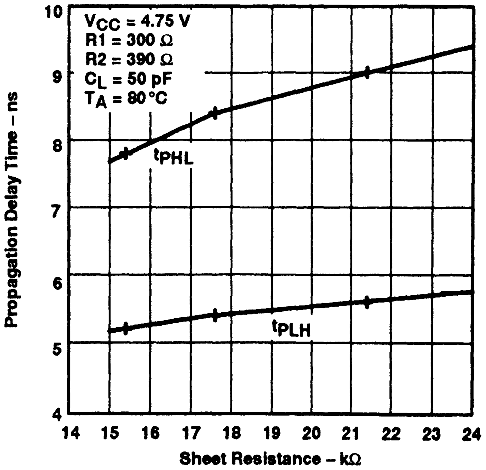
ENABLE TIME
vs
SHEET RESISTANCE



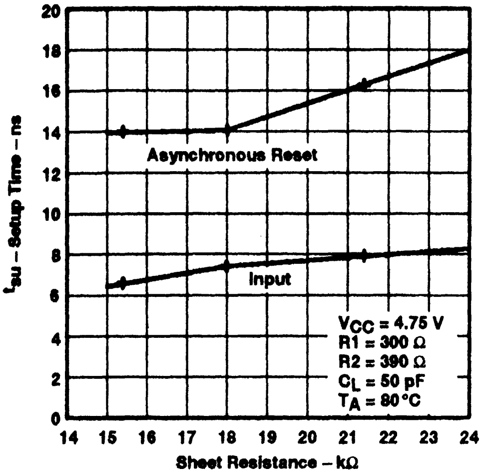
SETUP TIME
vs
SHEET RESISTANCE



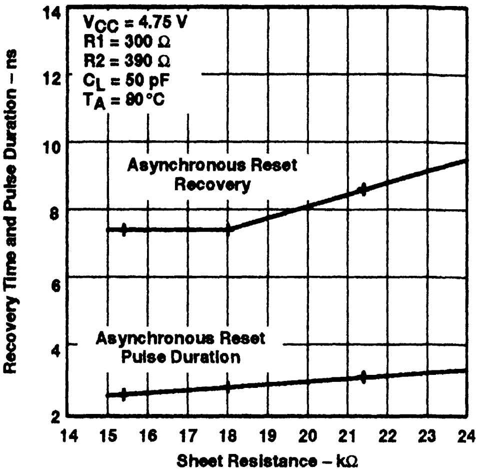
PROPAGATION DELAY TIME
(CLK to Q)
vs
SHEET RESISTANCE



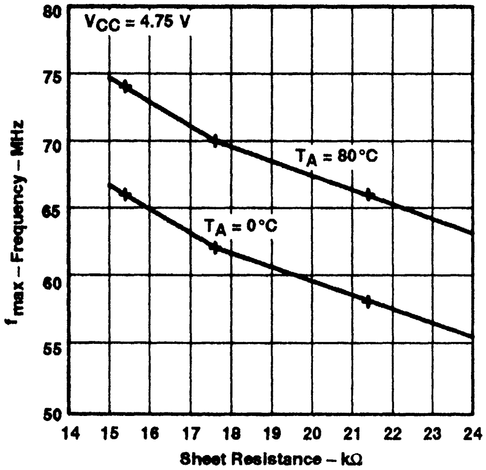
SETUP TIME
vs
SHEET RESISTANCE



ASYNCHRONOUS RESET
RECOVERY TIME and PULSE DURATION
vs
SHEET RESISTANCE



FREQUENCY
vs
SHEET RESISTANCE



IMPACT-X Programmable Sequencers

Devices included in this section:

TIBPLS506AC
TIBPSG507AC

DEVICE INFORMATION

IMPACT-X Programmable Sequencers

1. Technology .... IMPACT-X
2. Package Types : .... 24-pin plastic DIP,
   24-pin ceramic DIP,
   28-pin plastic PLCC
3. Last Die Revision .... B
4. Bar Size .... 125 x 173 mils
5. Still Air Thermal Impedance :

	PDIP	**CDIP**	**PLCC**
$R_{\theta JA}$	70.4	62.1	94.1
$R_{\theta JC}$	25.7	13.6	20.6

6. $R_{\theta JA}$ with Air Flow :

FPM	**PDIP**	**CDIP**	**PLCC**
0	83.0	66.4	83.3
100	63.0	49.6	57.9
250	46.0	39.1	46.4
500	38.0	31.5	35.3
750		27.8	28.8
1000			25.4

QUALIFICATION INFORMATION

The programmable sequencers are qualified using the standard qualification program. The following summaries give the required tests and results for this device and any additional test performed for additional data.

Required Tests and Results for PLS506A and PSG507A

Device Type: PLS506A
Package Type: 24 pin PDIP
Die Lot Number: 9137700

TEST	SS/F	ENDPOINT	RESULTS	EXTENDED READPOINT	RESULTS
150°C Dynamic Op-Life	129/1	384 HRS	129/0[1]		
125°C Dynamic Op-Life	129/1	1000 HRS	128/0[2]	2000 HRS	128/0
130°C/85% RH HAST	129/1	100 HRS	129/0	500 HRS	129/0
–65°C/150°C Temp Cycle	129/1	1000 CYC	129/1[3]		
–65°C/150°C Thermal Shock	129/1	200 CYC	129/0	1000 CYC	129/0
Autoclave	77/1	240 HRS	77/0	384 HRS	77/0
ESD	3/0	2000 V	6/0		

1. 1 unit mechanically damaged, broken lead, unable to test - removed from population.
2. EOS damage due to reverse socket insertion - removed from population. TI FA Report # D12-00423
3. Fuse Defect. TI FA Report # D12-00413

Required Tests and Results for PLS506A and PSG507A Rev B Process Change

Device Type: PSG507A
Package Type: 24 pin PDIP
Die Lot Numbers: 0206608 and 1027230

TEST	SS/F	ENDPOINT	RESULTS
125°C Dynamic Op-Life	116/0	1000 HRS	116/0
130°C/85% RH HAST	129/1	200 HRS	150/1[1]
–65°C/150°C Thermal Shock	129/1	1000 CYC	231/0

Device Type: PLS506A
Package Type: 24 pin PDIP
Die Lot Number: 1031145

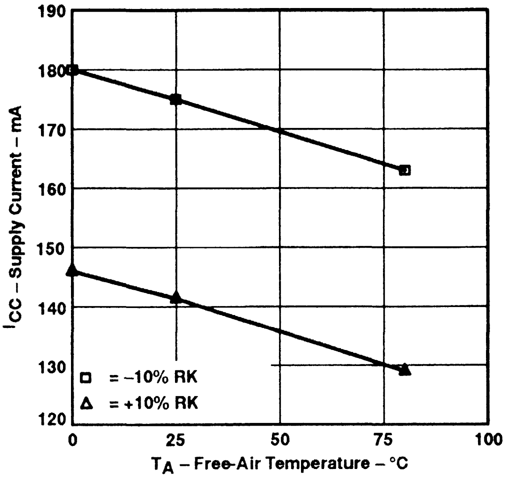
TEST	SS/F	ENDPOINT	RESULTS
125°C Dynamic Op-Life	116/0	1000 HRS	116/0
130°C/85% RH HAST	77/0	200 HRS	77/0
–65°C/150°C Thermal Shock	77/0	1000 CYC	116/0

1. Bond wire short due to excessive wire sweep. TI FA Report # D00-10541

CHARACTERIZATION INFORMATION

TIBPLS506AC and TIBPSG507AC

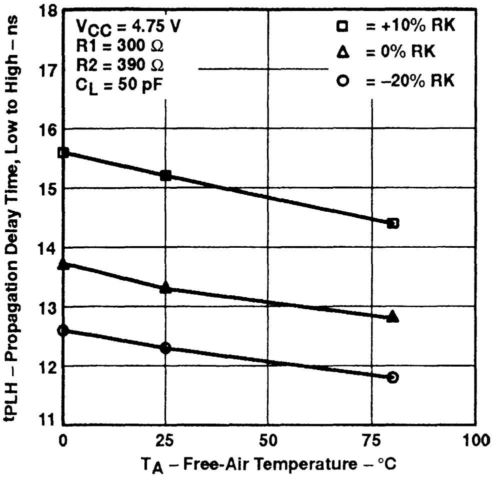
The typical RK values for TIBPLS506AC and TIBPSG507AC range from −10% to +10%. RK values beyond this range are shown in the following graphs.



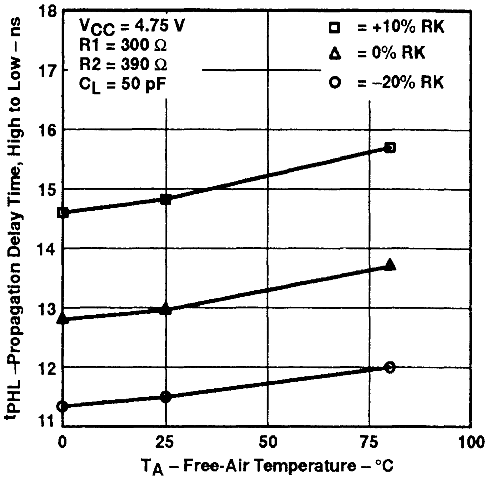
SUPPLY CURRENT
vs
FREE-AIR TEMPERATURE

TIBPLS506A and TIBPSG507A (continued)

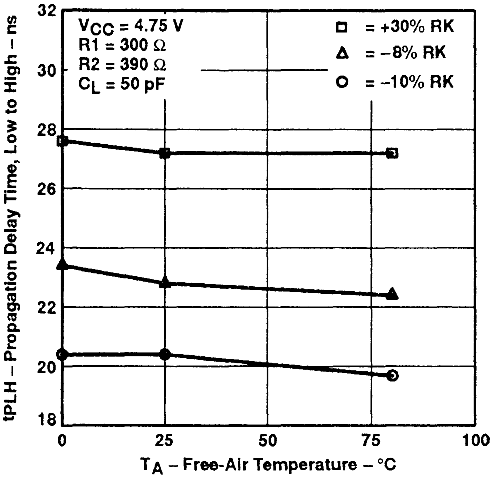
PROPAGATION DELAY TIME
t_{PLH} from I to Q (nonregistered)
vs
FREE-AIR TEMPERATURE



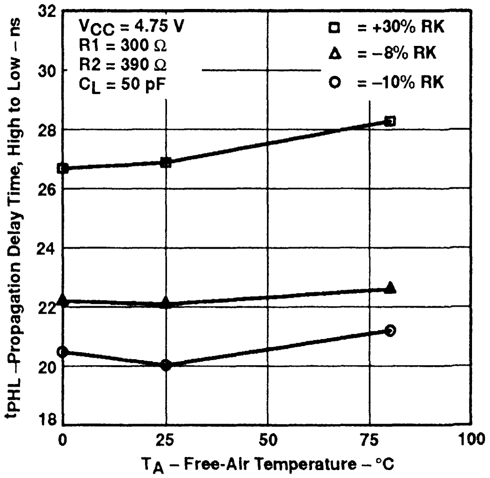
PROPAGATION DELAY TIME
t_{PHL} from I to Q (nonregistered)
vs
FREE-AIR TEMPERATURE



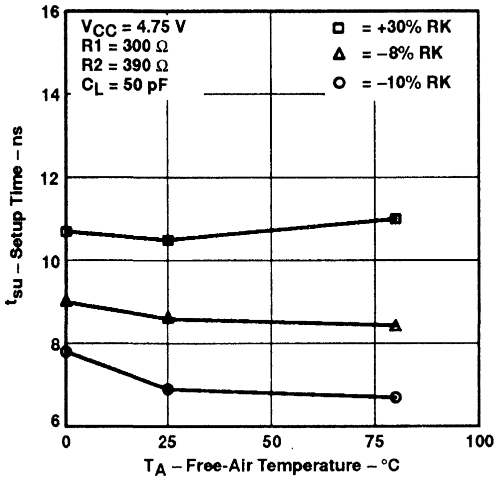
PROPAGATION DELAY TIME
t_{PLH} from I to Q (nonregistered) with C-array
vs
FREE-AIR TEMPERATURE



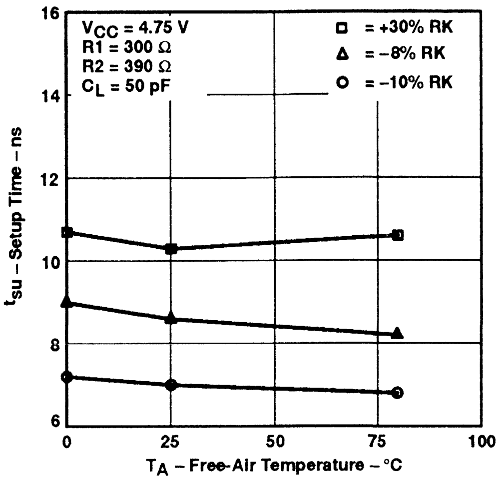
PROPAGATION DELAY TIME
t_{PHL} from I to Q (nonregistered) with C-array
vs
FREE-AIR TEMPERATURE



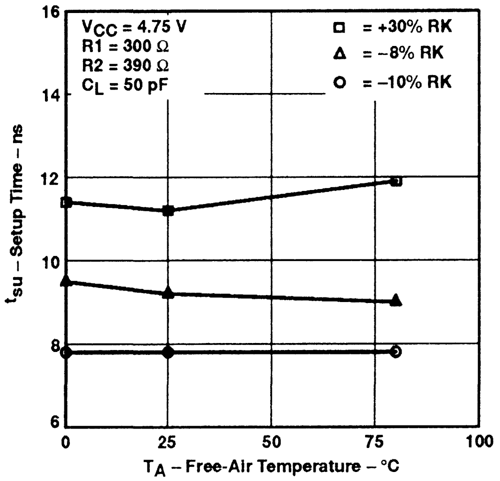
OUTPUT REGISTER SETUP TIME
(Input or feedback to S/R inputs before CLK ↑)
vs
FREE-AIR TEMPERATURE



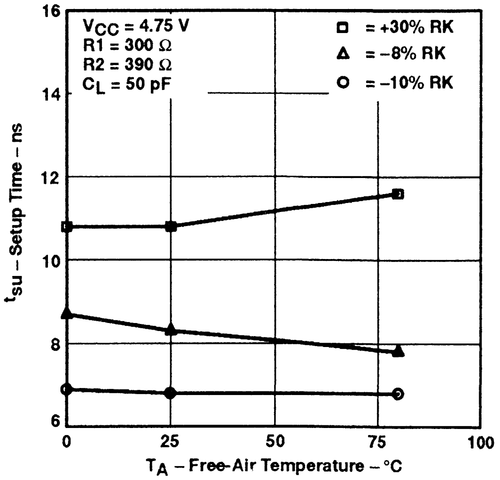
OUTPUT REGISTER SETUP TIME
(Input or feedback to S/R inputs before CLK ↓)
vs
FREE-AIR TEMPERATURE



BURIED REGISTER SETUP TIME
(Input or feedback to S/R inputs before CLK ↑)
vs
FREE-AIR TEMPERATURE

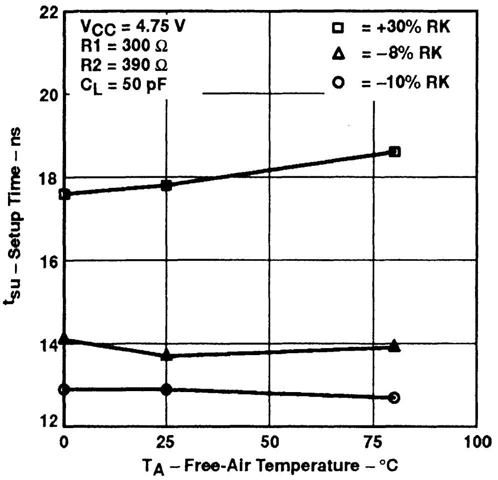


BURIED REGISTER SETUP TIME
(Input or feedback to S/R inputs before CLK ↓)
vs
FREE-AIR TEMPERATURE

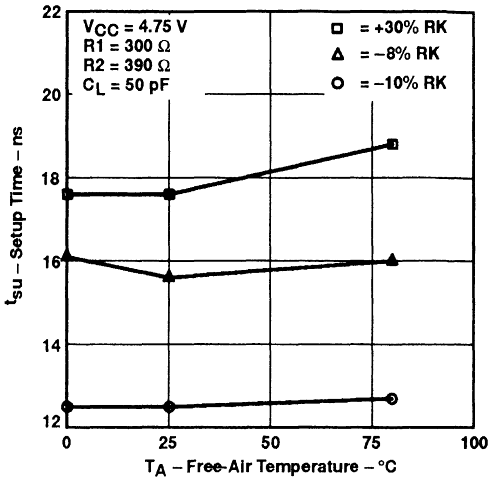


TIBPLS506A and TIBPSG507A (continued)

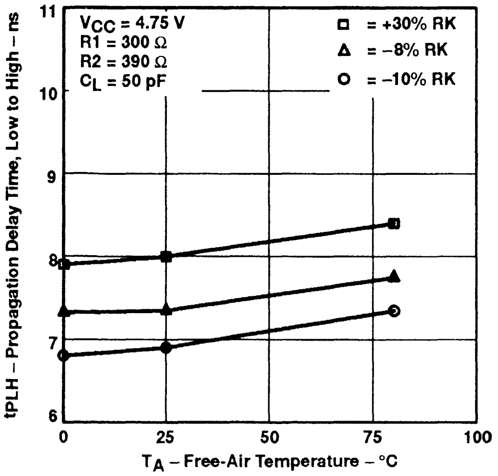
OUTPUT REGISTER SETUP TIME
(Input or feedback with C-array
to S/R inputs before CLK ↑)
vs
FREE-AIR TEMPERATURE



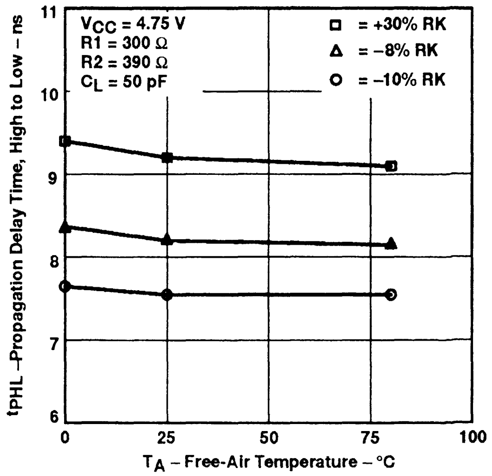
OUTPUT REGISTER SETUP TIME
(Input or feedback with C-array
to S/R inputs before CLK ↓)
vs
FREE-AIR TEMPERATURE



PROPAGATION DELAY TIME
(t_{PLH} from CLK ↓ to Output Register Q)
vs
FREE-AIR TEMPERATURE

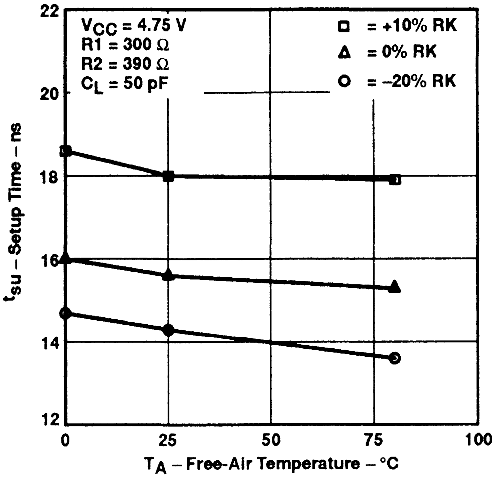


PROPAGATION DELAY TIME
(t_{PHL} from CLK ↓ to Output Register Q)
vs
FREE-AIR TEMPERATURE

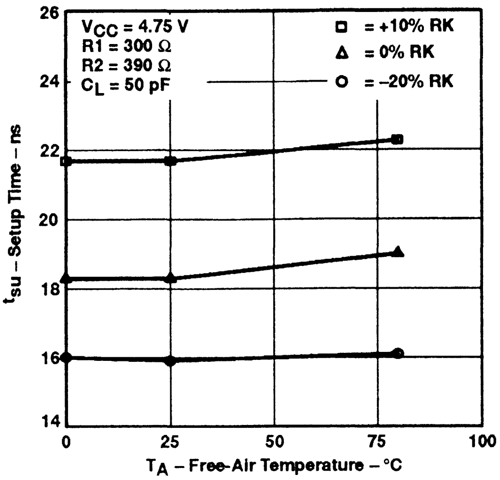


TIBPSG507A (only)

COUNTER SETUP TIME
(Input or feedback to SCLR0 before CLK ↓)
vs
FREE-AIR TEMPERATURE

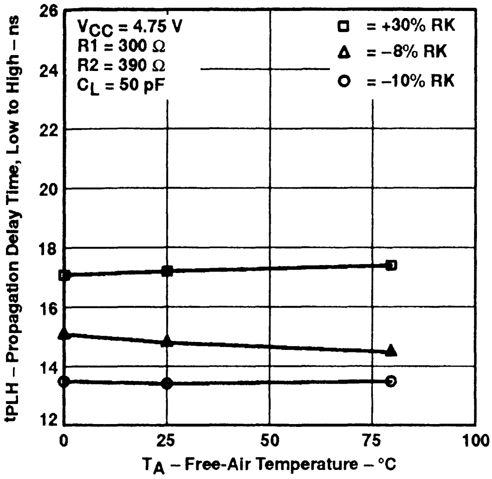


COUNTER SETUP TIME
(Input or feedback to $\overline{CNT}$/HLD0 before CLK ↓)
vs
FREE-AIR TEMPERATURE

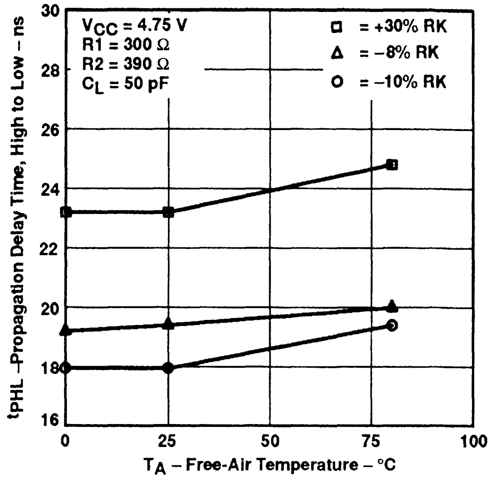


TIBPLS506A and TIBPSG507A (continued)

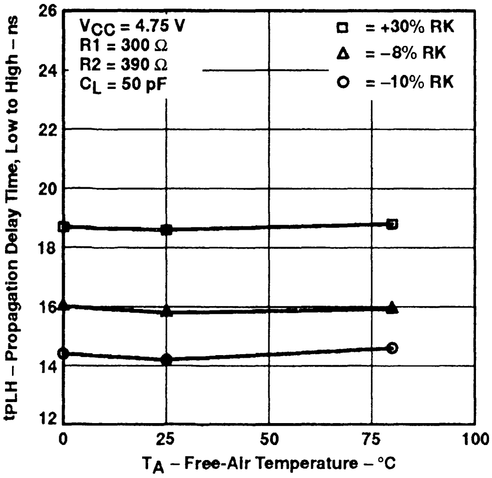
PROPAGATION DELAY TIME (t$_{PLH}$ from CLK ↑ to Buried Register Q) vs FREE-AIR TEMPERATURE



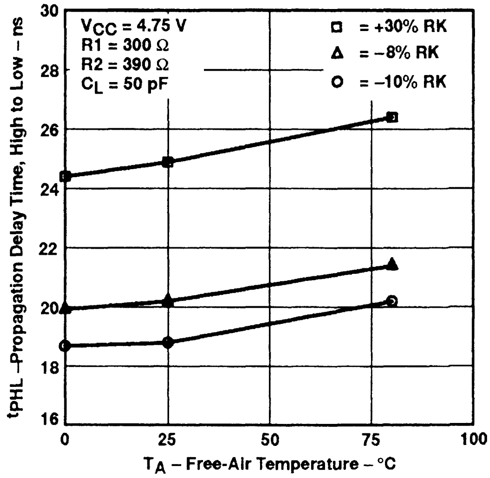
PROPAGATION DELAY TIME (t$_{PHL}$ from CLK ↑ to Buried Register Q) vs FREE-AIR TEMPERATURE



PROPAGATION DELAY TIME (t$_{PLH}$ from CLK ↓ to Buried Register Q) vs FREE-AIR TEMPERATURE

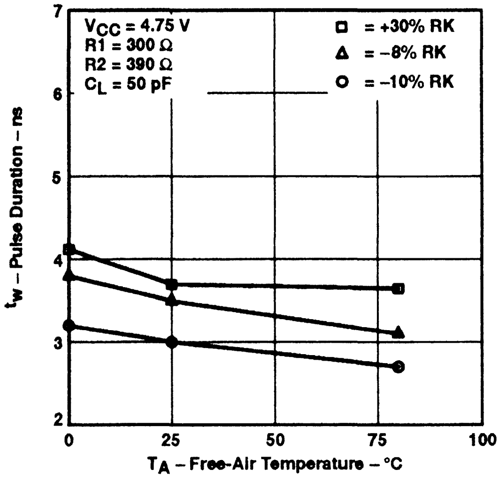


PROPAGATION DELAY TIME (t$_{PHL}$ from CLK ↓ to Buried Register Q) vs FREE-AIR TEMPERATURE

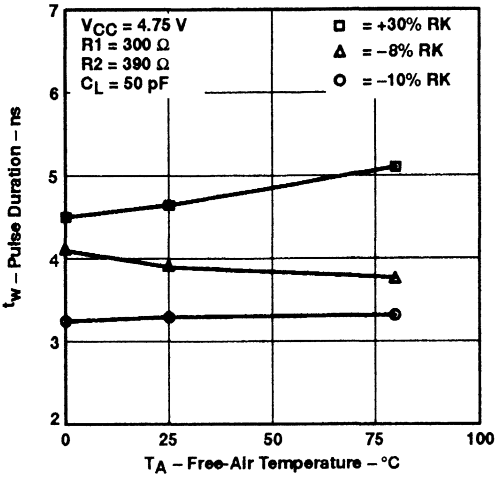


TIBPLS506A and TIBPSG507A (continued)

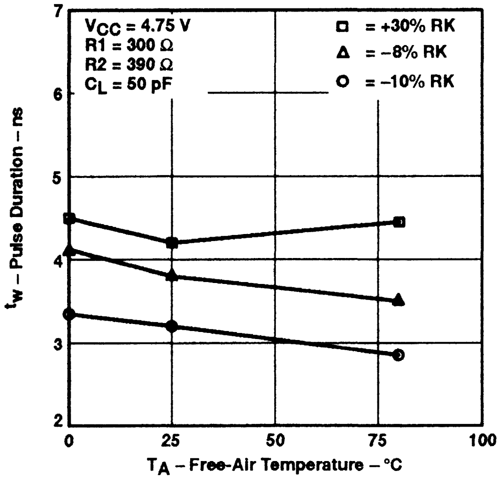
OUTPUT REGISTER PULSE DURATION (CLK high) vs FREE-AIR TEMPERATURE



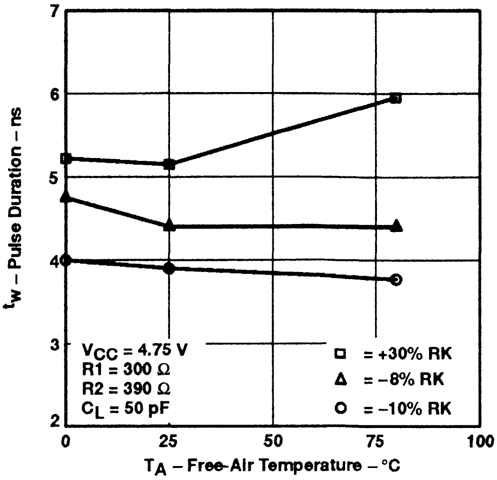
OUTPUT REGISTER PULSE DURATION (CLK low) vs FREE-AIR TEMPERATURE



BURIED REGISTER PULSE DURATION (CLK high) vs FREE-AIR TEMPERATURE

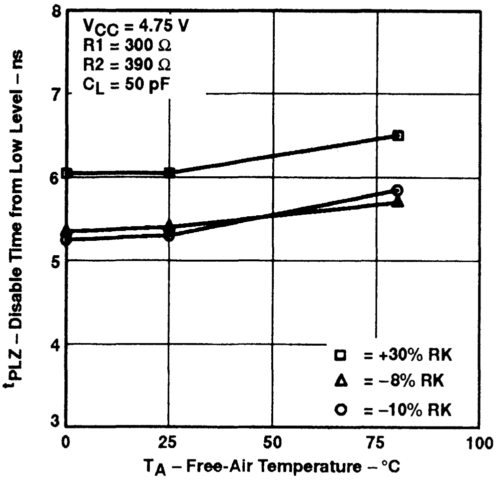


BURIED REGISTER PULSE DURATION (CLK low) vs FREE-AIR TEMPERATURE

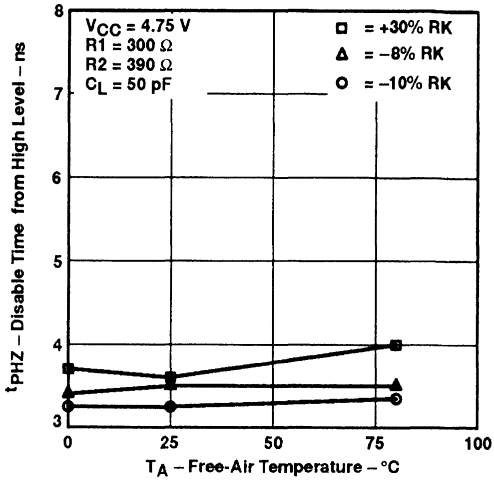


TIBPLS506A and TIBPSG507A (continued)

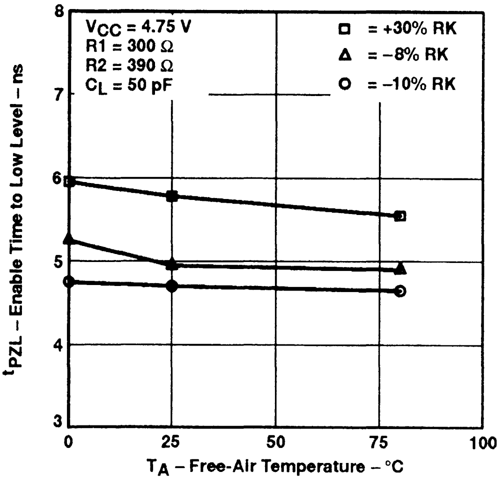
DISABLE TIME
(t_{PLZ} from $\overline{OE}$↑ to Q)
vs
FREE-AIR TEMPERATURE



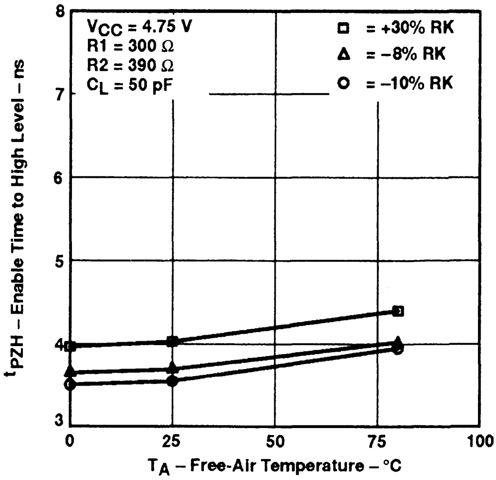
DISABLE TIME
(t_{PHZ} from $\overline{OE}$↑ to Q)
vs
FREE-AIR TEMPERATURE



ENABLE TIME
(t_{PZL} from $\overline{OE}$↓ to Q)
vs
FREE-AIR TEMPERATURE



ENABLE TIME
(t_{PZH} from $\overline{OE}$↓ to Q)
vs
FREE-AIR TEMPERATURE



TICPAL22V10Z

DEVICE INFORMATION

TICPAL22V10Z

1. Technology .... CMOS
2. Package Types : .... 24-pin plastic DIP,
   24-pin windowed ceramic DIP,
   28-pin plastic PLCC
3. Last Die Revision .... B
4. Bar Size .... 93 x 160 mils
5. Still Air Thermal Impedance :

	PDIP	**CDIP**	**PLCC**
$R_{\theta JA}$	70.4	62.1	95.1
$R_{\theta JC}$	25.7	13.6	21.5

6. $R_{\theta JA}$ with Air Flow :

FPM	**PDIP**	**CDIP**	**PLCC**
0	83.0	66.4	84.0
100	63.0	49.6	58.0
250	46.0	39.1	46.0
500	38.0	31.5	35.0
750		27.8	29.0
1000			25.0

QUALIFICATION INFORMATION

The TICPAL22V10Z device is qualified with the accelerated qualification program. The PLCC package needed additional qualification due to a change of mold compound. The following summaries give the required tests, results, and any additional testing performed for additional data.

Required Tests and Results for TICPAL22V10Z

Package Type:	24 pin PD
Date Code:	9013
Die Lot Number:	9333169

TEST	SS/F	ENDPOINT	RESULTS	EXTENDED READPOINT	RESULTS
150°C Dynamic Op-Life	129/1	413 HRS	129/1[1]		
125°C Dynamic Op-Life	129/1	168 HRS	129/1[2]	1000 HRS	128/0
130°C/85% RH HAST	129/1	100 HRS	129/0	200 HRS	129/0
–65°C/150°C Thermal Shock	77/1	200 CYC	77/0	1000 CYC	77/0
Autoclave	77/1	240 HRS	77/0		
Latchup	5/0		5/0		
ESD	3/0	2000 V	3/3[3]		
ESD		1500 V	3/2[3]		
ESD		1000 V	3/0		

Required Tests and Results for TICPAL22V10Z PLCC Package

Package Type:	28 pin PLCC
Date Code:	9033BL
Die Lot Number:	0089327

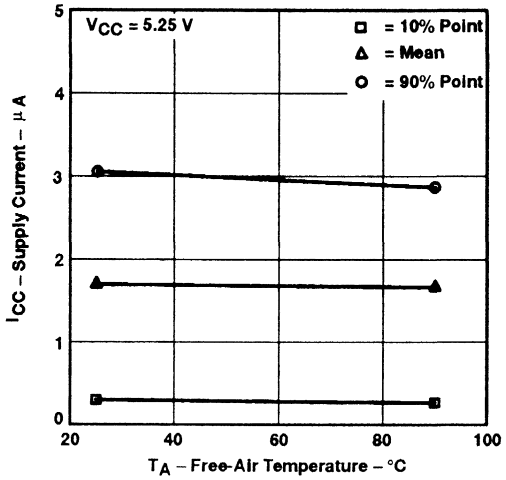
TEST	SS/F	ENDPOINT	RESULTS	EXTENDED READPOINT	RESULTS
150°C Storage Life	77/1	1000 HRS	77/0		
125°C Dynamic Op-Life	129/1	1000 HRS	129/0		
85°C/85% RH	129/1	1000 HRS	129/0		
–65°C/150°C Thermal Shock	77/1	200 CYC	77/0	1000 CYC	77/0
–65°C/150°C Temp Cycle	129/1	1000 CYC	129/0		
Autoclave	77/1	240 HRS	77/0	288 HRS	77/0
ESD		1000 V	3/0[3]		

1. Root cause of failure undetermined.
2. Failure due to particulate contamination of gate oxide. TI FA Report # D12-00526
3. Device released on 1 kV ESD waver.

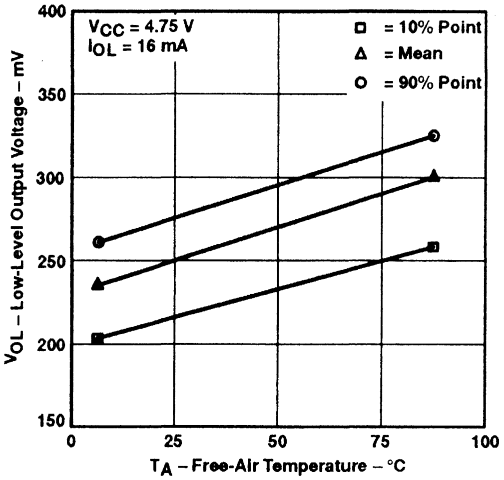
CHARACTERIZATION INFORMATION

TICPAL22V10Z

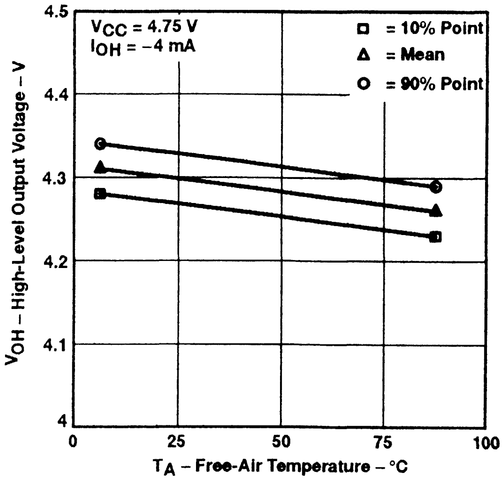
STANDBY SUPPLY CURRENT
(Zero-Power Mode)
vs
FREE-AIR TEMPERATURE



LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

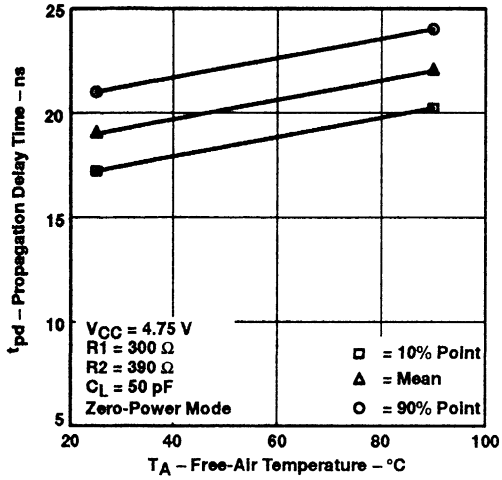


HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE

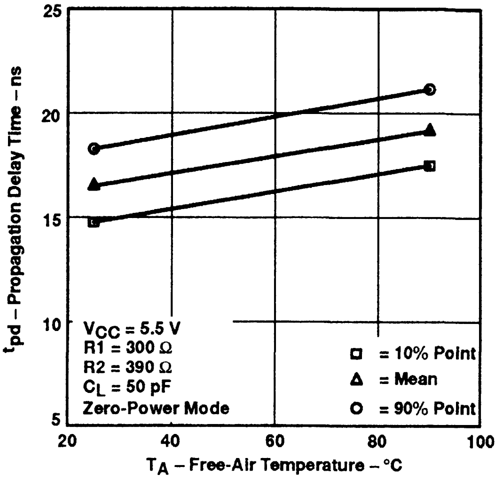


TICPAL22V10Z (continued)

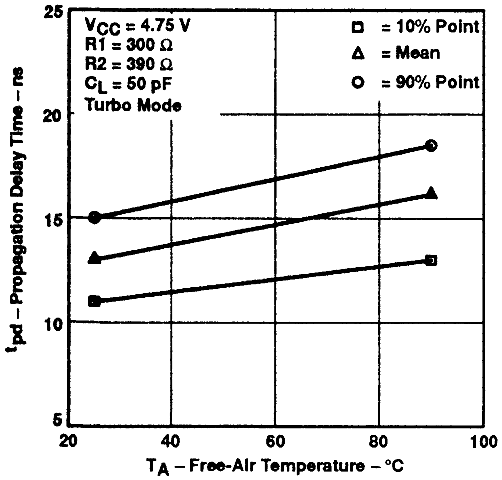
PROPAGATION DELAY TIME (I, I/O to O, I/O) vs FREE-AIR TEMPERATURE



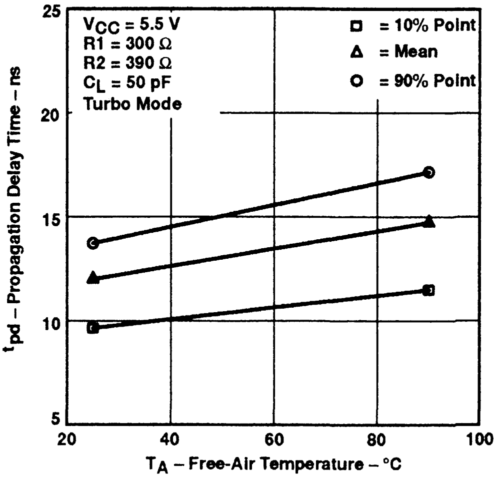
PROPAGATION DELAY TIME (I, I/O to O, I/O) vs FREE-AIR TEMPERATURE



PROPAGATION DELAY TIME (I, I/O to O, I/O) vs FREE-AIR TEMPERATURE

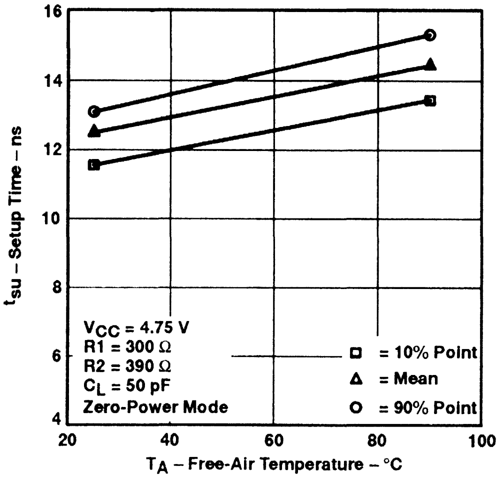


PROPAGATION DELAY TIME (I, I/O to O, I/O) vs FREE-AIR TEMPERATURE

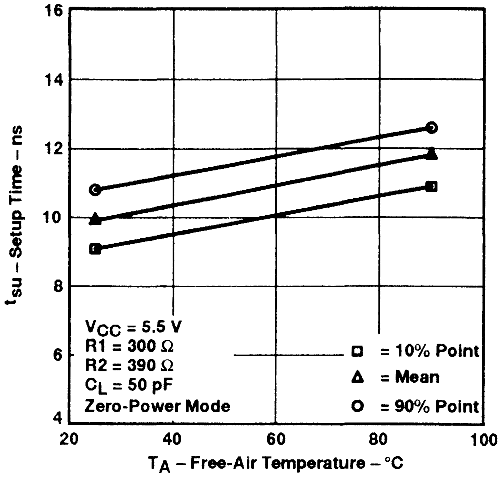


TICPAL22V10Z (continued)

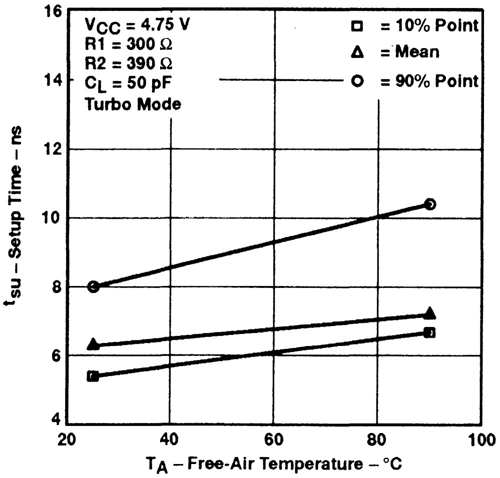
SETUP TIME
(Input or Feedback)
vs
FREE-AIR TEMPERATURE



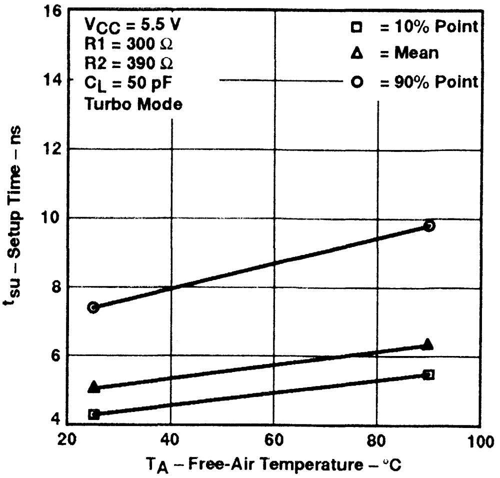
SETUP TIME
(Input or Feedback)
vs
FREE-AIR TEMPERATURE



SETUP TIME
(Input or Feedback)
vs
FREE-AIR TEMPERATURE

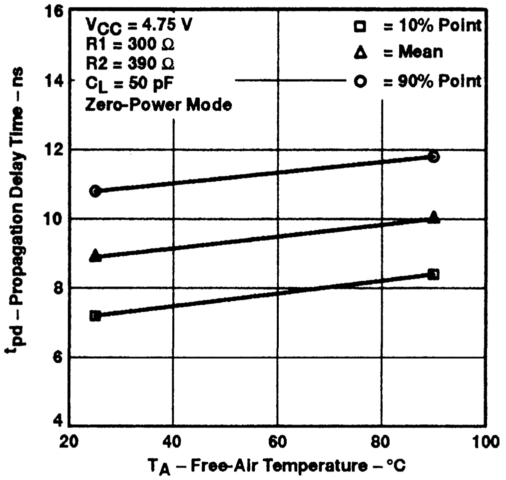


SETUP TIME
(Input or Feedback)
vs
FREE-AIR TEMPERATURE

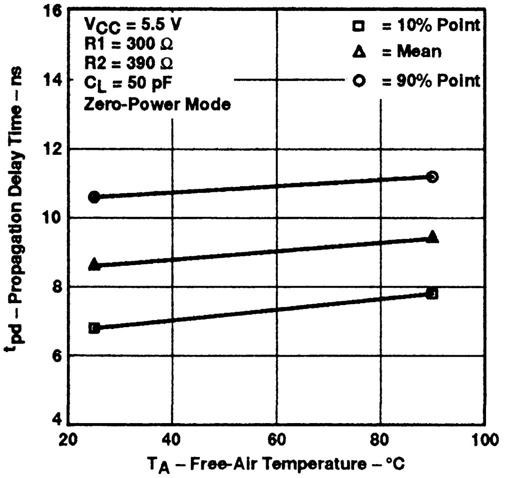


TICPAL22V10Z (continued)

PROPAGATION DELAY TIME (CLK to Q) vs FREE-AIR TEMPERATURE

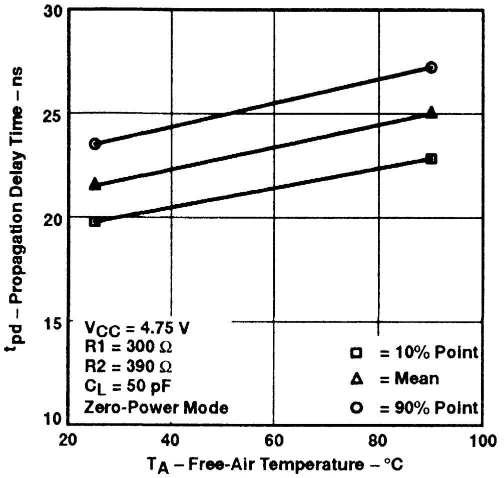


PROPAGATION DELAY TIME (CLK to Q) vs FREE-AIR TEMPERATURE

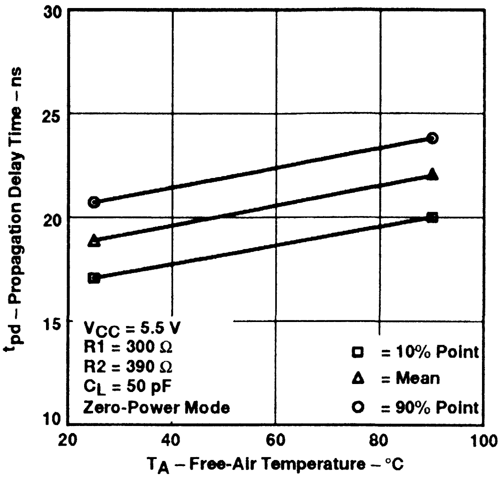


TICPAL22V10Z (continued)

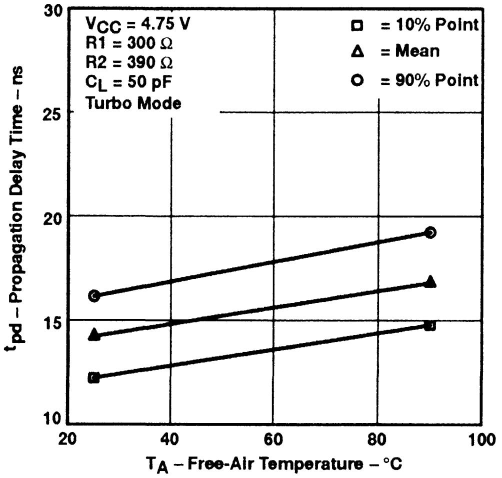
PROPAGATION DELAY TIME
(Asynchronous Reset to Q)
vs
FREE-AIR TEMPERATURE



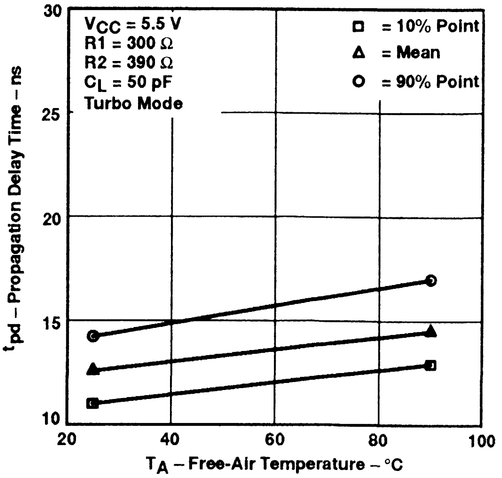
PROPAGATION DELAY TIME
(Asynchronous Reset to Q)
vs
FREE-AIR TEMPERATURE



PROPAGATION DELAY TIME
(Asynchronous Reset to Q)
vs
FREE-AIR TEMPERATURE

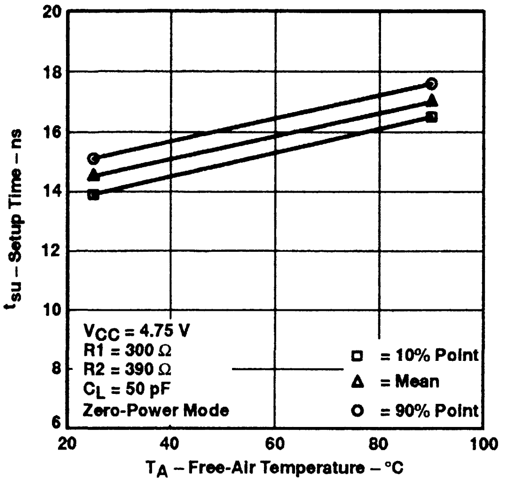


PROPAGATION DELAY TIME
(Asynchronous Reset to Q)
vs
FREE-AIR TEMPERATURE

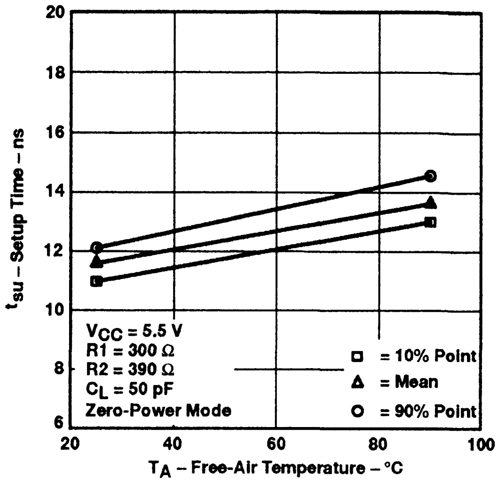


TICPAL22V10Z (continued)

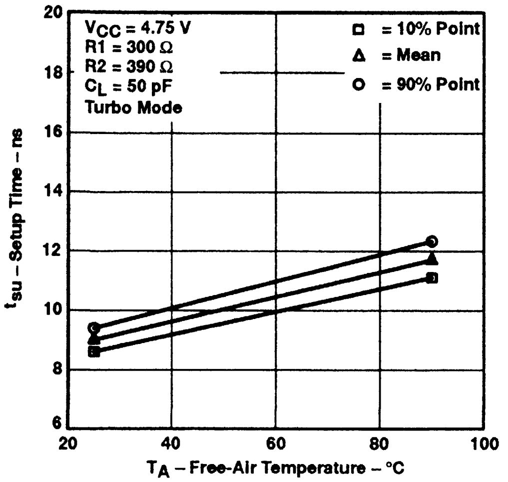
SETUP TIME
(Asynchronous Reset Inactive)
vs
FREE-AIR TEMPERATURE



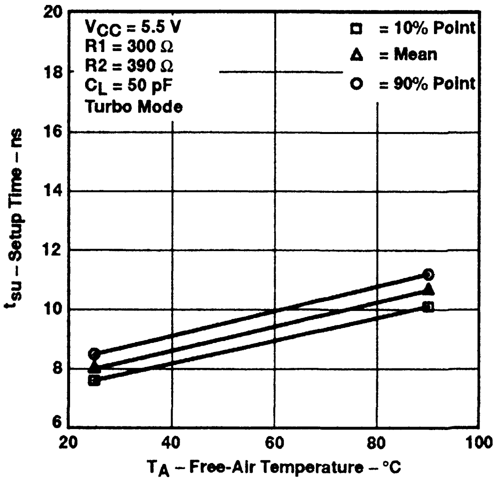
SETUP TIME
(Asynchronous Reset Inactive)
vs
FREE-AIR TEMPERATURE



SETUP TIME
(Asynchronous Reset Inactive)
vs
FREE-AIR TEMPERATURE

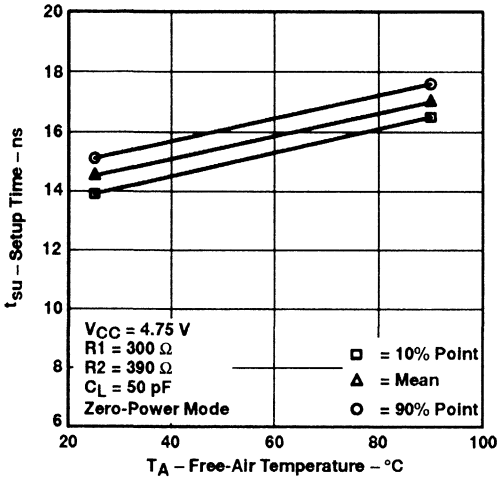


SETUP TIME
(Asynchronous Reset Inactive)
vs
FREE-AIR TEMPERATURE

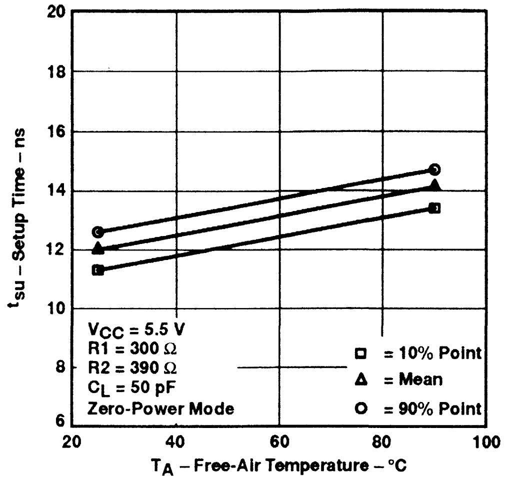


TICPAL22V10Z (continued)

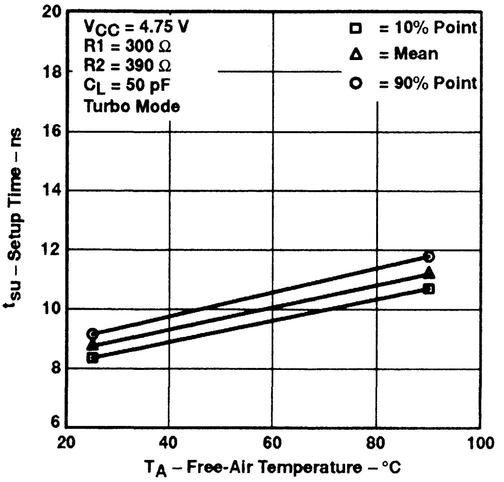
SETUP TIME
(Synchronous Preset Inactive)
vs
FREE-AIR TEMPERATURE



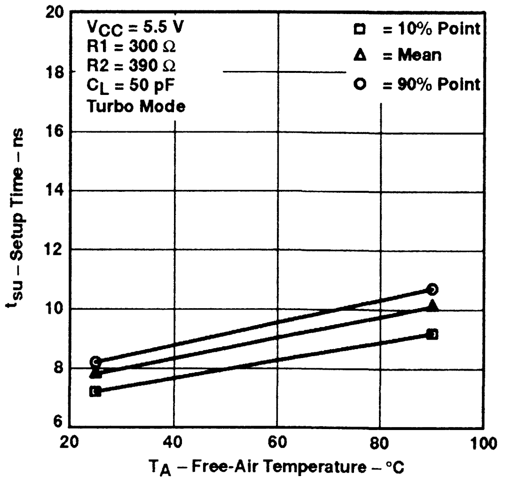
SETUP TIME
(Synchronous Preset Inactive)
vs
FREE-AIR TEMPERATURE



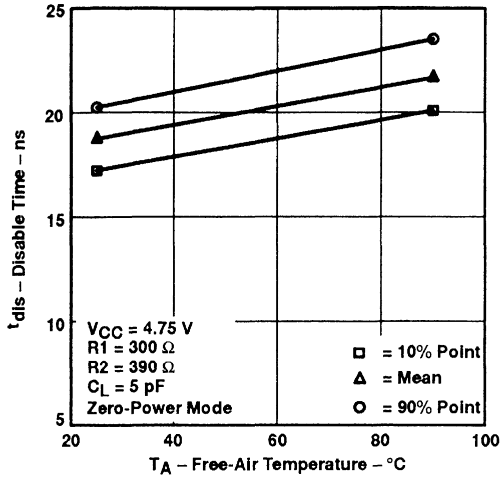
SETUP TIME
(Synchronous Preset Inactive)
vs
FREE-AIR TEMPERATURE

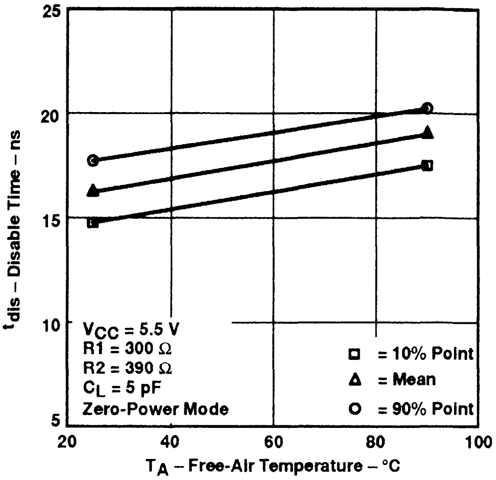


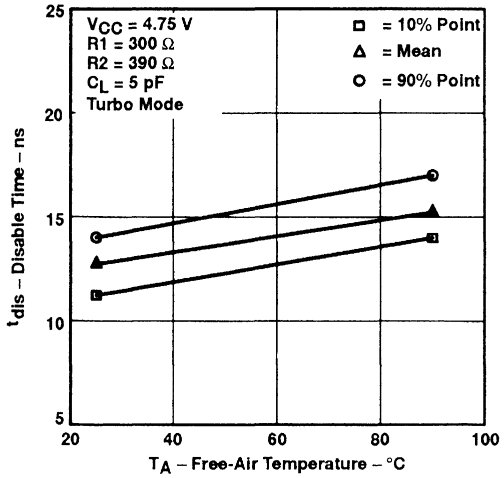
SETUP TIME
(Synchronous Preset Inactive)
vs
FREE-AIR TEMPERATURE

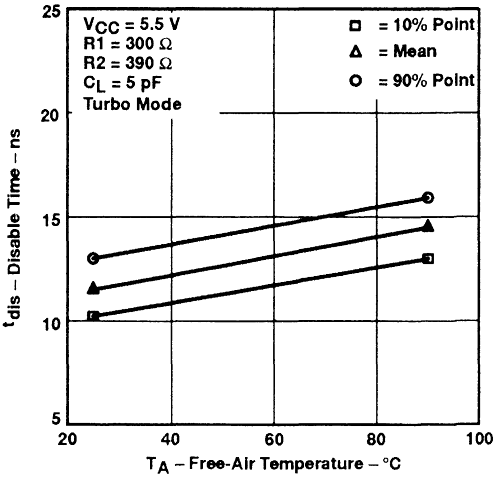


TICPAL22V10Z (continued)


DISABLE TIME
(I, I/O to O, I/O)
vs
FREE-AIR TEMPERATURE

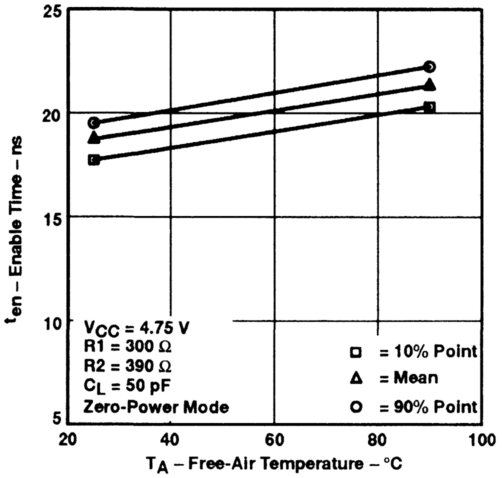

DISABLE TIME
(I, I/O to O, I/O)
vs
FREE-AIR TEMPERATURE


DISABLE TIME
(I, I/O to O, I/O)
vs
FREE-AIR TEMPERATURE

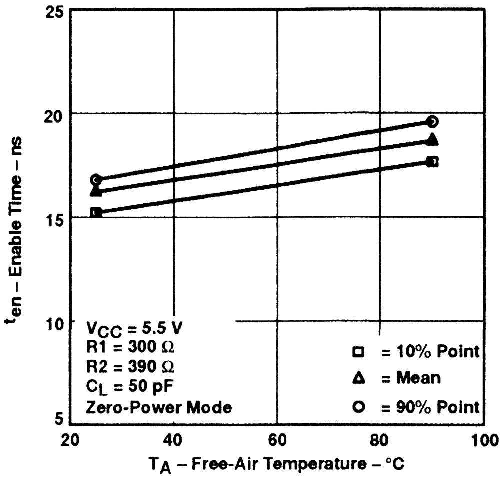

DISABLE TIME
(I, I/O to O, I/O)
vs
FREE-AIR TEMPERATURE

TICPAL22V10Z (continued)

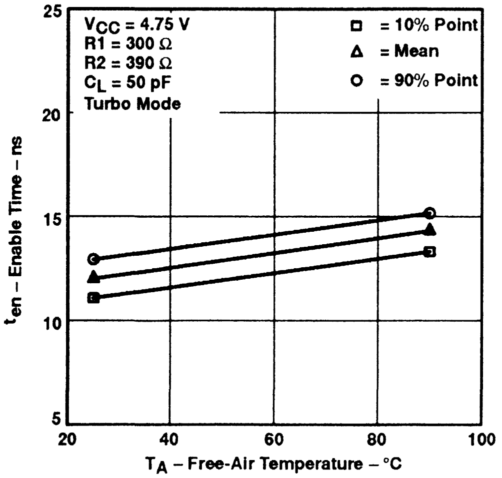
ENABLE TIME (I, I/O to O, I/O) vs FREE-AIR TEMPERATURE



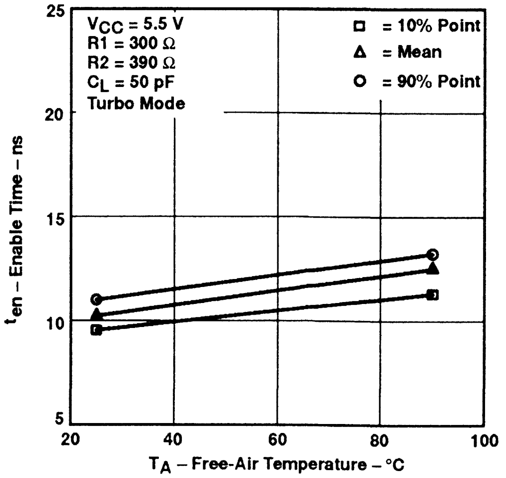
ENABLE TIME (I, I/O to O, I/O) vs FREE-AIR TEMPERATURE



ENABLE TIME (I, I/O to O, I/O) vs FREE-AIR TEMPERATURE



ENABLE TIME (I, I/O to O, I/O) vs FREE-AIR TEMPERATURE



EP330

DEVICE INFORMATION

EP330

1. Technology .... CMOS
2. Package Types : .... 20-pin plastic DIP,
   20-pin plastic PLCC
3. Last Die Revision .... A
4. Bar Size : .... 86 x 106 mils
5. Still Air Thermal Impedance :

	PDIP	**PLCC**
$R_{\theta JA}$	75.2	105.5
$R_{\theta JC}$	35.4	31.0

6. $R_{\theta JA}$ with Air Flow :

FPM	**PDIP**	**PLCC**
0	92.6	103.5
100	73.5	82.2
250	55.4	64.6
500	47.5	51.7

QUALIFICATION INFORMATION

The EP330 device is qualified using the accelerated qualification program. The following summaries give the required tests and results for this device and any additional test performed for additional data.

This device is released on waver due to ESD failures over 1000 V.

Required Tests and Results for EP330

Package Type: 20 pin PDIP
Die Lot Numbers: 0158622 and 0197535

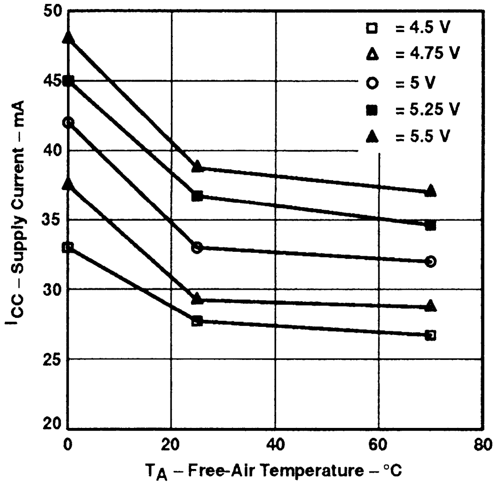
TEST	SS/F	ENDPOINT	RESULTS	EXTENDED READPOINT	RESULTS
150°C Dynamic Op-Life	129/1	413 HRS	129/0		
125°C Dynamic Op-Life	129/1	168 HRS	129/0		
130°C/85% RH HAST	129/1	100 HRS	129/0	200 HRS	129/0
–65°C/150°C Thermal Shock	77/1	200 CYC	77/0		
Latchup	5/0		5/0		
ESD	3/0	2000 V	3/3[1]		
ESD		1000 V	3/0		

1. Device released on 1 kV ESD waver.

CHARACTERIZATION INFORMATION

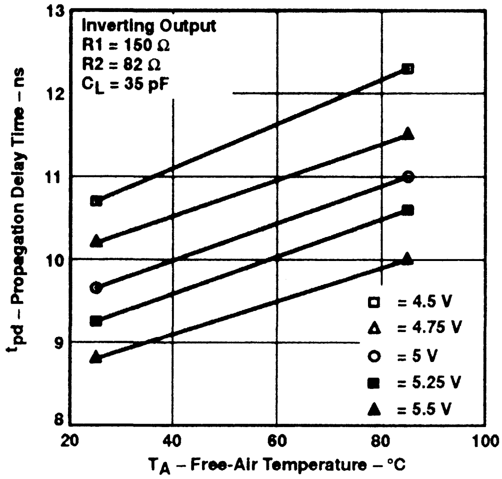
EP330

SUPPLY CURRENT
(Programmed as a 8-Bit Counter)
vs
FREE-AIR TEMPERATURE

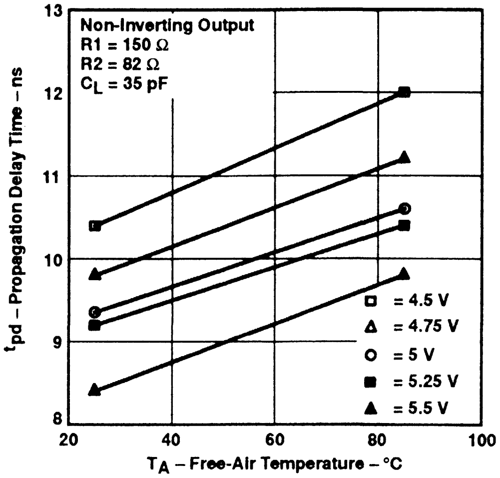


EP330 (continued)

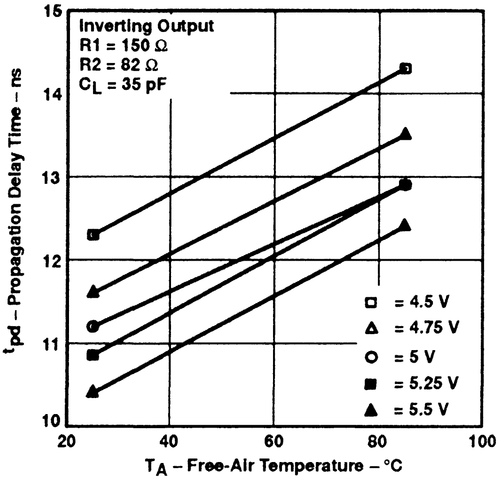
PROPAGATION DELAY TIME (Input to Nonregistered Output Delay) vs FREE-AIR TEMPERATURE



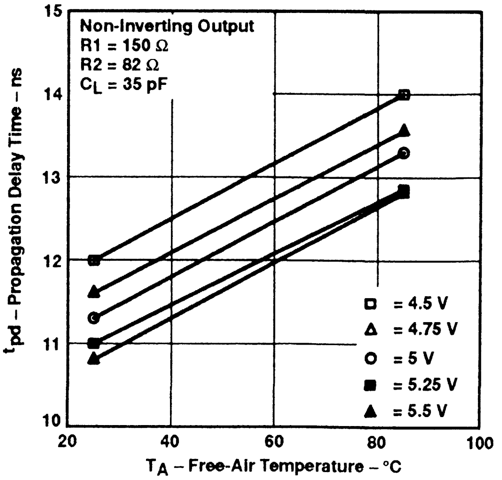
PROPAGATION DELAY TIME (Input to Nonregistered Output Delay) vs FREE-AIR TEMPERATURE



PROPAGATION DELAY TIME (I/O to Nonregistered Output Delay) vs FREE-AIR TEMPERATURE

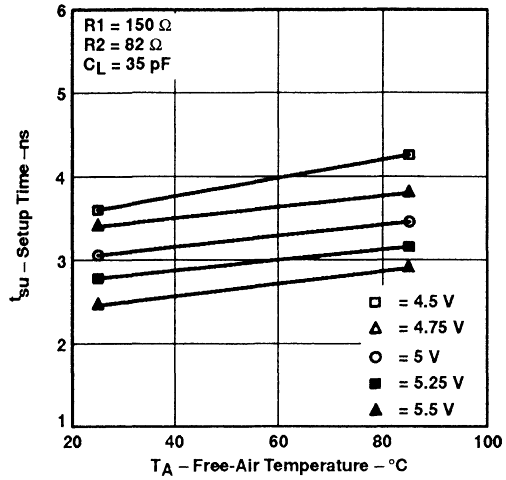


PROPAGATION DELAY TIME (I/O to Nonregistered Output Delay) vs FREE-AIR TEMPERATURE

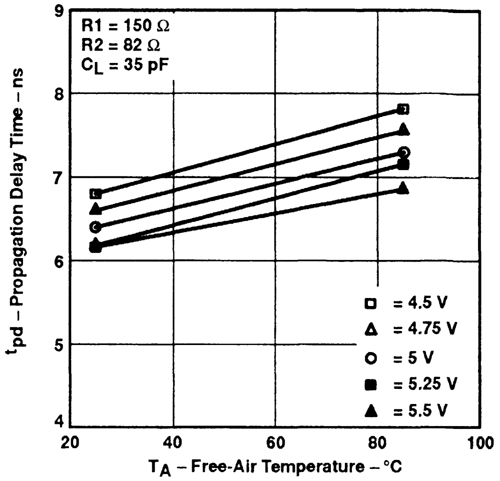


EP330 (continued)

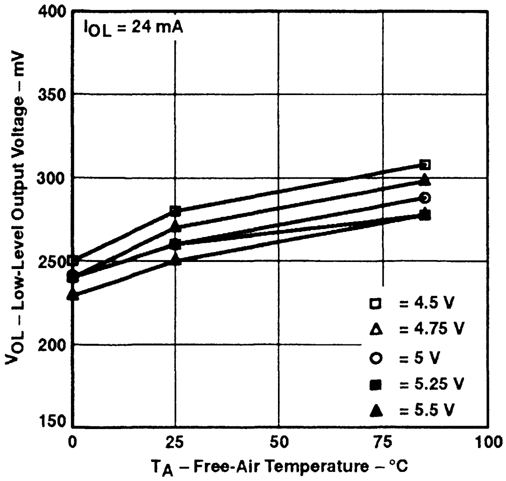
SETUP TIME
vs
FREE-AIR TEMPERATURE



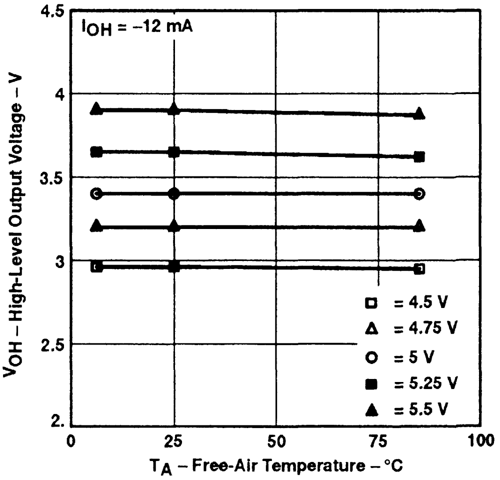
PROPAGATION DELAY TIME
(Clock Input to Registered Output Delay)
vs
FREE-AIR TEMPERATURE



LOW-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE



HIGH-LEVEL OUTPUT VOLTAGE
vs
FREE-AIR TEMPERATURE



EP630

DEVICE INFORMATION

EP630

1. Technology .... CMOS
2. Package Types : .... 24-pin plastic DIP, 28-pin plastic PLCC
3. Last Die Revision .... F
4. Bar Size .... 108 x 134 mils
5. Still Air Thermal Impedance :

	PDIP	**PLCC**
$R_{\theta JA}$	71.5	99.5
$R_{\theta JC}$	31.2	27.0

6. $R_{\theta JA}$ with Air Flow :

FPM	**PDIP**	**PLCC**
0	82.6	92.9
100	62.8	69.6
250	46.3	61.0
500	37.6	50.1
750		44.2
1000		41.0

QUALIFICATION INFORMATION

The EP630 device is qualified using the accelerated qualification program. The following summaries give the required tests and results for this device and any additional test performed for additional data.

This device is released on waver due to ESD failures over 1000 V.

Required Tests and Results for EP630

Package Type: 24 pin PDIP
Date Code: 031DL
Die Lot Number: 0060736

TEST	SS/F	ENDPOINT	RESULTS	EXTENDED READPOINT	RESULTS
150°C Dynamic Op-Life	129/1	433 HRS	129/0		
125°C Dynamic Op-Life	129/1	168 HRS	129/0	1000 HRS	129/0
130°C/85% RH HAST	129/1	100 HRS	129/0	200 HRS	129/0
–65°C/150°C Thermal Shock	77/1	100 CYC	77/0	200 CYC	77/0
Latchup	5/0		5/0		
ESD	3/0	2000 V	3/3[1]		
ESD		1000 V	3/0		

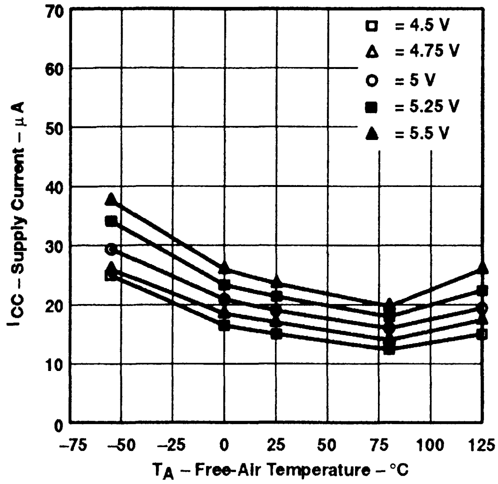
[1] Device released on 1 kV ESD waver.

CHARACTERIZATION INFORMATION

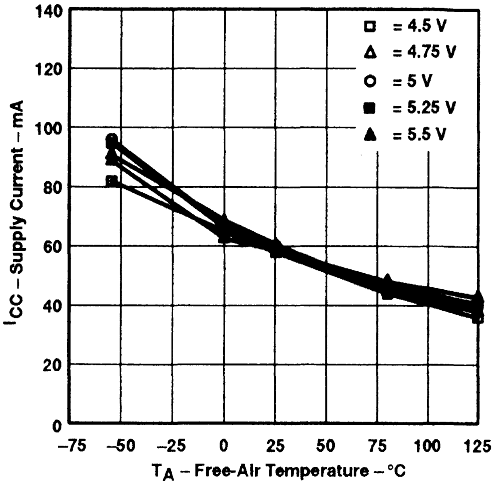
EP630

EP630

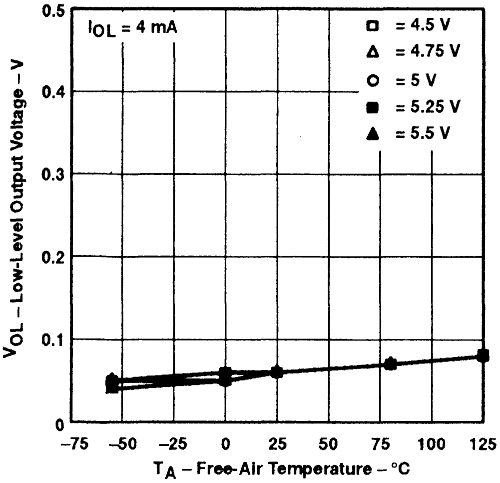
SUPPLY CURRENT (Standby Mode) vs FREE-AIR TEMPERATURE



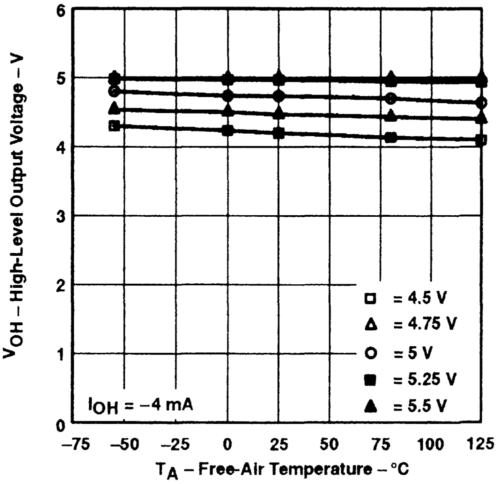
SUPPLY CURRENT (Turbo Mode) vs FREE-AIR TEMPERATURE



LOW-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

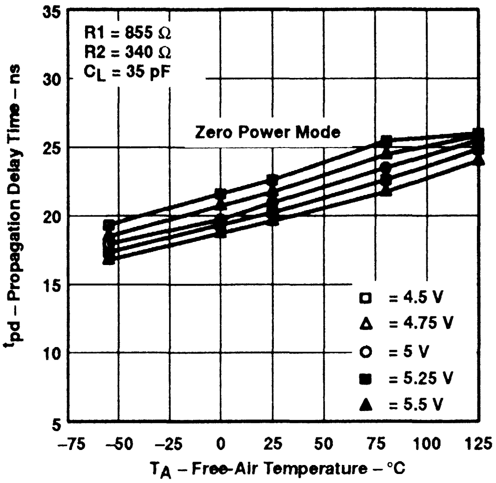


HIGH-LEVEL OUTPUT VOLTAGE vs FREE-AIR TEMPERATURE

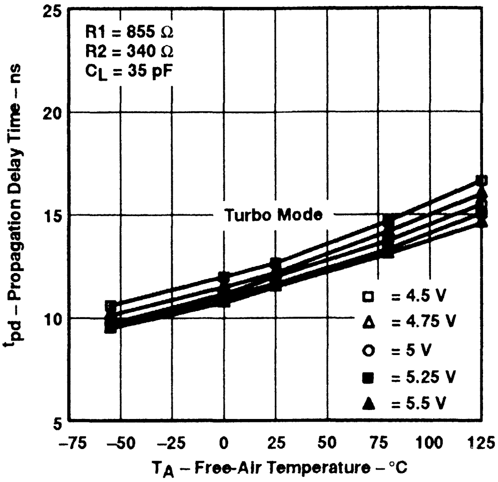


EP630 (continued)

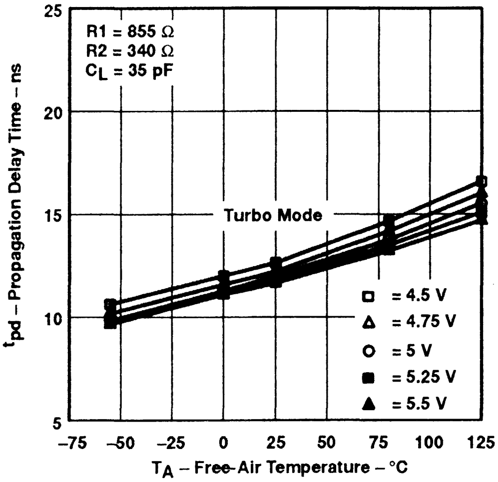
PROPAGATION DELAY TIME (Input to Nonregistered Output Delay) vs FREE-AIR TEMPERATURE



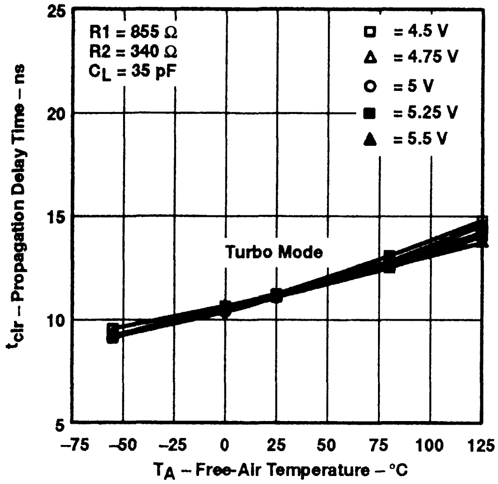
PROPAGATION DELAY TIME (Input to Nonregistered Output Delay) vs FREE-AIR TEMPERATURE

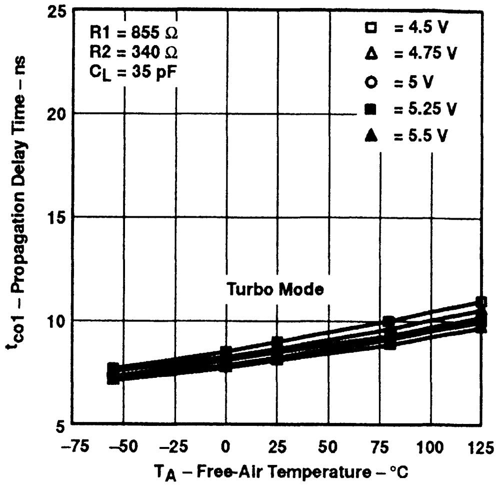


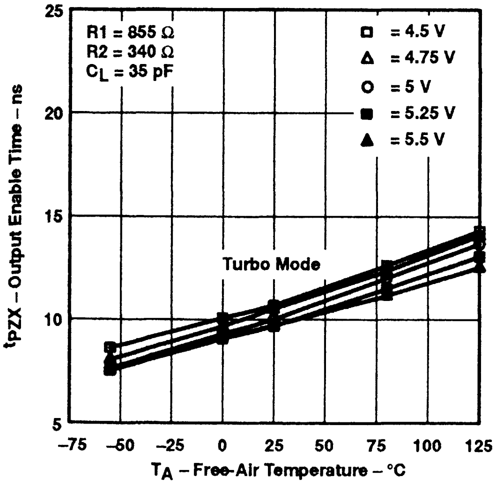
PROPAGATION DELAY TIME (I/O Input to nonregistered Output delay) vs FREE-AIR TEMPERATURE

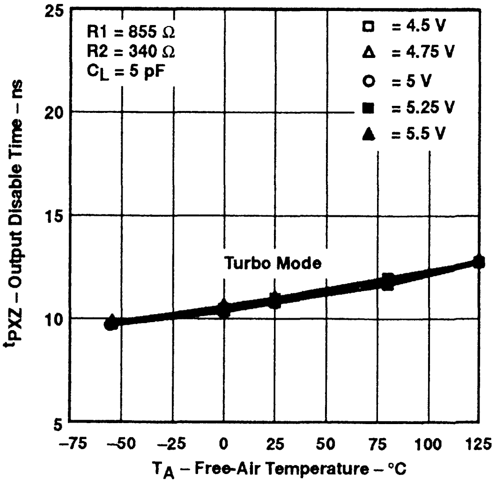


EP630 (continued)


PROPAGATION DELAY TIME
(Asynchronous Output Clear Time)
vs
FREE-AIR TEMPERATURE


PROPAGATION DELAY TIME
(Clock to Output Delay Time)
vs
FREE-AIR TEMPERATURE


OUTPUT ENABLE TIME
vs
FREE-AIR TEMPERATURE


OUTPUT DISABLE TIME
vs
FREE-AIR TEMPERATURE

EP1830

DEVICE INFORMATION

EP1830

1. Technology .... CMOS
2. Package Types : .... 68-pin plastic PLCC
3. Last Die Revision C
4. Bar Size .... 305 x 133 mils
5. Still Air Thermal Impedance :

	PLCC
$R_{\theta JA}$	49.7
$R_{\theta JC}$	11.4

6. $R_{\theta JA}$ with Air Flow :

FPM	**PLCC**
100	43.4
250	32.7
500	27.8

QUALIFICATION INFORMATION

The EP1830 device is qualified using the accelerated qualification program. The following summaries give the required tests and results for this device and any additional test performed for additional data.

This device is released on waver due to ESD failures over 1000 V.

Required Tests and Results for EP1830

Package Type:	68 pin PLCC
Date Code:	129AL
Die Lot Number:	1155252

TEST	**SS/F**	**ENDPOINT**	**RESULTS**	**EXTENDED READPOINT**	**RESULTS**
125°C Dynamic Op-Life	77/0	1000 HRS	77/0		
130°C/85% RH HAST	129/1	100 HRS	129/0	200 HRS	129/0
–65°C/150°C Thermal Shock	77/1	100 CYC	77/0	200 CYC	77/0
–65°C/150°C Temp Cycle	77/1	1000 CYC	77/0		
Latchup	5/0		5/0		
ESD	3/0	2000 V	3/3[1]		
ESD		1000 V	3/0		

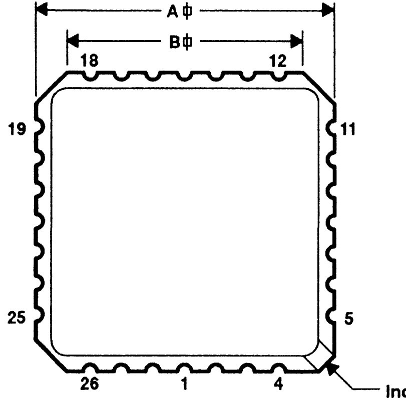
1. Device released on 1 kV ESD waver.

FK020 and FK028 ceramic chip carrier packages

Each of these hermetically sealed chip carrier packages has a three-layer ceramic base with a metal lid and braze seal. The packages are intended for surface mounting on solder lands on 1,27 (0.050) centers. Terminals require no additional cleaning or processing when used in soldered assembly.

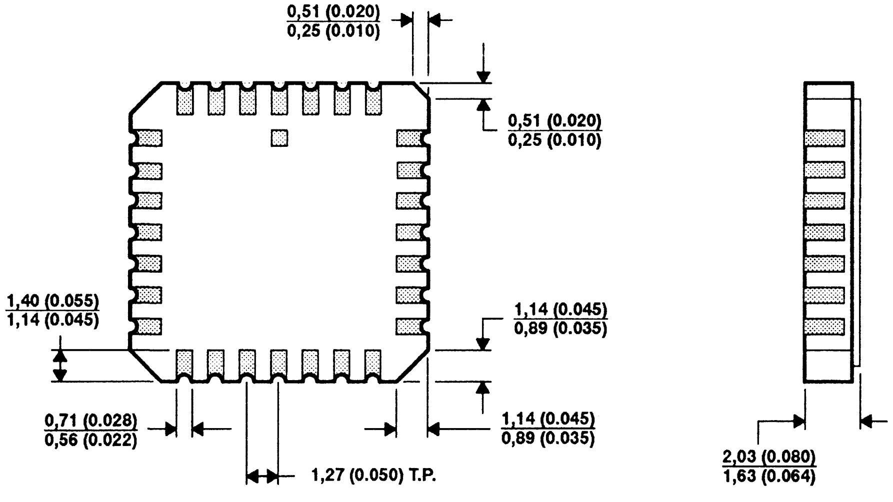
FK package terminal assignments conform to JEDEC Standards 1 and 2.

FK020 and FK028
(28-pin used for illustration)



JEDEC OUTLINE DESIGNATION†	NO. OF TERMINALS	A MIN	A MAX	B MIN	B MAX
MS004CB	20	8,69 (0.342)	9,09 (0.358)	7,80 (0.307)	9,09 (0.358)
MS004CC	28	11,23 (0.442)	11,63 (0.458)	10,31 (0.406)	11,63 (0.458)

† All dimensions and notes for the specified JEDEC outline apply.

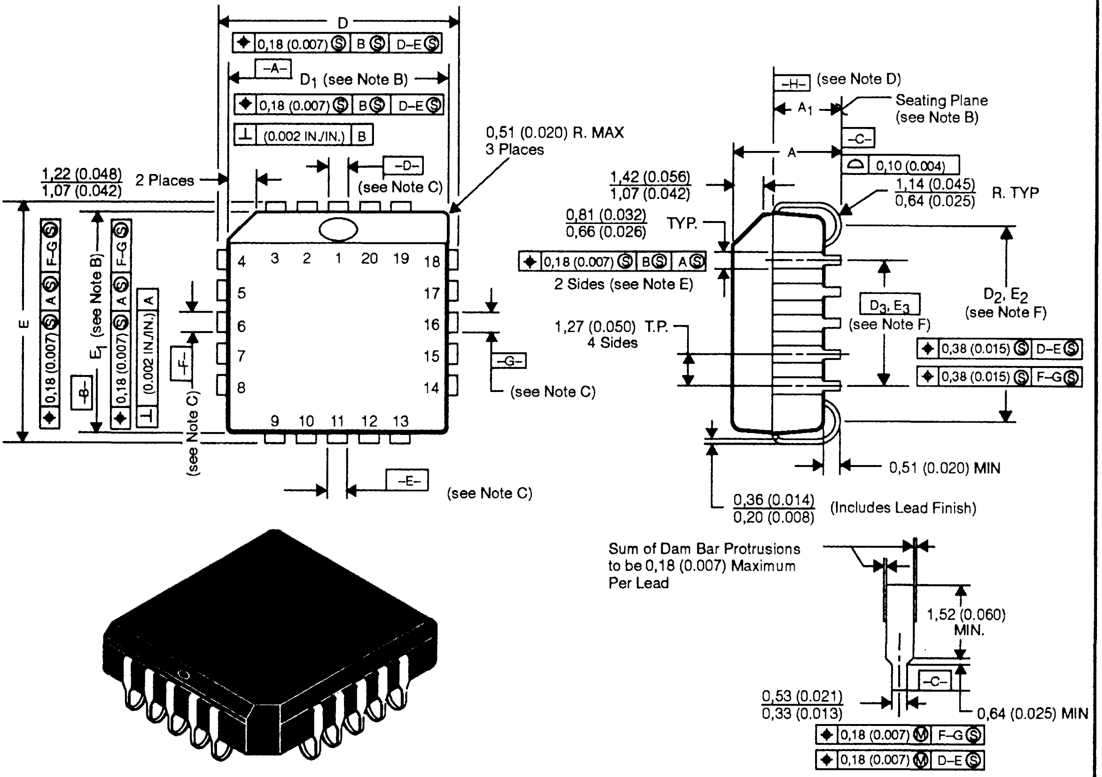


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

FN020 and FN028 plastic chip carrier packages

Each of these chip carrier packages consists of a circuit mounted on a lead frame and enncapsulated within an electrically nonconductive plastic compound. The compound withstands soldering temperatures with no deformation, and circuit performance characteristics remain stable when the devices are operated in high-humidity conditions. The package is intended for surface mounting on 1,27 (0.050) centers. Leads require no additional cleaning or processing when used in soldered assembly.

FN020 and FN028
(20-pin package used for illustration)



(see table on following page for additional dimensions)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. All dimensions conform to JEDEC Specification MO-047AA/AB. Dimensions and tolerancing are per ANSI Y14.5M – 1982.

B. Dimensions D_1 and E_1 do not include mold flash protrusion. Protrusion shall not exceed 0,25 (0.010) on any side. Centerline of center pin each side is within 0,10 (0.004) of package centerline by dimension B. The lead contact points are planar within 0,10 (0.004).

C. Datums D – E and F – G for center leads are determined at datum – H –.

D. Datum – H – is located at top of leads where they exit plastic body.

E. Location of datums – A – and – B – to be determined at datum – H –.

F. Determined at seating plane – C –.

FN020 and FN028 plastic chip carrier packages (continued)

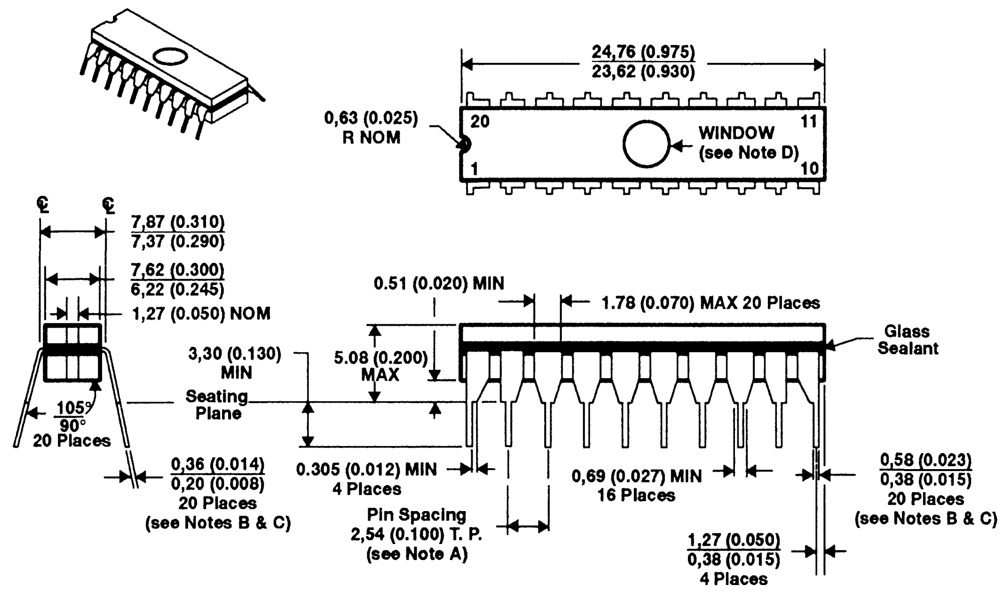
JEDEC OUTLINE	NO.OF PINS	A		A_1		D, E		D_1, E_1		D_2, E_2		D_3, E_3
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	BASIC
MO-047AA	20	4,19 (0.165)	4,57 (0.180)	2,29 (0.090)	3,05 (0.120)	9,78 (0.385)	10,03 (0.395)	8,89 (0.350)	9,04 (0.356)	7,37 (0.290)	8,38 (0.330)	5,08 (0.200)
MO-047AB	28	4,19 (0.165)	4,57 (0.180)	2,29 (0.090)	3,05 (0.120)	12,32 (0.485)	12,57 (0.495)	11,43 (0.450)	11,58 (0.456)	9,91 (0.390)	10,92 (0.430)	7,62 (0.300)

NOTES: A. All dimensions conform to JEDEC Specification MO-047AA/AB. Dimensions and tolerancing are per ANSI Y14.5M – 1982.
F. Determined at seating plane $\boxed{-C-}$.

J020 ceramic dual-in-line package

These hermetically sealed dual-in-line packages consist of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Solder-coated leads require no additional cleaning or processing when used in soldered assembly.

J020



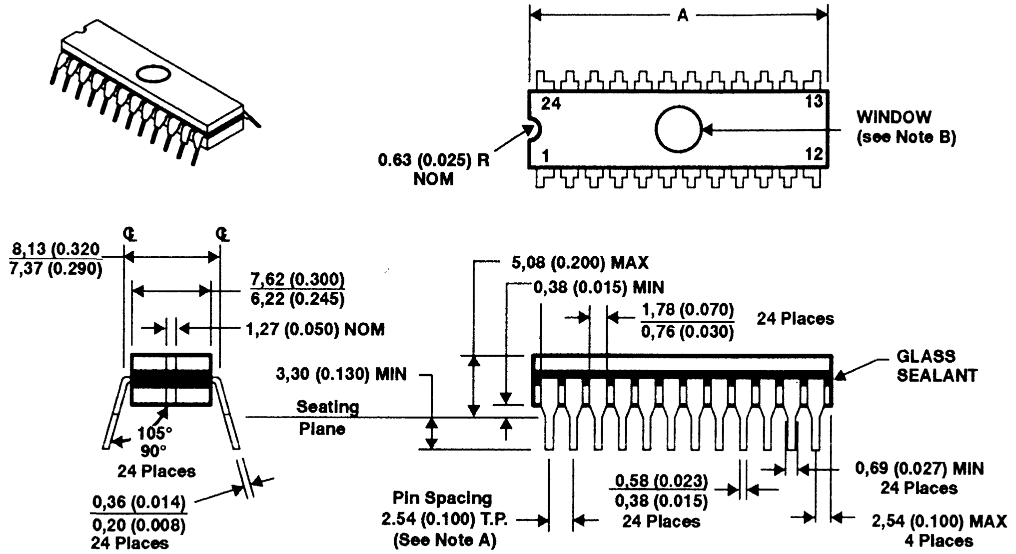
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES:
- A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
- B. This dimension does not apply for solder-dipped leads.
- C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above the seating plane
- D. The window is present only on UV-eraseable products.

JT024 and JT028 ceramic dual-in-line packages

These hermetically sealed dual-in-line packages consist of a ceramic base, ceramic cap, and a lead frame. Hermetic sealing is accomplished with glass. The package is intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Solder-coated leads require no additional cleaning or processing when used in soldered assembly.

JT024 and JT028
(24-pin package used for illustration)



PINS / DIM	24	28
A MAX	32,51 (1.280)	37,95 (1.480)

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

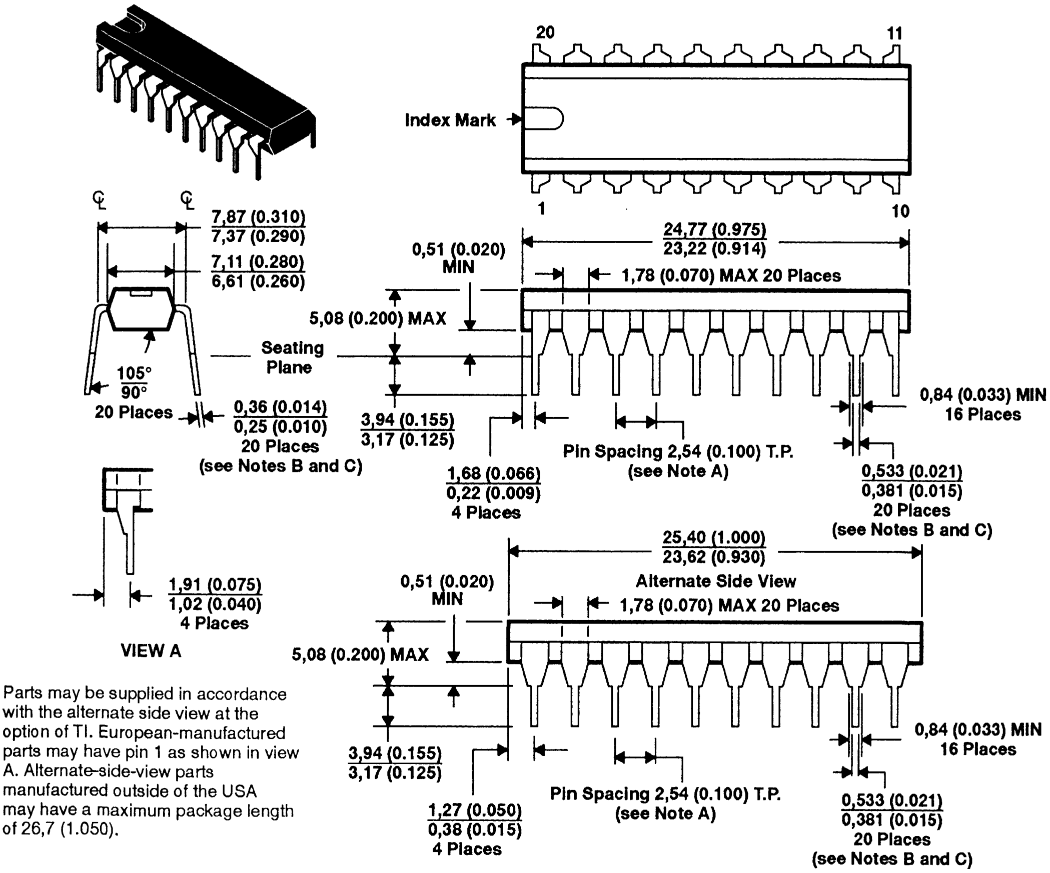
NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. The window is present only on UV-eraseable products.

N020 300-mil plastic dual-in-line package

This dual-in-line packages consists of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics will remain stable when operated in high-humidity conditions. These packages are intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

N020

Designation per JEDEC Std 30: PDIP-T20



Parts may be supplied in accordance with the alternate side view at the option of TI. European-manufactured parts may have pin 1 as shown in view A. Alternate-side-view parts manufactured outside of the USA may have a maximum package length of 26,7 (1.050).

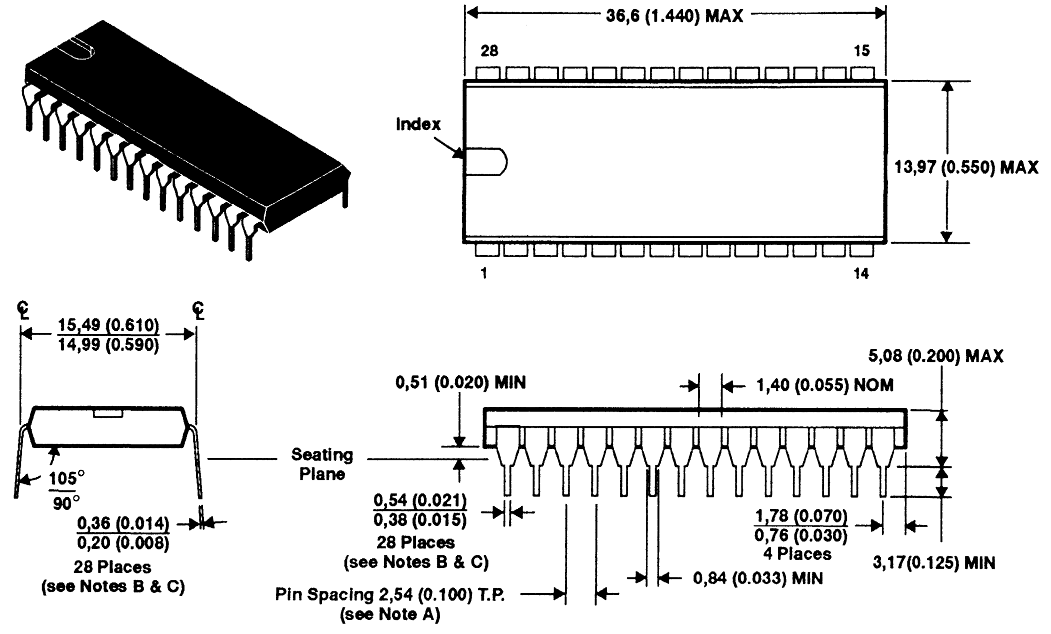
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

N028 600-mil plastic dual-in-line package

This dual-in-line package consist of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics will remain stable when operated in high-humidity conditions. These packages are intended for insertion in mounting-hole rows on 15,24 (0.600) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

N028



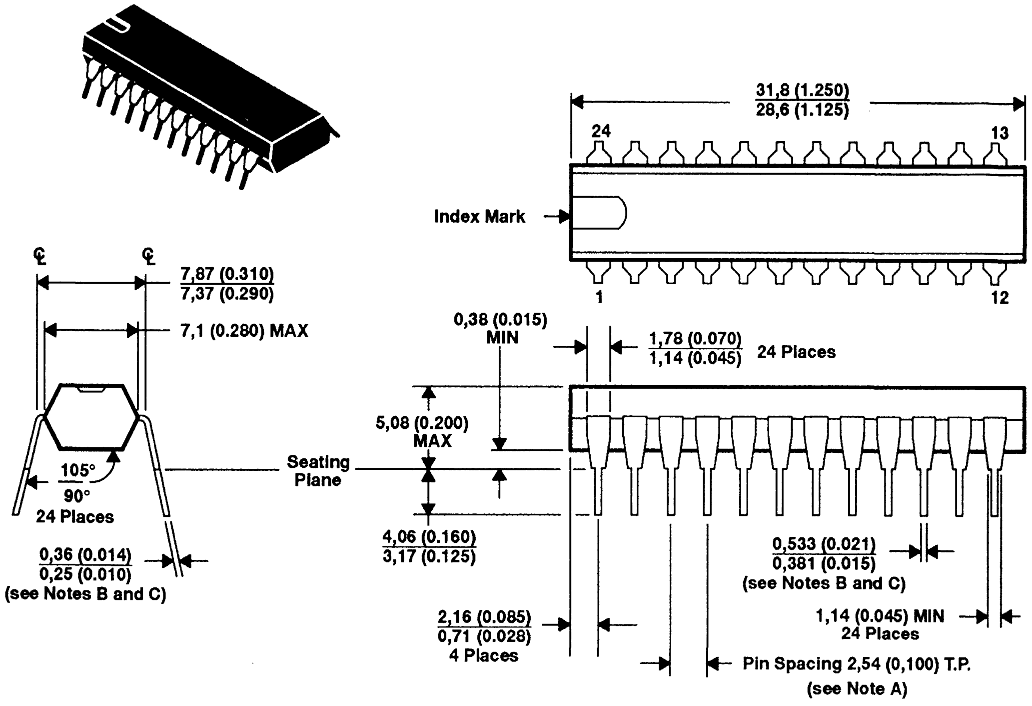
ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

NT024 300-mil plastic dual-in-line package

This dual-in-line package consist of a circuit mounted on a lead frame and encapsulated within a plastic compound. The compound will withstand soldering temperature with no deformation and circuit performance characteristics will remain stable when operated in high-humidity conditions. These packages are intended for insertion in mounting-hole rows on 7,62 (0.300) centers. Once the leads are compressed and inserted, sufficient tension is provided to secure the package in the board during soldering. Leads require no additional cleaning or processing when used in soldered assembly.

NT024

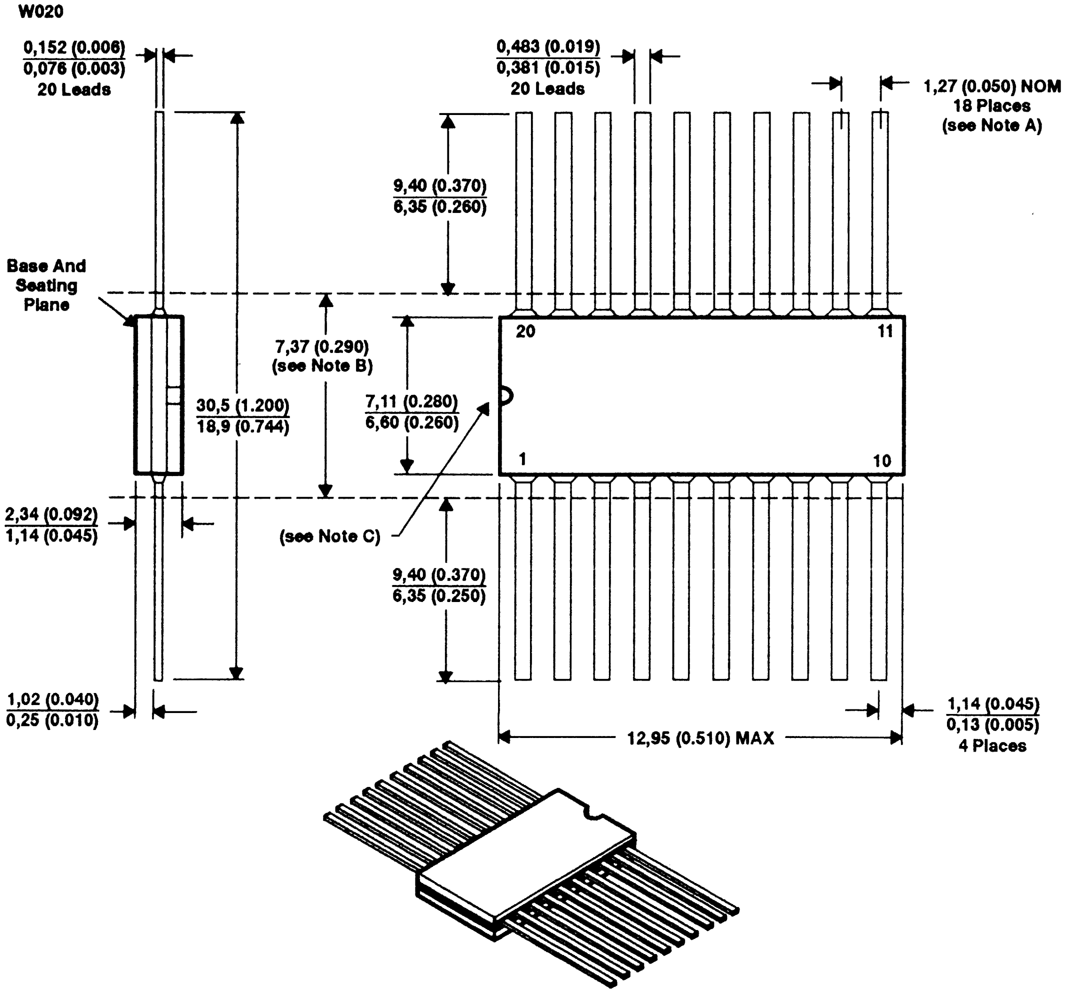


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Each pin centerline is located within 0,25 (0.010) of its true longitudinal position.
B. This dimension does not apply for solder-dipped leads.
C. When solder-dipped leads are specified, dipped area of the lead extends from the lead tip to at least 0,51 (0.020) above seating plane.

W020 ceramic flat package

This hermetically sealed flat package consists of an electrically nonconductive ceramic base and cap and a lead frame. Hermetic sealing is accomplished with glass. Leads require no additional cleaning or processing when used in soldered assembly.

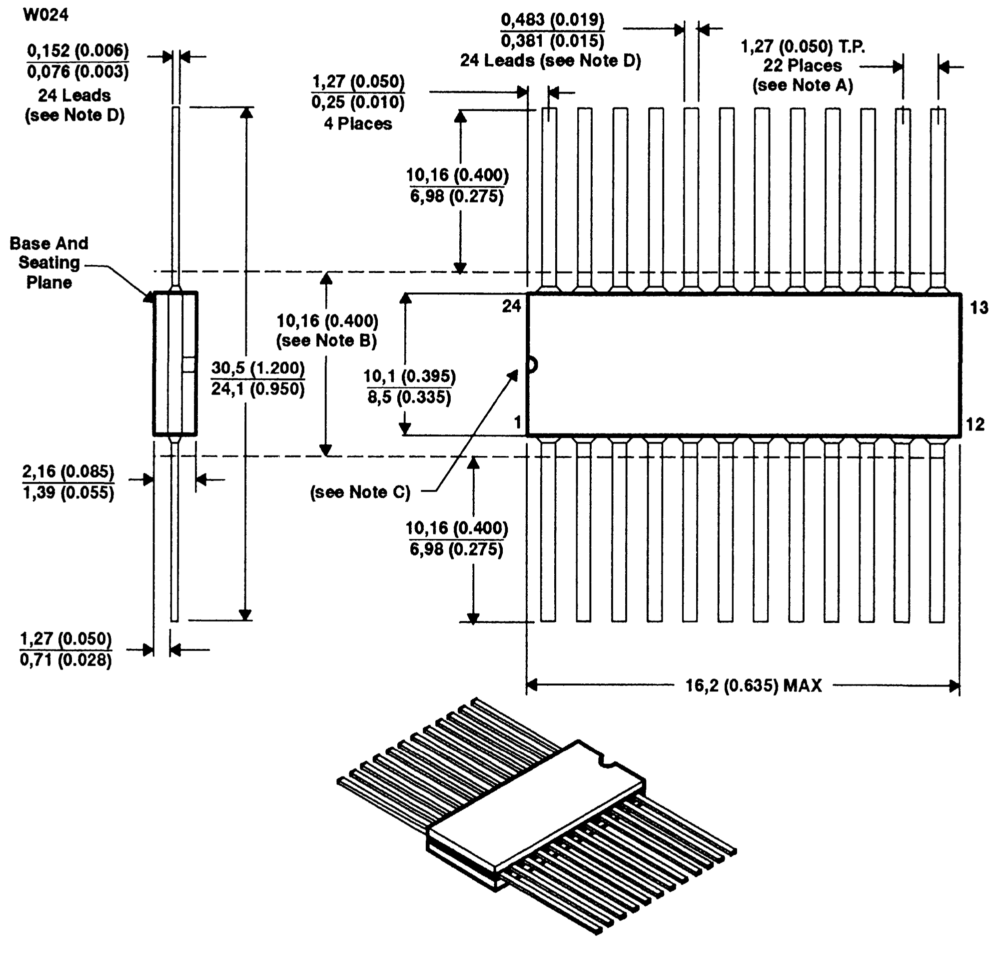


ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES: A. Leads are within 0,13 (0.005) radius of true position (T.P.) at maximum material condition.
B. This dimension determines a zone within which all body and lead irregularities lie.
C. Index point is provided on cap for terminal identification only.

W024 ceramic flat package

This hermetically sealed flat package consists of an electrically nonconductive ceramic base and cap and a lead frame. Hermetic sealing is accomplished with glass. Leads require no additional cleaning or processing when used in soldered assembly.



Falls Within JEDEC MO-019AA Dimensions

ALL LINEAR DIMENSIONS ARE IN MILLIMETERS AND PARENTHETICALLY IN INCHES

NOTES:
- A. Leads are within 0,13 (0.005) radius of true position (T.P.) at maximum material condition.
- B. This dimension determines a zone within which all body and lead irregularities lie.
- C. Index point is provided on cap for terminal identification only.
- D. Not applicable for solder-dipped leads. When solder-dipped leads are specified, dipped area extends from lead tip to within 1,27 (0.050) of the package body.

Notes

Notes

Notes

Notes

TI North American Sales Offices

ALABAMA: Huntsville: (205) 837-7530

ARIZONA: Phoenix: (602) 995-1007

CALIFORNIA: Irvine: (714) 660-1200
San Diego: (619) 278-9600
Santa Clara: (408) 980-9000
Woodland Hills: (818) 704-8100

COLORADO: Aurora: (303) 368-8000

CONNECTICUT: Wallingford: (203) 269-0074

FLORIDA: Altamonte Springs: (407) 260-2116
Fort Lauderdale: (305) 973-8502
Tampa: (813) 885-7588

GEORGIA: Norcross: (404) 662-7967

ILLINOIS: Arlington Heights: (708) 640-3000

INDIANA: Carmel: (317) 573-6400
Fort Wayne: (219) 489-4697

KANSAS: Overland Park: (913) 451-4511

MARYLAND: Columbia: (410) 964-2003

MASSACHUSETTS: Waltham: (617) 895-9100

MICHIGAN: Farmington Hills: (313) 553-1581

MINNESOTA: Eden Prairie: (612) 828-9300

MISSOURI: St. Louis: (314) 821-8400

NEW JERSEY: Iselin: (908) 750-1050

NEW MEXICO: Albuquerque: (505) 345-2555

NEW YORK: East Syracuse: (315) 463-9291
Fishkill: (914) 897-2900
Melville: (516) 454-6600
Pittsford: (716) 385-6770

NORTH CAROLINA: Charlotte: (704) 527-0930
Raleigh: (919) 876-2725

OHIO: Beachwood: (216) 765-7258
Beavercreek: (513) 427-6200

OREGON: Beaverton: (503) 643-6758

PENNSYLVANIA: Blue Bell: (215) 825-9500

PUERTO RICO: Hato Rey: (809) 753-8700

TEXAS: Austin: (512) 250-6769
Dallas: (214) 917-1264
Houston: (713) 778-6592
Midland: (915) 561-7137

UTAH: Salt Lake City: (801) 466-8972

WISCONSIN: Waukesha: (414) 798-1001

CANADA: Nepean: (613) 726-1970
Richmond Hill: (416) 884-9181
St. Laurent: (514) 335-8392

TI Regional Technology Centers

CALIFORNIA: Irvine: (714) 660-8140
Santa Clara: (408) 748-2222

GEORGIA: Norcross: (404) 662-7945

ILLINOIS: Arlington Heights: (708) 640-2909

INDIANA: Indianapolis: (317) 573-6400

MASSACHUSETTS: Waltham: (617) 895-9196

MEXICO: Mexico City: 491-70834

MINNESOTA: Minneapolis: (612) 828-9300

TEXAS: Dallas: (214) 917-3881

CANADA: Nepean: (613) 726-1970

Customer Response Center

TOLL FREE: (800) 336-5236
OUTSIDE USA: (214) 995-6611
(8:00 a.m. – 5:00 p.m. CST)

TI Authorized North American Distributors

Alliance Electronics, Inc. (military product only)
Almac/Arrow
Anthem Electronics
Arrow/Schweber
Future Electronics (Canada)
GRS Electronics Co., Inc.
Hall-Mark Electronics
Marshall Industries
Newark Electronics
Rochester Electronics, Inc.
(obsolete product only (508) 462-9332)
Wyle Laboratories
Zeus Components

TI Distributors

ALABAMA: Arrow/Schweber (205) 837-6955; Hall-Mark (205) 837-8700; Marshall (205) 881-9235.

ARIZONA: Anthem (602) 966-6600; Arrow/Schweber (602) 437-0750; Hall-Mark (602) 431-0030; Marshall (602) 496-0290; Wyle (602) 437-2088.

CALIFORNIA: Los Angeles/Orange County: Anthem (818) 775-1333, (714) 768-4444; Arrow/Schweber (818) 380-9686, (714) 838-5422; Hall-Mark (818) 773-4500, (714) 727-6000; Marshall (818) 878-7000, (714) 458-5301; Wyle (818) 880-9000, (714) 863-9953; Zeus (714) 921-9000, (818) 889-3838;

Sacramento: Anthem (916) 624-9744; Hall-Mark (916) 624-9781; Marshall (916) 635-9700; Wyle (916) 638-5282;

San Diego: Anthem (619) 453-9005; Arrow/Schweber (619) 565-4800; Hall-Mark (619) 268-1201; Marshall (619) 578-9600; Wyle (619) 565-9171; Zeus (619) 277-9681.

San Francisco Bay Area: Anthem (408) 453-1200; Arrow/Schweber (408) 441-9700, (510) 490-9477; Hall-Mark (408) 432-4000; Marshall (408) 942-4600; Wyle (408) 727-2500; Zeus (408) 629-4789.

COLORADO: Anthem (303) 790-4500; Arrow/Schweber (303) 799-0258; Hall-Mark (303) 790-1662; Marshall (303) 451-8383; Wyle (303) 457-9953.

CONNECTICUT: Anthem (203) 575-1575; Arrow/Schweber (203) 265-7741; Hall-Mark (203) 271-2844; Marshall (203) 265-3822.

FLORIDA: Fort Lauderdale: Arrow/Schweber (305) 429-8200; Halll-Mark (305) 971-9280; Marshall (305) 977-4880.

Orlando: Arrow/Schweber (407) 333-9300; Hall-Mark (407) 830-5855; Marshall (407) 767-8585; Zeus (407) 788-9100.

Tampa: Hall-Mark (813) 541-7440; Marshall (813) 573-1399.

GEORGIA: Arrow/Schweber (404) 497-1300; Hall-Mark (404) 623-4400; Marshall (404) 923-5750.

ILLINOIS: Anthem (708) 884-0200; Arrow/Schweber (708) 250-0500; Hall-Mark (312) 860-3800; Marshall (708) 490-0155; Newark (312)784-5100.

INDIANA: Arrow/Schweber (317) 299-2071; Hall-Mark (317) 872-8875; Marshall (317) 297-0483.

IOWA: Arrow/Schweber (319) 395-7230.

KANSAS: Arrow/Schweber (913) 541-9542; Hall-Mark (913) 888-4747; Marshall (913) 492-3121.

MARYLAND: Anthem (301) 995-6640; Arrow/Schweber (301) 596-7800; Hall-Mark (301) 988-9800; Marshall (301) 622-1118; Zeus (301) 997-1118.

MASSACHUSETTS: Anthem (508) 657-5170; Arrow/Schweber (508) 658-0900; Hall-Mark (508) 667-0902; Marshall (508) 658-0810; Wyle (617) 272-7300; Zeus (617) 246-8200.

MICHIGAN: Detroit: Arrow/Schweber (313) 462-2290; Hall-Mark (313) 416-5800; Marshall (313) 525-5850; Newark (313) 967-0600.

MINNESOTA: Anthem (612) 944-5454; Arrow/Schweber (612) 941-5280; Hall-Mark (612) 881-2600; Marshall (612) 559-2211.

MISSOURI: Arrow/Schweber (314) 567-6888; Hall-Mark (314) 291-5350; Marshall (314) 291-4650.

NEW JERSEY: Anthem (201) 227-7960; Arrow/Schweber (201) 227-7880, (609) 596-8000; Hall-Mark (201) 515-3000, (609) 235-1900; Marshall (201) 882-0320, (609) 234-9100.

NEW MEXICO: Alliance (505) 292-3360.

NEW YORK: Long Island: Anthem (516) 864-6600; Arrow/Schweber (516) 231-1000; Hall-Mark (516) 737-0600; Marshall (516) 273-2424; Zeus (914) 937-7400.

Rochester: Arrow/Schweber (716) 427-0300; Hall-Mark (716) 425-3300; Marshall (716) 235-7620.

Syracuse: Marshall (607) 785-2345.

NORTH CAROLINA: Arrow/Schweber (919) 876-3132; Hall-Mark (919) 872-0712; Marshall (919) 878-9882.

OHIO: Cleveland: Arrow/Schweber (216) 248-3990; Hall-Mark (216) 349-4632; Marshall (216) 248-1788.

Columbus: Hall-Mark (614) 888-3313.

Dayton: Arrow/Schweber (513) 435-5563; Marshall (513) 898-4480; Zeus (513) 293-6162.

OKLAHOMA: Arrow/Schweber (918) 252-7537; Hall-Mark (918) 254-6110.

OREGON: Almac/Arrow (503) 629-8090; Anthem (503) 643-1114; Marshall (503) 644-5050; Wyle (503) 643-7900.

PENNSYLVANIA: Anthem (215) 443-5150; Arrow/Schweber (215) 928-1800; GRS (215) 922-7037; (609) 964-8560; Marshall (412) 788-0441.

TEXAS: Austin: Arrow/Schweber (512) 835-4180; Hall-Mark (512) 258-8848; Marshall (512) 837-1991; Wyle (512) 345-8853;

Dallas: Anthem (214) 238-7100; Arrow/Schweber (214) 380-6464; Hall-Mark (214) 553-4300; Marshall (214) 233-5200; Wyle (214) 235-9953; Zeus (214) 783-7010;

Houston: Arrow/Schweber (713) 530-4700; Hall-Mark (713) 781-6100; Marshall (713) 467-1666; Wyle (713) 879-9953.

UTAH: Anthem (801) 973-8555; Arrow/Schweber (801) 973-6913; Marshall (801) 973-2288; Wyle (801) 974-9953.

WASHINGTON: Almac/Arrow (206) 643-9992, Anthem (206) 483-1700; Marshall (206) 486-5747; Wyle (206) 881-1150.

WISCONSIN: Arrow/Schweber (414) 792-0150; Hall-Mark (414) 797-7844; Marshall (414) 797-8400.

CANADA: Calgary: Future (403) 235-5325;

Edmonton: Future (403) 438-2858;

Montreal: Arrow/Schweber (514) 421-7411; Future (514) 694-7710; Marshall (514) 694-8142

Ottawa: Arrow/Schweber (613) 226-6903; Future (613) 820-8313.

Quebec: Future (418) 897-6666.

Toronto: Arrow/Schweber (416) 670-7769; Future (416) 612-9200; Marshall (416) 458-8046.

Vancouver: Arrow/Schweber (604) 421-2333; Future (604) 294-1166.

TI Die Processors

Chip Supply	(407) 298-7100
Elmo Semiconductor	(818) 768-7400
Minco Technology Labs	(512) 834-2022

TEXAS INSTRUMENTS

D0892

©1992 Texas Instruments Incorporated

TI Worldwide Sales Offices

ALABAMA: Huntsville: 4960 Corporate Drive,
Suite 150, Huntsville, AL 35805, (205) 837-7530.

ARIZONA: Phoenix: 8825 N. 23rd Avenue, Suite 100,
Phoenix, AZ 85021, (602) 995-1007.

CALIFORNIA: Irvine: 1920 Main Street, Suite 900,
Irvine, CA 92714, (714) 660-1200;
San Diego: 5625 Ruffin Road, Suite 100,
San Diego, CA 92123, (619) 278-9600;
Santa Clara: 5353 Betsy Ross Drive,
Santa Clara, CA 95054, (408) 980-9000;
Woodland Hills: 21550 Oxnard Street, Suite 700,
Woodland Hills, CA 91367, (818) 704-8100.

COLORADO: Aurora: 1400 S. Potomac Street, Suite 101,
Aurora, CO 80012, (303) 368-8000.

CONNECTICUT: Wallingford: 9 Barnes Industrial Park
So., Wallingford, CT 06492, (203) 269-0074.

FLORIDA: Altamonte Springs: 370 S. North Lake
Boulevard, Suite 1008, Altamonte Springs, FL 32701,
(407) 260-2116;
Fort Lauderdale: 2950 N.W. 62nd Street,
Suite 100, Fort Lauderdale, FL 33309,
(305) 973-8502; **Tampa:** 4803 George Road, Suite 390,
Tampa, FL 33634-6234, (813) 885-7588.

GEORGIA: Norcross: 5515 Spalding Drive,
Norcross, GA 30092-2560, (404) 662-7967.

ILLINOIS: Arlington Heights: 515 West Algonquin,
Arlington Heights, IL 60005, (708) 640-6925.

INDIANA: Carmel: 550 Congressional Drive, Suite 100,
Carmel, IN 46032, (317) 573-6400;
Fort Wayne: 103 Airport North Office Park,
Fort Wayne, IN 46825, (219) 489-4697.

KANSAS: Overland Park: 7300 College Boulevard,
Lighton Plaza, Suite 150, Overland Park, KS 66210,
(913) 451-4511.

MARYLAND: Columbia: 8815 Centre Park Drive,
Suite 100, Columbia, MD 21045, (410) 964-2003.

MASSACHUSETTS: Waltham: Bay Colony Corporate
Center 950 Winter Street, Suite 2800, Waltham, MA 02154,
(617) 895-9100.

MICHIGAN: Farmington Hills: 33737 W. 12 Mile Road,
Farmington Hills, MI 48018, (313) 553-1581.

MINNESOTA: Eden Prairie: 11000 W. 78th Street,
Suite 100, Eden Prairie, MN 55344, (612) 828-9300.

MISSOURI: St. Louis: 12412 Powerscourt Drive,
Suite 125, St. Louis, MO 63131, (314) 821-8400.

NEW JERSEY: Iselin: Metropolitan Corporate Plaza, 485
Bldg E. U.S. 1 South, Iselin, NJ 08830, (908) 750-1050.

NEW MEXICO: Albuquerque: 2709 J. Pan American
Freeway, N.E., Albuquerque, NM 87101, (505) 345-2555.

NEW YORK: East Syracuse: 6365 Collamer Drive,
East Syracuse, NY 13057, (315) 463-9291;
Fishkill: 300 Westage Business Center, Suite 140,
Fishkill, NY 12524, (914) 897-2900;
Melville: 48 South Service Road, Suite 100, Melville, NY
11747, (516) 454-6601;
Pittsford: 2851 Clover Street, Pittsford, NY 14534,
(716) 385-6770.

NORTH CAROLINA: Charlotte: 8 Woodlawn Green,
Suite 100, Charlotte, NC 28217, (704) 527-0930;
Raleigh: 2809 Highwoods Boulevard, Suite 100,
Raleigh, NC 27625, (919) 876-2725.

OHIO: Beachwood: 23775 Commerce Park Road,
Beachwood, OH 44122-5875, (216) 765-7258;
Beavercreek: 4200 Colonel Glenn Highway, Suite 600,
Beavercreek, OH 45431, (513) 427-6200.

OREGON: Beaverton: 6700 S.W. 105th Street,
Suite 110, Beaverton, OR 97005, (503) 643-6758.

PENNSYLVANIA: Blue Bell: 670 Sentry Parkway,
Suite 200, Blue Bell, PA 19422, (215) 825-9500.

PUERTO RICO: Hato Rey: 615 Mercantile Plaza Building,
Suite 505, Hato Rey, PR 00919, (809) 753-8700.

TEXAS: Austin: 12501 Research Boulevard,
Austin, TX 78759, (512) 250-6769;
Dallas: 7839 Churchill Way, Dallas, TX 75251,
(214) 917-1264;
Houston: 9301 Southwest Freeway, Commerce Park, Suite
360, Houston, TX 77074, (713) 778-6592;
Midland: FM 1788 & I-20, Midland, TX 79711-0448.
(915) 561-7137.

UTAH: Salt Lake City: 2180 South 1300 East, Sute 335,
Salt Lake City, UT 54106, (801) 466-8972.

WISCONSIN: Waukesha: 20825 Swenson Drive,
Suite 900, Waukesha WI 53186, (414) 798-1001.

CANADA: Nepean: 301 Moodie Drive, Suite 102, Mallom
Center, Nepean, Ontario, Canada K2H 9C4,
(613) 726-1970;
Richmond Hill: 280 Centre Street East, Richmond Hill,
Ontario, Canada L4C 1B1, (416) 884-9181;
St. Laurent: 9460 Trans Canada Highway, St. Laurent,
Quebec, Canada H4S 1R7, (514) 335-8392.

AUSTRALIA (& NEW ZEALAND): Texas Instruments
Australia Ltd., 6-10 Talavera Road, North Ryde (Sydney),
New South Wales, Australia 2113, 2-878-9000; 14th Floor,
380 Street, Kilda Road, Melbourne, Victoria, Australia 3004,
3-696-1211; 171 Philip Highway, Elizabeth, South Australia
5112, 8 255-2066.

BELGIUM: Texas Instruments Belgium S.A./N.V.,
Avenue Jules Bordetlaan 11, 1140 Brussels, Belgium,
(02) 242 30 80.

BRAZIL: Texas Instruments Electronicos do Brasil Ltda.,
Av. Eng. Luiz Carlos Berrini 1461-11o andar, 04571,
Sao Paulo, SP, Brazil, 11-535–5133.

DENMARK: Texas Instruments A/S, Borupvang 2D,
2750 Ballerup, Denmark, (44) 68 74 00.

FINLAND: Texas Instruments OY, Ahertajantle 3,
P.O. Box 86, 02321 Espoo, Finland, (0) 802 6517.

FRANCE: Texas Instruments France, 8-10 Avenue
Morane-Saulnier, B.P. 67, 78141 Velizy Villacoublay Cedex,
France, (1) 30 70 1003.

GERMANY: Texas Instruments Deutschland GmbH.,
Haggertystrasse 1, 8050 Freising, (08161) 80-0;
Kurfurstendamm 195-196, 1000 Berlin 15, (030) 8 82 73 65;
Dusseldorfer Strasse 40, 6236 Eschborn 1, (06196) 80 70;
Kirchhorster Strasse 2, 3000 Hannover 51, (0511) 64 68-0;
Maybachstrasse II, 7302 Ostfildern 2 (Nellingen),
(0711) 3403257; Gildehofcenter, Hollestrasses 3, 4300
Essen 1, (0201) 24 25-0.

HOLLAND: Texas Instruments Holland B.V., Hogehilweg
19, Postbus 12995, 1100 AZ Amsterdam-Zuidoost, Holland,
(020) 5602911.

HONG KONG: Texas Instruments Hong Kong Ltd., 8th
Floor, World Shipping Center, 7 Canton Road, Kowloon,
Hong Kong, 737-0338.

HUNGARY: Texas Instruments Representation, Budaorsi
ut.42, 1112 Budapest, Hungary, (1) 1 66 66 17.

IRELAND: Texas Instruments Ireland Ltd., 7/8 Harcourt
Street, Dublin 2, Ireland, (01) 755233.

ITALY: Texas Instruments Italia S.p.A., Centro Direzionale
Colleoni, Palazzo Perseo-Via Paracelso 12, 20041 Agrate
Brianza (Mi), Italy, (039) 63221; Via Castello della Magliana,
38, 00148 Roma, Italy (06) 6572651; Via Amendola, 17,
40100 Bologna, Italy (051) 554004.

JAPAN: Texas Instruments Japan Ltd., Aoyama Fuji
Building 3-6-12 Kita-Aoyama Minato-ku, Tokyo, Japan 107,
03-498-2111; MS Shibaura Building 9F, 4-13-23 Shibaura,
Minato-ku, Tokyo, Japan 108, 03-769-8700; Nissho-iwai
Building 5F, 2-5-8 Imabashi, Chuou-ku, Osaka, Japan 541,
06-204-1881; Dai-ni Toyota Building Nishi-kan 7F, 4-10-27
Meieki, Nakamura-ku, Nagoya, Japan 450, 052-583-8691;
Kanazawa Oyama-cho Daiichi Seimei Building 6F, 3-10
Oyama-cho, Kanazawa, Ishikawa, Japan 920,
0762-23-5471; Matsumoto Showa Building 6F, 1-2-11
Fukashi, Matsumoto, Nagano, Japan 390, 0263-33-1060;
Daiichi Olympic Tachikawa Building 6F, 1-25-12,
Akebono-cho, Tachikawa, Tokyo, Japan 190,
0425-27-6760; Yokohama Business Park East Tower 10F,
134 Goudo-cho Hodogaya-ku, Yokohama-shi, Kanagawa,
Japan 240, 045-338-1220; Nihon Seimei Kyoto Yasaka
Building 5F, 843-2, Higashi Shiokohji-cho, Higashi-iru,
Nishinotoh-in, Shiokohji-dori, Shimogyo-ku, Kyoto, Japan
600, 075-341-7713; Sumitomo Seimei Kumagaya Building
8F, 2-44 Yayoi, Kumagaya, Saitama, Japan 360,
0485-22-2440; 2597-1, Aza Harudai, Oaza Yasaka, Kitsuki,
Oita, Japan 873, 09786-3-3211.

KOREA: Texas Instruments Korea Ltd., 28th Floor, Trade
Tower, 159, Samsung-Dong, Kangnam-ku Seoul, Korea, 2
551-2800.

MALAYSIA: Texas Instruments Malaysia, Sdn. Bhd., Asia
Pacific, Lot 36.1 #Box 93, Menara Maybank, 100 Jalan Tun
Perak, 50050 Kuala Llumpur, Malaysia, 2306001.

MEXICO: Texas Instruments de Mexico S.A., de C.V.,
Alfonso Reyes 115, Col. Hipodromo Condesa, Mexico, D.F.,
Mexico 06170, 5-515-6081.

NORWAY: Texas Instruments Norge A/S, P.B. 106, Refstad
(Sinsenveien 53), 0513 Oslo 5, Norway, (02) 155 090.

PEOPLE'S REPUBLIC OF CHINA: Texas Instruments
China Inc., Beijing Representative Office, 7-05 CITIC
Building, 19 Jianguomenwai Dajie, Beijing, China,
500-2255, Ext. 3750.

PHILIPPINES: Texas Instruments Asia Ltd.,
Philippines Branch, 14th Floor, Ba-Lepanto Building,
Paseo de Roxas, Makati, Metro Manila, Philippines,
2-8176031.

PORTUGAL: Texas Instruments Equipamento Electronico
(Portugal) Ltda., Ing. Frederico Ulricho, 2650 Moreira Da
Maia, 4470 Maia, Portugal (2) 948 1003.

**SINGAPORE (& INDIA, INDONESIA, MALAYSIA,
THAILAND):** Texas Instruments Singapore (PTE) Ltd.,
Asia Pacific, 101 Thomson Road, #23-01,
United Square, Singapore 1130, 3508100.

SPAIN: Texas Instruments Espana S.A., c/Gobelas 43,
Urbanizasion, La Florida, 28023, Madrid, Spain, (1) 372
8051; c/Diputacion, 279-3-5, 08007 Barcelona, Spain, (3)
317 91 80.

SWEDEN: Texas Instruments International Trade
Corporation (Sverigefilialen), Isafjordsgaton, Box 30, S-164
93 Kista, Sweden, (08) 752 58 00.

SWITZERLAND: Texas Instruments Switzerland AG,
Riedstrasse 6, C8953 Dietikon, Switzerland,
(01) 744 2811.

TAIWAN: Texas Instruments Taiwan Limited, Taipei
Branch, 10th Floor Bank Tower, 205 Tung Hwa N. Road,
Taipei, Taiwan, 10592 Republic of China, 2-7139311.

TURKEY: Texas Instruments, DSEG MidEast Regional
Marketing Office, Karum Center, Suite 442, Iran Caddesi
21, 06680 Kavakldere, Ankara, Turkey, 4-468-0155.

UNITED KINGDOM: Texas Instruments Ltd., Manton Lane,
Bedford, England, MK41 7PA, (0234) 270 111.

TI Authorized North American Distributors

- Alliance Electronics, Inc. (military product only)
- Almac/Arrow
- Anthem Electronics
- Arrow/Schweber
- Future Electronics (Canada)
- GRS Electronics Co., Inc. *
- Hall-Mark Electronics
- Marshall Industries
- Newark Electronics *
- Wyle Laboratories
- Zeus Components
- Rochester Electronics, Inc. (obsolete product only)

*Not authorized for TI military products

TEXAS INSTRUMENTS

B0892

©1992 Texas Instruments Incorporated

TEXAS
INSTRUMENTS

Printed in U.S.A.

SRPD001A